

**Rockchip**  
**RV1109/RV1126**  
**Technical Reference Manual**  
**Part2**

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## Appendix

Abbreviation	Full Name	Instruction
ACA	Accessory Charger Adapter	An adaptor which allows a single USB port to be attached to both a charger and another device at the same time.
ADC	Analog-to-Digital Converter	Used to convert analog signal to digital signal.
AE	Automatic Exposure	Realizes the function of automatic exposure processing.
AF	Auto Focus	Realizes the measurement of image definition.
AGC	Automatic Gain Control	An adaptive system found in electronic devices that automatically controls the gain of a signal: the average output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels.
AI	Artificial Intelligence	A new technical science to study and develop theories, methods, techniques and application systems for simulating, extending and extending human intelligence.
AVC	Advanced Video Coding	One video agreement, also can be called H.264
AVS	Audio Video coding Standard	One video agreement
AWB	Automatic White Balance	Provides the white balance function, and configures the gains of the R, Gr, Gb, and B components.
BCSH	Brightness, Contrast, Saturation and Hue	BCSH is used for brightness, contrast, saturation and hue adjustment.
BLC	Black Level Correction	A function to subtract a DC offset from picture data.
BLE	Blending	Gather many source data to final output data
CC	Combining Check	Can correction wrong ME and MC.
CCM	Color Correction Matrix	Used to correct the color crosstalk because of three channel response of sensor when only one channel color input.
CDP	Charging Downstream Port	A Charging Downstream Port (CDP) is a downstream port on a device that complies with the USB 2.0 definition of a host or a hub, except that it shall support the Charging Downstream Port features specified herein.
CMD	Command	Command
CMOS	Complementary Metal Oxide Semiconductor	Use for CMOS sensor
CSC	Color Space Convert	RGB2YUV, YUV2RGB
CSI	Camera Serial Interface	A standard interface between a camera and a host processor for mobile applications.
DAC	Digital-to-Analog Converter	A system that converts a digital signal into an analog signal.
DAP	Debug Access Port	A TAP block that acts as an AMBA (AHB or AHB-Lite) master for access to a system bus. The DAP is the term used to encompass a set of modular blocks that support system wide debug. The DAP is a modular component, intended to be extendable to support optional access to multiple systems such as memory mapped AHB and

Abbreviation	Full Name	Instruction
		CoreSight APB through a single debug interface.
DCP	Dedicated Charging Port	A downstream port on a device that outputs power through a USB connector, but is not capable of enumerating a downstream device
DCT	Discrete Cosine Transform	One video encoder tool.
DDR	Double Data Rate	A kind of dynamic memory.
DDR3	Double Data Rate 3	A kind of dynamic memory.
DDR3L	Double Data Rate 3 Low Voltage	A kind of dynamic memory.
DDR4	Double Data Rate 4	A kind of dynamic memory.
DFI	DDR PHY Interface	An interface protocol that defines the signals, timing parameters, and programmable parameters required to transfer control information and data over the DFI, to and from the DRAM devices, and between the MC and the PHY.
DMA	Direct Memory Access	A feature of computer systems that allows certain hardware subsystems to access main system memory, independent of the central processing unit (CPU).
DMAC	Direct Memory Access Controller	A programmable controller that manages DMA transfers.
DPCC	Defect Pixel Cluster Correction	Used to correct the defect pixels of the sensor, and supports both static and dynamic mode.
DST	Destination	Destination Image
DVP	Digital Video Port	A traditional sensor output interface. The video data are output in parallel.
EEDI	Enhanced Edge based Interpolation	Could interpolation smaller than 10 degree.
EHCI	Enhanced Host Controller Interface	The Enhanced Host Controller Interface (EHCI) for a Host Controller for the USB2.0
EOI	End Of Interrupt	Indicate the completion of interrupt processing for a given interrupt.
FBC	Frame Buffer Compression	A kind of method to reduce DDR bandwidth
FBCD	Frame Buffer Compression Decoder	Decode TNR and NR compression data from ddr under their respective fbcd mode.
FBCE	Frame Buffer Compression Encoder	Encode TNR, Sharp and FEC data to ddr under their respective fbce mode.
FEC	Fisheye Correction	Implemented by backward mapping.
FIFO	First In First Out	A method for organizing and manipulating a data buffer, where the oldest (first) entry, or head of the queue, is processed first.
FPN	Fixed Pattern Noise	A function for fixed pattern noise
FPS	Frame per Second	It is express that how many frames can be decoded by VDPU at one second.
FRC	Frame Rate Control	An algorithm of dither
FS	Full Speed	Full Speed model in USB2.0
GIC	Green Imbalance Correction	A method to correct the color imbalance in captured images
GPIO	General Purpose Input/Output	An uncommitted digital signal pin on an integrated circuit whose behavior (including whether it acts as input or output) is controllable by the user at run time.
HDR	High-Dynamic Range	Realize the function of three/two frames

Abbreviation	Full Name	Instruction
		synthesizing one frame.
HEVC	High Efficiency Video Coding	One video agreement, also can be called H.265
HNP	Host Negotiation Protocol	Host Negotiation Protocol in USB OTG Specification.
HS	High Speed	High Speed model in USB2.0
I2C	Inter-Integrated Circuit	Two wired (SCL and SDA), bi-directional serial bus
I2S	Inter-IC Sound, Integrated Interchip Sound	It is one of digital audio transmission standard.
IEP	Image Enhancement Processor	The main function is deinterlace.
Int8	Integer 8	8 bit integer including 1 bit sign bit
ISP	Image Signal Processor	contains standard sensor picture data processing functions
ISPP	Image Signal Post-Processing	Contains image post-processing and scaling function.
IXOY	Input X Fields Output Y frame	A kind of deinterlace mode(X and Y mean a number ).
JFIF	JPEG File Interchange Format	One image file standard.
JPEG	Joint Photographic Experts Group	One video agreement, used for picture compress.
LCD	Liquid Crystal Display	A type of display.
LDCH	Lens-Distortion	Achieves distortion correction under fisheye lens.
LPDDR3	Low Power Double Data Rate 3	A kind of dynamic memory.
LPDDR4	Low Power Double Data Rate 4	A kind of dynamic memory.
LS	Low Speed	Low Speed model in USB2.0
LSC	Lens Shading Correction	A function for lens shading problem
LUT	Look Up Table	Look Up Table
LVDS	Low-Voltage Differential Signaling	A differential signal technology with low power consumption, low bit error rate, low crosstalk and low radiation.
MAD	Multiply-add Unit	This is the unit designed to process multiply-add operation
MBAFF	Macro-block Adaptive Field Frame	One feature of h.264 stream.
MBPS	Mega Bits Per Second	The express that how many bits can be decoded by VDPU at one second.
MC	Motion Compensation	Filed based
MD	Motion Detection	Frame based
ME	Motion Estimate	Frame based
MI	Memory Interface	Write or read back data interface
MIPI	Mobile Industry Processor Interface	An open standard and specification for mobile application processors initiated by the MIPI consortium
MSPS	Million sample per second	Sample rate
MTL	Media Access Controller Transaction	The MAC Transaction Layer (MTL) provides the FIFO memory Interface to buffer and regulate the

Abbreviation	Full Name	Instruction
	Layer	packets between the application system memory and the MAC. It also enables the data to be transferred between the application clock and MAC clock domains. The MTL layer has two data paths: Transmit path and Receive Path.
MV	Motion Vector	Frame based
MVC	Multiview Video Coding	Also known as MVC 3D, it is a stereoscopic video coding standard for video compression.
NG	Noise Gate	A module used to detect and gate the noise.
NIU	Network Interface Units	NIU convert the incoming transaction information into special internal packets.
NN	Neural Network	Artificial Neural Network used in Deep Learning.
NPU	Neural Process Unit	NPU is the process unit which is dedicated to neural network. It is designed to accelerate the neural network arithmetic in field of AI (artificial intelligence) such as machine vision and natural language processing.
OHCI	Open Host Controller Interface	Open Host Controller Interface for USB.
OSD	On Screen Display	An on screen menu for making adjustments to the display
OTG	On The Go	This means USB can be host or device by configuration.
OTP	One Time Programmable	One Time Programmable Non-Volatile Memory system.
OTP NVM	One Time Programmable Non-Volatile Memory	One Time Programmable Non-Volatile Memory.
PCM	Pulse Code Modulation	A method used to digitally represent sampled analog signals. In a PCM stream, the amplitude of the analog signal is sampled regularly at uniform intervals, and each sample is quantized to the nearest value within a range of digital steps.
PD	Pull Down	A kind of film.
PDAF	Phase Detection Auto Focus	Replaces the PDAF points inside the raw input data
PDM	Pulse Density Modulation	A 1-bit over sampled audio format
PGA	Programmable Gain Amplifier	It can be controlled by software to amplify or decrease the amplitude of signal.
PWM	Pulse Width Modulation	A method for getting analog results with digital means. Digital control is used to create a square wave, a signal switched between on and off.
QoS	Quality of Service	The statistical allocation of throughput and delay, in terms of bandwidth and latency.
RAWNR	RAW Noise Reduction	Noise reduction on RAW domain
RGA	Raster Graphic Acceleration	Include image scale, alpha, overlay, rotation and so on.
RISC-V	Reduced Instruction Set Computer Five	RISC-V (pronounced "risk-five") is a new instruction set architecture (ISA) that was originally designed to support computer architecture research and education, but which we now hope will also become a standard free and open architecture for industry

Abbreviation	Full Name	Instruction
		implementations.
ROI	Region Of Interest	Tile based, Part of interest region in one picture
RSP	Role Swap Protocol	Role Swap Protocol in USB OTG Specification.
RX	Receive	
S/s	sample per second	Sample rate
SAR-ADC	Successive Approximation Register (SAR) A/D Converter	Voltage scaling module
SDP	Standard Downstream Port	A Standard Downstream Port (SDP) refers to a downstream port on a device that complies with the USB2.0 definition of a host or hub.
SDRAM	Synchronous Dynamic Random-access Memory	A kind of dynamic memory.
SLC	Single-Level Cell	Each cell in flash can only store 1bit data
SOF	Start of Frame	The first transaction in each (micro)frame. An SOF allows endpoints to identify the start of the (micro)frame and synchronize internal endpoint clocks to the host.
SRC	Source	Source Image
TDM	Time Division Multiplexing	TDM uses different time periods of the same physical connection to transmit different signals
TMO	Tone mapping	Realize wide dynamic compression
TNR	Time based Noise Reduction	Reduce noises to ensure that the image is quiet with the edges and details kept in YUV domain.
TS-ADC	Temperature-Sensor ADC	Temperature scaling module
TX	Transmit	
USB	Universal Serial Bus	Universal Serial Bus for peripheral.
UTMI	USB 2.0 Transceiver Macrocell Interface	Transceiver Macrocell Interface for USB2.0.
UVNR	UV based Noise Reduction	Filter the color noise
VDPU	Video Decoder Process Unit	A processor that can decoder video stream to picture for display.
VEPU	Video Encoder Process Unit	A processor that can encoder picture to video stream.
VOP	Video Output Processor	A video process engine and a display interface from memory frame buffer to display device.
VPU	Video Process Unit	Include VDPU and VEPU.
WDR	Wide Dynamic Range	Make the particularly bright and dark parts of the scene can see very clearly at the same time.
xHCI	eXtensible Host Controller Interface	eXtensible Host Controller Interface for Universal Serial Bus.
YNR	Y based Noise Reduction	Filter the noise of Y component

**Difference between RV1109 and RV1126**

Type	RV1109	RV1126
CPU	Dual A7	Quad A7
NPU	1.2Tops	2.0TOPS
ISP	5M up to 3072-pixel wide	14M <=4416*3312
Encoder	5M up to 3072-pixel wide	4K30 H.264/H.265
Decoder	5M up to 3072-pixel wide	4K30 H.264/H.265

## Chapter 1 DMC (Dynamic Memory Interface)

### 1.1 Overview

The DMC includes DDR protocol controller(PCTL) and DDRPHY which are a complete memory interface solution for DDR memory subsystems.

The PCTL SoC application bus interface supports AXI interface, with flexible address mapper logic allow application-specific mapping of row, column, bank, bank group and rank bits to achieve industry leading high-efficiency, low-latency and high-performance from memory interface.

The DDR PHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, write levelling training and programmable configuration controls.

The DMC supports the following features:

- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4
- Support up to 2 ranks and up to 4GB capacity
- Support 32-bit, 16-bit DDR data bus width
- Support up to 16-type address mapping
- Support up to 32-bank (including bank group)
- Support DDR burst8 for DDR3/DDR3L/DDR4/LPDDR3 and burst16 for LPDDR4
- Support different CL/WL latency
- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4SW frequency change
- Support auto gated clock through DDRC and AXI low power interface
- Support auto put DDR PHY entry or exit self-refresh by DFI lower power interface
- Support auto or SW issue entry or exit clock stop/power-down/self-refresh/deep power-down/max power saving mode
- Support SW or PMU auto let DDR PHY entry or exit retention/self-refresh
- Support open, close, intelligent pre-charge paging policy
- Support advance refresh control
- Support APB interface for PCTL and PHY software-accessible registers
- Support automatic RX DQS gate training and automatic write levelling training
- Support DDR monitor for debug:
  - AMBA 32-bit APB slave interface
  - Support to monitor DDR read or write address
  - Support to observe whether DDR access address within a specified range
  - Support to do the statistics about DDR read number, write number and active number
    - ◆ Hardware mode
    - ◆ Software mode
  - Support monitor interrupt

### 1.2 Block Diagram

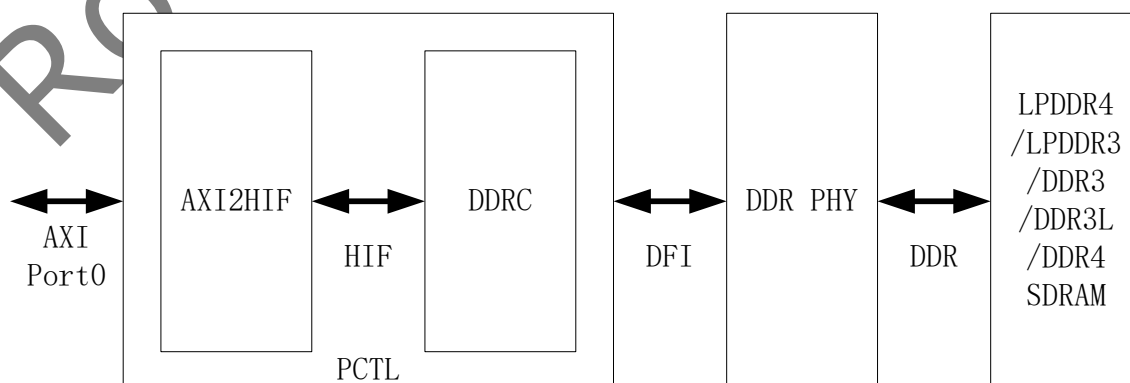


Fig.1-1 DMC Block Diagram

## 1.3 Function Description

### 1.3.1 PCTL

PCTL supports only one AXI Port0, it receives AXI transactions from memory schedule of interconnect. These transactions are queued internally and scheduled for access in order to the SDRAM while satisfying SDRAM protocol timing requirements. It in turn issues commands on the DFI interface to the DDR PHY block which launches and captures data to and from the SDRAM. PCTL contains the following main components:

- AXI2HIF block: This block provides the AXI interface to system level and HIF interface to DDRC block. It provides bus protocol handing, data buffering, data bus size conversion and memory burst alignment. Read is stored in a SRAM, read re-order buffer and return in order to the AXI Port.
- DDRC block: This block issues the read/write commands in order, carries out the DRAM page management, issues DRAM maintenance commands, and implement the DFI interface. Write data is stored in an SRAM until its associated command is issued to the PHY. Read data is handled by the response engine in the DDRC and is returned in order on the HIF.

### 1.3.2 DDR PHY

DDR PHY supports DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM and provides turnkey physical interface solutions for ICs requiring access to JEDEC compatible SDRAM devices. It is optimized for low power and high speed (up to 1866Mbps for DDR3/DDR3L/LPDDR3 and up to 2133Mbps for DDR4/LPDDR4) applications with robust timing and small silicon area in 14nm process. It supports all JEDEC DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM components in the market. The PHY components contain DDR specialized functional and utility SSTL I/Os up to 2133MHz in SMIC 14nm, critical timing synchronization module (TSM) and a low power/jitter DLLs with programmable fine-grain control for any SDRAM interface.

### 1.3.3 DDR Standby

The function of DDR standby module is to set the standby mode of DDR controller, PHY and memory scheduler. The standby mode is enabled by programming DDR standby control register through APB slave interface. When there are not any bus access to DDR data and register, DDR controller will be idle. Once DDR controller is idle for a period of time, the DDR standby module will generate a low power request to DDR controller and also generate appropriate interface logic to gate the clock of DDR controller, DDR PHY and memory scheduler.

### 1.3.4 DDR Monitor

The DDR Monitor Module has three functions, the first function is used when debug, it will monitor the DDR read or write address. The second function is also used when debug, it will observe whether DDR access address within a specified range. The third function is used to do the statistics about DDR bandwidth and utilization.



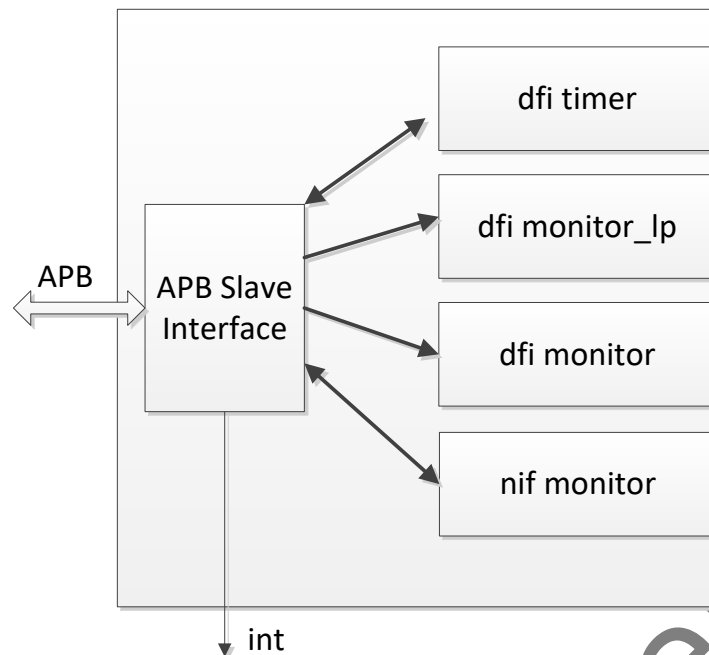


Fig.1-2 DDR Monitor Block Diagram

The host processor gets access to DDR Monitor Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt.

DDR Monitor does the monitor and statistics by dfi monitor module, nif monitor module and dfi monitor\_lp module.

## 1.4 Register Description

Slave address can be divided into different length for different usage, which is shown as follows.

### 1.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
<u>DDRC_MSTR</u>	0x0000	W	0x03040001	Master Register 0
<u>DDRC_STAT</u>	0x0004	W	0x00000000	Operating Mode Status Register
<u>DDRC_MRCTRL0</u>	0x0010	W	0x00000030	Mode Register Read/Write Control Register 0
<u>DDRC_MRCTRL1</u>	0x0014	W	0x00000000	Mode Register Read/Write Control Register 1
<u>DDRC_MRSTAT</u>	0x0018	W	0x00000000	Mode Register Read/Write Status Register
<u>DDRC_MRCTRL2</u>	0x001C	W	0x00000000	Mode Register Read/Write Control Register 2
<u>DDRC_DERATEEN</u>	0x0020	W	0x00000000	Temperature Derate Enable Register
<u>DDRC_DERATEINT</u>	0x0024	W	0x00800000	Temperature Derate Interval Register
<u>DDRC_PWRCTL</u>	0x0030	W	0x00000000	Lower Power Control Register
<u>DDRC_PWRTMG</u>	0x0034	W	0x00402010	Lower Power Timing Register
<u>DDRC_HWLPCTL</u>	0x0038	W	0x00000003	Hardware Lower Power Control Register

Name	Offset	Size	Reset Value	Description
<u>DDRC_HWFFCCTL</u>	0x003C	W	0x00000010	Hardware Fast Frequency Change Control Register
<u>DDRC_HWFFCSTAT</u>	0x0040	W	0x00000000	Hardware Fast Frequency Change Status Register
<u>DDRC_RFSHCTL0</u>	0x0050	W	0x00210000	Refresh Control Register
<u>DDRC_RFSHCTL1</u>	0x0054	W	0x00000000	Refresh Control Register 1
<u>DDRC_RFSHCTL3</u>	0x0060	W	0x00000000	Refresh Control Register 3
<u>DDRC_RFSHTMG</u>	0x0064	W	0x0062008C	Refresh Timing Register
<u>DDRC_CRCPARCTL0</u>	0x00C0	W	0x00000000	CRC Parity Control Register 0
<u>DDRC_CRCPARCTL1</u>	0x00C4	W	0x00001000	CRC Parity Control Register 1
<u>DDRC_CRCPARSTAT</u>	0x00CC	W	0x00000000	CRC Parity Status Register
<u>DDRC_INIT0</u>	0x00D0	W	0x0002004E	SDRAM Initialization Register 0
<u>DDRC_INIT1</u>	0x00D4	W	0x00000000	SDRAM Initialization Register 1
<u>DDRC_INIT2</u>	0x00D8	W	0x00000D05	SDRAM Initialization Register 2
<u>DDRC_INIT3</u>	0x00DC	W	0x00000510	SDRAM Initialization Register 3
<u>DDRC_INIT4</u>	0x00E0	W	0x00000000	SDRAM Initialization Register 4
<u>DDRC_INIT5</u>	0x00E4	W	0x00100004	SDRAM Initialization Register 5
<u>DDRC_INIT6</u>	0x00E8	W	0x00000000	SDRAM Initialization Register 6
<u>DDRC_INIT7</u>	0x00EC	W	0x00000000	SDRAM Initialization Register 7
<u>DDRC_DIMMCTL</u>	0x00F0	W	0x00000000	DIMM Control Register
<u>DDRC_RANKCTL</u>	0x00F4	W	0x0000066F	Rank Control Register
<u>DDRC_DRAMTMG0</u>	0x0100	W	0x0F101B0F	SDRAM Timing Register 0
<u>DDRC_DRAMTMG1</u>	0x0104	W	0x00080414	SDRAM Timing Register 1
<u>DDRC_DRAMTMG2</u>	0x0108	W	0x0305060D	SDRAM Timing Register 2
<u>DDRC_DRAMTMG3</u>	0x010C	W	0x0050400C	SDRAM Timing Register 3
<u>DDRC_DRAMTMG4</u>	0x0110	W	0x05040405	SDRAM Timing Register 4
<u>DDRC_DRAMTMG5</u>	0x0114	W	0x05050403	SDRAM Timing Register 5
<u>DDRC_DRAMTMG6</u>	0x0118	W	0x02020005	SDRAM Timing Register 6
<u>DDRC_DRAMTMG7</u>	0x011C	W	0x00000202	SDRAM Timing Register 7
<u>DDRC_DRAMTMG8</u>	0x0120	W	0x03034405	SDRAM Timing Register 8
<u>DDRC_DRAMTMG9</u>	0x0124	W	0x0004040D	SDRAM Timing Register 9
<u>DDRC_DRAMTMG10</u>	0x0128	W	0x001C180A	SDRAM Timing Register 10
<u>DDRC_DRAMTMG11</u>	0x012C	W	0x440C021C	SDRAM Timing Register 11
<u>DDRC_DRAMTMG12</u>	0x0130	W	0x00020010	SDRAM Timing Register 12
<u>DDRC_DRAMTMG13</u>	0x0134	W	0x1C200004	SDRAM Timing Register 13
<u>DDRC_DRAMTMG14</u>	0x0138	W	0x000000A0	SDRAM Timing Register 14
<u>DDRC_DRAMTMG15</u>	0x013C	W	0x00000000	SDRAM Timing Register 15
<u>DDRC_DRAMTMG17</u>	0x0144	W	0x00000000	SDRAM Timing Register 17
<u>DDRC_ZQCTL0</u>	0x0180	W	0x02000040	ZQ Control Register 0
<u>DDRC_ZQCTL1</u>	0x0184	W	0x02000100	ZQ Control Register 1
<u>DDRC_ZQCTL2</u>	0x0188	W	0x00000000	ZQ Control Register 2
<u>DDRC_ZQSTAT</u>	0x018C	W	0x00000000	ZQ Status Register

Name	Offset	Size	Reset Value	Description
<u>DDRC_DFITMG0</u>	0x0190	W	0x07020002	DFI Timing Register 0
<u>DDRC_DFITMG1</u>	0x0194	W	0x00000404	DFI Timing Register 1
<u>DDRC_DFILPCFG0</u>	0x0198	W	0x07000000	DFI Lower Power Configuration Register 0
<u>DDRC_DFILPCFG1</u>	0x019C	W	0x00000000	DFI Lower Power Configuration Register 1
<u>DDRC_DFIUPD0</u>	0x01A0	W	0x00400003	DFI Update Register 0
<u>DDRC_DFIUPD1</u>	0x01A4	W	0x00010001	DFI Update Register 1
<u>DDRC_DFIUPD2</u>	0x01A8	W	0x80000000	DFI Update Register 2
<u>DDRC_DFIMISC</u>	0x01B0	W	0x00000001	DFI Miscellaneous Control Register
<u>DDRC_DFITMG2</u>	0x01B4	W	0x00000202	DFI Timing Register 2
<u>DDRC_DFITMG3</u>	0x01B8	W	0x00000000	DFI Timing Register 3
<u>DDRC_DFISTAT</u>	0x01BC	W	0x00000000	DFI Status Register
<u>DDRC_DBICTL</u>	0x01C0	W	0x00000001	DM/DBI Control Register
<u>DDRC_DFIPHYMSTR</u>	0x01C4	W	0x00000001	DFI PHY Master
<u>DDRC_ADDRMAP0</u>	0x0200	W	0x00000000	Address Map Register 0
<u>DDRC_ADDRMAP1</u>	0x0204	W	0x00000000	Address Map Register 1
<u>DDRC_ADDRMAP2</u>	0x0208	W	0x00000000	Address Map Register 2
<u>DDRC_ADDRMAP3</u>	0x020C	W	0x00000000	Address Map Register 3
<u>DDRC_ADDRMAP4</u>	0x0210	W	0x00000000	Address Map Register 4
<u>DDRC_ADDRMAP5</u>	0x0214	W	0x00000000	Address Map Register 5
<u>DDRC_ADDRMAP6</u>	0x0218	W	0x00000000	Address Map Register 6
<u>DDRC_ADDRMAP7</u>	0x021C	W	0x00000000	Address Map Register 7
<u>DDRC_ADDRMAP8</u>	0x0220	W	0x00000000	Address Map Register 8
<u>DDRC_ADDRMAP9</u>	0x0224	W	0x00000000	Address Map Register 9
<u>DDRC_ADDRMAP10</u>	0x0228	W	0x00000000	Address Map Register 10
<u>DDRC_ADDRMAP11</u>	0x022C	W	0x00000000	Address Map Register 11
<u>DDRC_ODTCFG</u>	0x0240	W	0x04000400	ODT Configuration Register
<u>DDRC_ODTMAP</u>	0x0244	W	0x00002211	ODT/Rank Map Register
<u>DDRC_SCHED</u>	0x0250	W	0x00001004	Scheduler Control Register
<u>DDRC_SCHED1</u>	0x0254	W	0x00000000	Scheduler Control Register 1
<u>DDRC_PERFLPR1</u>	0x0264	W	0x0F00007F	Low Priority Read CAM Register 1
<u>DDRC_PERFWR1</u>	0x026C	W	0x0F00007F	Write CAM Register 1
<u>DDRC_DBG0</u>	0x0300	W	0x00000000	Debug Register 0
<u>DDRC_DBG1</u>	0x0304	W	0x00000000	Debug Register 1
<u>DDRC_DBGCAM</u>	0x0308	W	0x36000000	CAM Debug Register
<u>DDRC_DBGCMD</u>	0x030C	W	0x00000000	Command Debug Register
<u>DDRC_DBGSTAT</u>	0x0310	W	0x00000000	Status Debug Register
<u>DDRC_SWCTL</u>	0x0320	W	0x00000001	Software Register Programming Control Enable
<u>DDRC_SWSTAT</u>	0x0324	W	0x00000001	Software Register Programming Control Status

Name	Offset	Size	Reset Value	Description
<u>DDRC_POISONCFG</u>	0x036C	W	0x00110011	AXI Poison Configuration Register
<u>DDRC_POISONSTAT</u>	0x0370	W	0x00000000	AXI Poison Status Register
<u>DDRC_PSTAT</u>	0x03FC	W	0x00000000	Port Status Register
<u>DDRC_PCCFG</u>	0x0400	W	0x00000000	Port Common Configuration Register
<u>DDRC_PCFGR_0</u>	0x0404	W	0x00000000	Port 0 Configuration Read Register
<u>DDRC_PCFGW_0</u>	0x0408	W	0x00004000	Port 0 Configuration Write Register
<u>DDRC_PCTRL_0</u>	0x0490	W	0x00000000	Port 0 Control Register

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG0</u>	0x0000	W	0x0000000F	DDR PHY Register 00
<u>DDRPHY_REG1</u>	0x0004	W	0x00000088	DDR PHY Register 01
<u>DDRPHY_REG2</u>	0x0008	W	0x000000A0	DDR PHY Register 02
<u>DDRPHY_REG3</u>	0x000C	W	0x00000000	DDR PHY Register 03
<u>DDRPHY_REG4</u>	0x0010	W	0x00000000	DDR PHY Register 04
<u>DDRPHY_REG5</u>	0x0014	W	0x00000006	DDR PHY Register 05
<u>DDRPHY_REG6</u>	0x0018	W	0x00000000	DDR PHY Register 06
<u>DDRPHY_REGC</u>	0x0030	W	0x00000000	DDR PHY Register 0C
<u>DDRPHY_REGE</u>	0x0038	W	0x00000023	DDR PHY Register 0E
<u>DDRPHY_REGF</u>	0x003C	W	0x0000002F	DDR PHY Register 0F
<u>DDRPHY_REG10</u>	0x0040	W	0x00000000	DDR PHY Register 10
<u>DDRPHY_REG11</u>	0x0044	W	0x000000FC	DDR PHY Register 11
<u>DDRPHY_REG12</u>	0x0048	W	0x00000028	DDR PHY Register 12
<u>DDRPHY_REG13</u>	0x004C	W	0x0000000F	DDR PHY Register 13
<u>DDRPHY_REG14</u>	0x0050	W	0x00000041	DDR PHY Register 14
<u>DDRPHY_REG15</u>	0x0054	W	0x000000F4	DDR PHY Register 15
<u>DDRPHY_REG16</u>	0x0058	W	0x0000001F	DDR PHY Register 16
<u>DDRPHY_REG17</u>	0x005C	W	0x00000000	DDR PHY Register 17
<u>DDRPHY_REG18</u>	0x0060	W	0x00000000	DDR PHY Register 18
<u>DDRPHY_REG19</u>	0x0064	W	0x00000000	DDR PHY Register 19
<u>DDRPHY_REG1A</u>	0x0068	W	0x00000000	DDR PHY Register 1A
<u>DDRPHY_REG1B</u>	0x006C	W	0x00000000	DDR PHY Register 1B
<u>DDRPHY_REG1C</u>	0x0070	W	0x00000000	DDR PHY Register 1C
<u>DDRPHY_REG1D</u>	0x0074	W	0x00000000	DDR PHY Register 1D
<u>DDRPHY_REG1E</u>	0x0078	W	0x0000001F	DDR PHY Register 1E
<u>DDRPHY_REG1F</u>	0x007C	W	0x0000001F	DDR PHY Register 1F
<u>DDRPHY_REG20</u>	0x0080	W	0x00000002	DDR PHY Register 20
<u>DDRPHY_REG21</u>	0x0084	W	0x000000C6	DDR PHY Register 21
<u>DDRPHY_REG22</u>	0x0088	W	0x00000015	DDR PHY Register 22
<u>DDRPHY_REG23</u>	0x008C	W	0x0000003F	DDR PHY Register 23

Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG24</u>	0x0090	W	0x0000003F	DDR PHY Register 24
<u>DDRPHY_REG25</u>	0x0094	W	0x00000003	DDR PHY Register 25
<u>DDRPHY_REG29</u>	0x00A4	W	0x00000020	DDR PHY Register 29
<u>DDRPHY_REG2A</u>	0x00A8	W	0x00000000	DDR PHY Register 2A
<u>DDRPHY_REG2B</u>	0x00AC	W	0x00000091	DDR PHY Register 2B
<u>DDRPHY_REG2D</u>	0x00B4	W	0x00000040	DDR PHY Register 2D
<u>DDRPHY_REG2E</u>	0x00B8	W	0x00000000	DDR PHY Register 2E
<u>DDRPHY_REG2F</u>	0x00BC	W	0x00000010	DDR PHY Register 2F
<u>DDRPHY_REG30</u>	0x00C0	W	0x00000000	DDR PHY Register 30
<u>DDRPHY_REG31</u>	0x00C4	W	0x00000001	DDR PHY Register 31
<u>DDRPHY_REG32</u>	0x00C8	W	0x00000002	DDR PHY Register 32
<u>DDRPHY_REG33</u>	0x00CC	W	0x00000003	DDR PHY Register 33
<u>DDRPHY_REG34</u>	0x00D0	W	0x00000004	DDR PHY Register 34
<u>DDRPHY_REG35</u>	0x00D4	W	0x00000005	DDR PHY Register 35
<u>DDRPHY_REG36</u>	0x00D8	W	0x00000006	DDR PHY Register 36
<u>DDRPHY_REG37</u>	0x00DC	W	0x00000007	DDR PHY Register 37
<u>DDRPHY_REG38</u>	0x00E0	W	0x00000008	DDR PHY Register 38
<u>DDRPHY_REG39</u>	0x00E4	W	0x00000009	DDR PHY Register 39
<u>DDRPHY_REG3A</u>	0x00E8	W	0x0000000A	DDR PHY Register 3A
<u>DDRPHY_REG3B</u>	0x00EC	W	0x0000000B	DDR PHY Register 3B
<u>DDRPHY_REG3C</u>	0x00F0	W	0x0000000C	DDR PHY Register 3C
<u>DDRPHY_REG3D</u>	0x00F4	W	0x0000000D	DDR PHY Register 3D
<u>DDRPHY_REG3E</u>	0x00F8	W	0x0000000E	DDR PHY Register 3E
<u>DDRPHY_REG3F</u>	0x00FC	W	0x0000000F	DDR PHY Register 3F
<u>DDRPHY_REG40</u>	0x0100	W	0x00000010	DDR PHY Register 40
<u>DDRPHY_REG41</u>	0x0104	W	0x00000011	DDR PHY Register 41
<u>DDRPHY_REG42</u>	0x0108	W	0x00000012	DDR PHY Register 42
<u>DDRPHY_REG43</u>	0x010C	W	0x00000013	DDR PHY Register 43
<u>DDRPHY_REG44</u>	0x0110	W	0x00000014	DDR PHY Register 44
<u>DDRPHY_REG45</u>	0x0114	W	0x00000015	DDR PHY Register 45
<u>DDRPHY_REG46</u>	0x0118	W	0x00000016	DDR PHY Register 46
<u>DDRPHY_REG47</u>	0x011C	W	0x00000017	DDR PHY Register 47
<u>DDRPHY_REG48</u>	0x0120	W	0x00000018	DDR PHY Register 48
<u>DDRPHY_REG49</u>	0x0124	W	0x00000019	DDR PHY Register 49
<u>DDRPHY_REG4A</u>	0x0128	W	0x0000001A	DDR PHY Register 4A
<u>DDRPHY_REG4B</u>	0x012C	W	0x0000001B	DDR PHY Register 4B
<u>DDRPHY_REG4C</u>	0x0130	W	0x0000001C	DDR PHY Register 4C
<u>DDRPHY_REG4D</u>	0x0134	W	0x0000001D	DDR PHY Register 4D
<u>DDRPHY_REG4E</u>	0x0138	W	0x0000001E	DDR PHY Register 4E
<u>DDRPHY_REG4F</u>	0x013C	W	0x000000E4	DDR PHY Register 4F
<u>DDRPHY_REG50</u>	0x0140	W	0x00000000	DDR PHY Register 50
<u>DDRPHY_REG51</u>	0x0144	W	0x00000006	DDR PHY Register 51

Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG52</u>	0x0148	W	0x00000041	DDR PHY Register 52
<u>DDRPHY_REG53</u>	0x014C	W	0x00000008	DDR PHY Register 53
<u>DDRPHY_REG57</u>	0x015C	W	0x0000008C	DDR PHY Register 57
<u>DDRPHY_REG60</u>	0x0180	W	0x00000051	DDR PHY Register 60
<u>DDRPHY_REG61</u>	0x0184	W	0x00000089	DDR PHY Register 61
<u>DDRPHY_REG62</u>	0x0188	W	0x0000007F	DDR PHY Register 62
<u>DDRPHY_REG63</u>	0x018C	W	0x00000088	DDR PHY Register 63
<u>DDRPHY_REG64</u>	0x0190	W	0x00000013	DDR PHY Register 64
<u>DDRPHY_REG65</u>	0x0194	W	0x00000016	DDR PHY Register 65
<u>DDRPHY_REG66</u>	0x0198	W	0x00000001	DDR PHY Register 66
<u>DDRPHY_REG67</u>	0x019C	W	0x0000000E	DDR PHY Register 67
<u>DDRPHY_REG68</u>	0x01A0	W	0x0000000E	DDR PHY Register 68
<u>DDRPHY_REG69</u>	0x01A4	W	0x00000007	DDR PHY Register 69
<u>DDRPHY_REG6A</u>	0x01A8	W	0x00000007	DDR PHY Register 6A
<u>DDRPHY_REG6B</u>	0x01AC	W	0x000000FF	DDR PHY Register 6B
<u>DDRPHY_REG6C</u>	0x01B0	W	0x000000FF	DDR PHY Register 6C
<u>DDRPHY_REG6D</u>	0x01B4	W	0x00000000	DDR PHY Register 6D
<u>DDRPHY_REG6E</u>	0x01B8	W	0x00000060	DDR PHY Register 6E
<u>DDRPHY_REG6F</u>	0x01BC	W	0x00000009	DDR PHY Register 6F
<u>DDRPHY_REG70</u>	0x01C0	W	0x00000000	DDR PHY Register 70
<u>DDRPHY_REG71</u>	0x01C4	W	0x00000008	DDR PHY Register 71
<u>DDRPHY_REG72</u>	0x01C8	W	0x00000055	DDR PHY Register 72
<u>DDRPHY_REG73</u>	0x01CC	W	0x00000055	DDR PHY Register 73
<u>DDRPHY_REG74</u>	0x01D0	W	0x0000005A	DDR PHY Register 74
<u>DDRPHY_REG75</u>	0x01D4	W	0x0000003C	DDR PHY Register 75
<u>DDRPHY_REG76</u>	0x01D8	W	0x00000006	DDR PHY Register 76
<u>DDRPHY_REG77</u>	0x01DC	W	0x00000006	DDR PHY Register 77
<u>DDRPHY_REG78</u>	0x01E0	W	0x00000015	DDR PHY Register 78
<u>DDRPHY_REG79</u>	0x01E4	W	0x00000015	DDR PHY Register 79
<u>DDRPHY_REG7A</u>	0x01E8	W	0x00000000	DDR PHY Register 7A
<u>DDRPHY_REG7B</u>	0x01EC	W	0x00000000	DDR PHY Register 7B
<u>DDRPHY_REG7C</u>	0x01F0	W	0x00000020	DDR PHY Register 7C
<u>DDRPHY_REG7D</u>	0x01F4	W	0x00000001	DDR PHY Register 7D
<u>DDRPHY_REG7E</u>	0x01F8	W	0x00000000	DDR PHY Register 7E
<u>DDRPHY_REG90</u>	0x0240	W	0x00000012	DDR PHY Register 90
<u>DDRPHY_REG91</u>	0x0244	W	0x00000000	DDR PHY Register 91
<u>DDRPHY_REG92</u>	0x0248	W	0x00000000	DDR PHY Register 92
<u>DDRPHY_REG93</u>	0x024C	W	0x00000000	DDR PHY Register 93
<u>DDRPHY_REG94</u>	0x0250	W	0x00000000	DDR PHY Register 94
<u>DDRPHY_REG95</u>	0x0254	W	0x00000000	DDR PHY Register 95
<u>DDRPHY_REG96</u>	0x0258	W	0x00000000	DDR PHY Register 96
<u>DDRPHY_REG97</u>	0x025C	W	0x00000000	DDR PHY Register 97

Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG98</u>	0x0260	W	0x00000000	DDR PHY Register 98
<u>DDRPHY_REG99</u>	0x0264	W	0x00000000	DDR PHY Register 99
<u>DDRPHY_REG9A</u>	0x0268	W	0x00000000	DDR PHY Register 9A
<u>DDRPHY_REG9B</u>	0x026C	W	0x00000000	DDR PHY Register 9B
<u>DDRPHY_REG105</u>	0x0414	W	0x00000080	DDR PHY Register 105
<u>DDRPHY_REG118</u>	0x0460	W	0x00000000	DDR PHY Register 118
<u>DDRPHY_REG128</u>	0x04A0	W	0x00000080	DDR PHY Register 128
<u>DDRPHY_REG138</u>	0x04E0	W	0x00000000	DDR PHY Register 138
<u>DDRPHY_REG148</u>	0x0520	W	0x00000080	DDR PHY Register 148
<u>DDRPHY_REG150</u>	0x0540	W	0x00000007	DDR PHY Register 150
<u>DDRPHY_REG151</u>	0x0544	W	0x00000007	DDR PHY Register 151
<u>DDRPHY_REG152</u>	0x0548	W	0x00000007	DDR PHY Register 152
<u>DDRPHY_REG153</u>	0x054C	W	0x00000007	DDR PHY Register 153
<u>DDRPHY_REG154</u>	0x0550	W	0x00000007	DDR PHY Register 154
<u>DDRPHY_REG155</u>	0x0554	W	0x00000007	DDR PHY Register 155
<u>DDRPHY_REG156</u>	0x0558	W	0x00000007	DDR PHY Register 156
<u>DDRPHY_REG157</u>	0x055C	W	0x00000007	DDR PHY Register 157
<u>DDRPHY_REG158</u>	0x0560	W	0x00000007	DDR PHY Register 158
<u>DDRPHY_REG159</u>	0x0564	W	0x00000007	DDR PHY Register 159
<u>DDRPHY_REG15A</u>	0x0568	W	0x00000007	DDR PHY Register 15A
<u>DDRPHY_REG15B</u>	0x056C	W	0x00000007	DDR PHY Register 15B
<u>DDRPHY_REG15C</u>	0x0570	W	0x00000007	DDR PHY Register 15C
<u>DDRPHY_REG15D</u>	0x0574	W	0x00000007	DDR PHY Register 15D
<u>DDRPHY_REG15E</u>	0x0578	W	0x00000007	DDR PHY Register 15E
<u>DDRPHY_REG15F</u>	0x057C	W	0x00000007	DDR PHY Register 15F
<u>DDRPHY_REG160</u>	0x0580	W	0x00000007	DDR PHY Register 160
<u>DDRPHY_REG161</u>	0x0584	W	0x00000007	DDR PHY Register 161
<u>DDRPHY_REG162</u>	0x0588	W	0x00000007	DDR PHY Register 162
<u>DDRPHY_REG163</u>	0x058C	W	0x00000007	DDR PHY Register 163
<u>DDRPHY_REG164</u>	0x0590	W	0x00000007	DDR PHY Register 164
<u>DDRPHY_REG165</u>	0x0594	W	0x00000007	DDR PHY Register 165
<u>DDRPHY_REG166</u>	0x0598	W	0x00000007	DDR PHY Register 166
<u>DDRPHY_REG167</u>	0x059C	W	0x00000007	DDR PHY Register 167
<u>DDRPHY_REG168</u>	0x05A0	W	0x00000007	DDR PHY Register 168
<u>DDRPHY_REG169</u>	0x05A4	W	0x00000007	DDR PHY Register 169
<u>DDRPHY_REG16A</u>	0x05A8	W	0x00000007	DDR PHY Register 16A
<u>DDRPHY_REG16B</u>	0x05AC	W	0x00000007	DDR PHY Register 16B
<u>DDRPHY_REG16C</u>	0x05B0	W	0x00000007	DDR PHY Register 16C
<u>DDRPHY_REG16D</u>	0x05B4	W	0x00000007	DDR PHY Register 16D
<u>DDRPHY_REG16E</u>	0x05B8	W	0x00000007	DDR PHY Register 16E
<u>DDRPHY_REG16F</u>	0x05BC	W	0x00000007	DDR PHY Register 16F
<u>DDRPHY_REG230</u>	0x08C0	W	0x0000001F	DDR PHY Register 230

Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG231</u>	0x08C4	W	0x0000003F	DDR PHY Register 231
<u>DDRPHY_REG232</u>	0x08C8	W	0x00000000	DDR PHY Register 232
<u>DDRPHY_REG235</u>	0x08D4	W	0x0000003F	DDR PHY Register 235
<u>DDRPHY_REG236</u>	0x08D8	W	0x00000000	DDR PHY Register 236
<u>DDRPHY_REG23C</u>	0x08F0	W	0x00000000	DDR PHY Register 23C
<u>DDRPHY_REG240</u>	0x0900	W	0x00000000	DDR PHY Register 240
<u>DDRPHY_REG2B0</u>	0x0AC0	W	0x0000001F	DDR PHY Register 2B0
<u>DDRPHY_REG2B1</u>	0x0AC4	W	0x0000003F	DDR PHY Register 2B1
<u>DDRPHY_REG2B2</u>	0x0AC8	W	0x00000000	DDR PHY Register 2B2
<u>DDRPHY_REG2B5</u>	0x0AD4	W	0x0000003F	DDR PHY Register 2B5
<u>DDRPHY_REG2B6</u>	0x0AD8	W	0x00000000	DDR PHY Register 2B6
<u>DDRPHY_REG330</u>	0x0CC0	W	0x0000005A	DDR PHY Register 330
<u>DDRPHY_REG331</u>	0x0CC4	W	0x000000A5	DDR PHY Register 331
<u>DDRPHY_REG332</u>	0x0CC8	W	0x000000C3	DDR PHY Register 332
<u>DDRPHY_REG333</u>	0x0CCC	W	0x0000003C	DDR PHY Register 333
<u>DDRPHY_REG33A</u>	0x0CE8	W	0x000000A5	DDR PHY Register 33A
<u>DDRPHY_REG33B</u>	0x0CEC	W	0x0000005A	DDR PHY Register 33B
<u>DDRPHY_REG33C</u>	0x0CF0	W	0x0000003C	DDR PHY Register 33C
<u>DDRPHY_REG33D</u>	0x0CF4	W	0x000000C3	DDR PHY Register 33D
<u>DDRPHY_REG344</u>	0x0D10	W	0x0000005A	DDR PHY Register 344
<u>DDRPHY_REG345</u>	0x0D14	W	0x000000A5	DDR PHY Register 345
<u>DDRPHY_REG346</u>	0x0D18	W	0x000000C3	DDR PHY Register 346
<u>DDRPHY_REG347</u>	0x0D1C	W	0x0000003C	DDR PHY Register 347
<u>DDRPHY_REG34E</u>	0x0D38	W	0x000000A5	DDR PHY Register 34E
<u>DDRPHY_REG34F</u>	0x0D3C	W	0x0000005A	DDR PHY Register 34F
<u>DDRPHY_REG350</u>	0x0D40	W	0x0000003C	DDR PHY Register 350
<u>DDRPHY_REG351</u>	0x0D44	W	0x000000C3	DDR PHY Register 351
<u>DDRPHY_REG358</u>	0x0D60	W	0x0000005A	DDR PHY Register 358
<u>DDRPHY_REG359</u>	0x0D64	W	0x000000A5	DDR PHY Register 359
<u>DDRPHY_REG35A</u>	0x0D68	W	0x000000C3	DDR PHY Register 35A
<u>DDRPHY_REG35B</u>	0x0D6C	W	0x0000003C	DDR PHY Register 35B
<u>DDRPHY_REG362</u>	0x0D88	W	0x000000A5	DDR PHY Register 362
<u>DDRPHY_REG363</u>	0x0D8C	W	0x0000005A	DDR PHY Register 363
<u>DDRPHY_REG364</u>	0x0D90	W	0x0000003C	DDR PHY Register 364
<u>DDRPHY_REG365</u>	0x0D94	W	0x000000C3	DDR PHY Register 365
<u>DDRPHY_REG36C</u>	0x0DB0	W	0x0000005A	DDR PHY Register 36C
<u>DDRPHY_REG36D</u>	0x0DB4	W	0x000000A5	DDR PHY Register 36D
<u>DDRPHY_REG36E</u>	0x0DB8	W	0x000000C3	DDR PHY Register 36E
<u>DDRPHY_REG36F</u>	0x0DBC	W	0x0000003C	DDR PHY Register 36F
<u>DDRPHY_REG376</u>	0x0DD8	W	0x000000A5	DDR PHY Register 376
<u>DDRPHY_REG377</u>	0x0DDC	W	0x0000005A	DDR PHY Register 377
<u>DDRPHY_REG378</u>	0x0DE0	W	0x0000003C	DDR PHY Register 378



Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG379</u>	0x0DE4	W	0x000000C3	DDR PHY Register 379
<u>DDRPHY_REG380</u>	0x0E00	W	0x00000040	DDR PHY Register 380
<u>DDRPHY_REG381</u>	0x0E04	W	0x00000041	DDR PHY Register 381
<u>DDRPHY_REG382</u>	0x0E08	W	0x00000021	DDR PHY Register 382
<u>DDRPHY_REG387</u>	0x0E1C	W	0x00000006	DDR PHY Register 387
<u>DDRPHY_REG388</u>	0x0E20	W	0x00000000	DDR PHY Register 388
<u>DDRPHY_REG389</u>	0x0E24	W	0x00000000	DDR PHY Register 389
<u>DDRPHY_REG38A</u>	0x0E28	W	0x00000006	DDR PHY Register 38A
<u>DDRPHY_REG38B</u>	0x0E2C	W	0x00000000	DDR PHY Register 38B
<u>DDRPHY_REG38C</u>	0x0E30	W	0x00000000	DDR PHY Register 38C
<u>DDRPHY_REG38D</u>	0x0E34	W	0x00000006	DDR PHY Register 38D
<u>DDRPHY_REG38E</u>	0x0E38	W	0x00000000	DDR PHY Register 38E
<u>DDRPHY_REG38F</u>	0x0E3C	W	0x00000000	DDR PHY Register 38F
<u>DDRPHY_REG3A0</u>	0x0E80	W	0x00000000	DDR PHY Register 3A0
<u>DDRPHY_REG3A1</u>	0x0E84	W	0x00000000	DDR PHY Register 3A1
<u>DDRPHY_REG3A2</u>	0x0E88	W	0x00000000	DDR PHY Register 3A2
<u>DDRPHY_REG3A3</u>	0x0E8C	W	0x00000000	DDR PHY Register 3A3
<u>DDRPHY_REG3A4</u>	0x0E90	W	0x00000000	DDR PHY Register 3A4
<u>DDRPHY_REG3A5</u>	0x0E94	W	0x00000000	DDR PHY Register 3A5
<u>DDRPHY_REG3A6</u>	0x0E98	W	0x00000000	DDR PHY Register 3A6
<u>DDRPHY_REG3A7</u>	0x0E9C	W	0x00000000	DDR PHY Register 3A7
<u>DDRPHY_REG3A8</u>	0x0EA0	W	0x00000000	DDR PHY Register 3A8
<u>DDRPHY_REG3A9</u>	0x0EA4	W	0x00000000	DDR PHY Register 3A9
<u>DDRPHY_REG3AA</u>	0x0EA8	W	0x00000000	DDR PHY Register 3AA
<u>DDRPHY_REG3AB</u>	0x0EAC	W	0x00000000	DDR PHY Register 3AB
<u>DDRPHY_REG3AC</u>	0x0EB0	W	0x00000000	DDR PHY Register 3AC
<u>DDRPHY_REG3AD</u>	0x0EB4	W	0x00000000	DDR PHY Register 3AD
<u>DDRPHY_REG3AE</u>	0x0EB8	W	0x00000000	DDR PHY Register 3AE
<u>DDRPHY_REG3AF</u>	0x0EBC	W	0x00000000	DDR PHY Register 3AF
<u>DDRPHY_REG3B0</u>	0x0EC0	W	0x00000000	DDR PHY Register 3B0
<u>DDRPHY_REG3B1</u>	0x0EC4	W	0x00000000	DDR PHY Register 3B1
<u>DDRPHY_REG3B2</u>	0x0EC8	W	0x00000000	DDR PHY Register 3B2
<u>DDRPHY_REG3B3</u>	0x0ECC	W	0x00000000	DDR PHY Register 3B3
<u>DDRPHY_REG3B4</u>	0x0ED0	W	0x00000000	DDR PHY Register 3B4
<u>DDRPHY_REG3B5</u>	0x0ED4	W	0x00000000	DDR PHY Register 3B5
<u>DDRPHY_REG3B6</u>	0x0ED8	W	0x00000000	DDR PHY Register 3B6
<u>DDRPHY_REG3B7</u>	0x0EDC	W	0x00000000	DDR PHY Register 3B7
<u>DDRPHY_REG3B8</u>	0x0EE0	W	0x00000000	DDR PHY Register 3B8
<u>DDRPHY_REG3B9</u>	0x0EE4	W	0x00000000	DDR PHY Register 3B9
<u>DDRPHY_REG3BA</u>	0x0EE8	W	0x00000000	DDR PHY Register 3BA
<u>DDRPHY_REG3BB</u>	0x0EEC	W	0x00000000	DDR PHY Register 3BB
<u>DDRPHY_REG3BC</u>	0x0EF0	W	0x00000000	DDR PHY Register 3BC

Name	Offset	Size	Reset Value	Description
<u>DDRPHY_REG3BD</u>	0x0EF4	W	0x00000000	DDR PHY Register 3BD
<u>DDRPHY_REG3BE</u>	0x0EF8	W	0x00000000	DDR PHY Register 3BE
<u>DDRPHY_REG3BF</u>	0x0EFC	W	0x00000000	DDR PHY Register 3BF
<u>DDRPHY_REG3C0</u>	0x0F00	W	0x00000000	DDR PHY Register 3C0
<u>DDRPHY_REG3C1</u>	0x0F04	W	0x00000000	DDR PHY Register 3C1
<u>DDRPHY_REG3C2</u>	0x0F08	W	0x00000000	DDR PHY Register 3C2
<u>DDRPHY_REG3C3</u>	0x0F0C	W	0x00000000	DDR PHY Register 3C3
<u>DDRPHY_REG3C4</u>	0x0F10	W	0x00000000	DDR PHY Register 3C4
<u>DDRPHY_REG3C5</u>	0x0F14	W	0x00000000	DDR PHY Register 3C5
<u>DDRPHY_REG3C6</u>	0x0F18	W	0x00000000	DDR PHY Register 3C6
<u>DDRPHY_REG3C7</u>	0x0F1C	W	0x00000000	DDR PHY Register 3C7
<u>DDRPHY_REG3C8</u>	0x0F20	W	0x00000000	DDR PHY Register 3C8
<u>DDRPHY_REG3C9</u>	0x0F24	W	0x00000000	DDR PHY Register 3C9
<u>DDRPHY_REG3CA</u>	0x0F28	W	0x00000000	DDR PHY Register 3CA
<u>DDRPHY_REG3CB</u>	0x0F2C	W	0x00000000	DDR PHY Register 3CB
<u>DDRPHY_REG3CC</u>	0x0F30	W	0x00000000	DDR PHY Register 3CC
<u>DDRPHY_REG3CD</u>	0x0F34	W	0x00000000	DDR PHY Register 3CD
<u>DDRPHY_REG3CE</u>	0x0F38	W	0x00000000	DDR PHY Register 3CE
<u>DDRPHY_REG3CF</u>	0x0F3C	W	0x00000000	DDR PHY Register 3CF
<u>DDRPHY_REG3D0</u>	0x0F40	W	0x00000000	DDR PHY Register 3D0
<u>DDRPHY_REG3D1</u>	0x0F44	W	0x00000000	DDR PHY Register 3D1
<u>DDRPHY_REG3D2</u>	0x0F48	W	0x00000000	DDR PHY Register 3D2
<u>DDRPHY_REG3D3</u>	0x0F4C	W	0x00000000	DDR PHY Register 3D3
<u>DDRPHY_REG3D4</u>	0x0F50	W	0x00000000	DDR PHY Register 3D4
<u>DDRPHY_REG3D5</u>	0x0F54	W	0x00000000	DDR PHY Register 3D5
<u>DDRPHY_REG3D6</u>	0x0F58	W	0x00000000	DDR PHY Register 3D6
<u>DDRPHY_REG3D7</u>	0x0F5C	W	0x00000000	DDR PHY Register 3D7
<u>DDRPHY_REG3D8</u>	0x0F60	W	0x00000000	DDR PHY Register 3D8
<u>DDRPHY_REG3D9</u>	0x0F64	W	0x00000000	DDR PHY Register 3D9
<u>DDRPHY_REG3DA</u>	0x0F68	W	0x00000000	DDR PHY Register 3DA
<u>DDRPHY_REG3DB</u>	0x0F6C	W	0x00000000	DDR PHY Register 3DB
<u>DDRPHY_REG3DC</u>	0x0F70	W	0x00000000	DDR PHY Register 3DC
<u>DDRPHY_REG3DD</u>	0x0F74	W	0x00000000	DDR PHY Register 3DD
<u>DDRPHY_REG3DE</u>	0x0F78	W	0x00000000	DDR PHY Register 3DE
<u>DDRPHY_REG3DF</u>	0x0F7C	W	0x00000000	DDR PHY Register 3DF
<u>DDRPHY_REG3E0</u>	0x0F80	W	0x00000007	DDR PHY Register 3E0

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 1.4.2 Detail Register Description

#### **DDRC\_MSTR**

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	device_config Configuration of device used 2'b00: x4 device 2'b01: x8 device 2'b10: x16 device 2'b11: x32 device Programming Mode: Static
29	RW	0x0	frequency_mode Choose which register are used. 1'b0: Original registers 1'b1: FREQ1 registers Programming Mode: Quasi-dynamic Group 2
28:26	RO	0x0	reserved
25:24	RW	0x3	active_ranks 2'b01: One Rank 2'b11: Two Ranks Others: Reserved Programming Mode: Static
23	RO	0x0	reserved
22	RW	0x0	frequency_ratio selects the frequency ratio 1'b0: 1:2 mode 1'b1: 1:1 mode Programming Mode: Static
21:20	RW	0x0	active_logical_ranks Number of logical ranks for DDR4 3DS 2'b00: Monolithic (no stack) 2'b01: 2H stack 2'b10: 4H stack 2'b11: 8H stack Programming Mode: Static
19:16	RW	0x4	burst_rdwr SDRAM burst length used: 4'b0001: Burst length of 2 4'b0010: Burst length of 4 4'b0100: Burst length of 8 4'b1000: Burst length of 16 Programming Mode: Static
15	RW	0x0	dll_off_mode 1'b1: Dll-off mode for lower frequency operation 1'b0: Dll-on mode for normal frequency operation Programming Mode: Quasi-dynamic Group 2
14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	data_bus_width 2'b00: Full DQ bus width to SDRAM 2'b01: Half DQ bus width to SDRAM Others: Reserved Programming Mode: Static
11	RW	0x0	geardown_mode 1'b1: Enable geardown mode 1'b0: Normal mode Programming Mode: Quasi-dynamic Group 2
10	RW	0x0	en_2t_timing_mode 1'b1: Use 2T timing 1'b0: Use 1T timing Programming Mode: Static
9	RW	0x0	burstchop 1'b1: Enable burst-chop 1'b0: Disable burst-chop Programming Mode: Static
8	RW	0x0	burst_mode 1'b0: Sequential burst mode 1'b1: Interleaved burst mode Programming Mode: Static
7:6	RO	0x0	reserved
5	RW	0x0	lpddr4 1'b1: LPDDR4 1'b0: Non-LPDDR4 Programming Mode: Static
4	RW	0x0	ddr4 1'b1: DDR4 1'b0: Non-DDR4 Programming Mode: Static
3	RW	0x0	lpddr3 1'b1: LPDDR3 1'b0: Non-LPDDR3 Programming Mode: Static
2:1	RO	0x0	reserved
0	RW	0x1	ddr3 1'b1: DDR3 1'b0: Non-DDR3 Programming Mode: Static

**DDRC\_STAT**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12	RO	0x0	selfref_cam_not_empty Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh. Programming Mode: Dynamic
11:10	RO	0x0	reserved
9:8	RO	0x0	selfref_state Self refresh state. This indicates self refresh or self refresh power down state for LPDDR4. This register is used for frequency change and MRR/MRW access during self refresh. 2'b00: SDRAM is not in Self Refresh. 2'b01: Self refresh 1 2'b10: Self refresh power down 2'b11: Self refresh 2 Programming Mode: Dynamic
7:6	RO	0x0	reserved
5:4	RO	0x0	selfref_type Flags if Self Refresh (except LPDDR4) or SR-Powerdown (LPDDR4) is entered and if it was under Automatic Self Refresh control only or not. 2'b00: SDRAM is not in Self Refresh (except LPDDR4) or SR-Powerdown (LPDDR4). If retry is enabled by CRCPARCTRL1.crc_parity_retry_enable, this also indicates SRE command is still in parity error window or retry is in-progress. 2'b11: SDRAM is in Self Refresh (except LPDDR4) or SRPowerdown (LPDDR4), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 2'b10: SDRAM is in Self Refresh (except LPDDR4) or SRPowerdown (LPDDR4), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. 2'b01: SDRAM is in Self Refresh, which was caused by PHY Master Request. Programming Mode: Dynamic
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x0	<p>operating_mode</p> <p>Operating mode. This is 3-bits wide in configurations with LPDDR3/LPDDR4/DDR4 support and 2-bits in all other configurations.</p> <p>LPDDR3/LPDDR4 and non-DDR4 designs:</p> <p>2'b00: Init</p> <p>2'b01: Normal</p> <p>2'b10: Power-down</p> <p>2'b11: Self refresh</p> <p>LPDDR3 or DDR4 designs:</p> <p>3'b000: Init</p> <p>3'b001: Normal</p> <p>3'b010: Power-down</p> <p>3'b011: Self refresh</p> <p>3'b1xx: Deep power-down/Maximum Power Saving Mode</p> <p>LPDDR4 designs:</p> <p>3'b000: Init</p> <p>3'b001: Normal</p> <p>3'b010: Power-down</p> <p>3'b011: Self refresh/Self refresh power-down</p> <p>Programming Mode: Dynamic</p>

**DDRC\_MRCTRL0**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	<p>mr_wr</p> <p>Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the uMCTL2 automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes.</p> <p>Programming Mode: Dynamic</p>
30	RW	0x0	<p>pba_mode</p> <p>Indicates whether PBA access is executed. When setting this bit to 1 along with setting pda_en to 1, uMCTL2 initiates PBA access instead of PDA access.</p> <p>1'b0: Per DRAM Addressability mode</p> <p>1'b1: Per Buffer Addressability mode</p> <p>The completion of PBA access is confirmed by MRSTAT.pda_done in the same way as PDA.</p> <p>Programming Mode: Dynamic</p>
29:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RW	0x0	<p>mr_addr Address of the mode register that is to be written to. 4'b0000: MR0 4'b0001: MR1 4'b0010: MR2 4'b0011: MR3 4'b0100: MR4 4'b0101: MR5 4'b0110: MR6 4'b0111: MR7 Don't Care for LPDDR3/LPDDR4 (see MRCTRL1.mr_data for mode register addressing in LPDDR3/LPDDR4). In case of DDR4, the bit[3:2] corresponds to the bank group bits. Programming Mode: Dynamic</p>
11:6	RO	0x00	reserved
5:4	RW	0x3	<p>mr_rank Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits should be set to 1. 2'b01: select rank 0 only 2'b10: select rank 1 only 2'b11: select rank 0 and 1 Programming Mode: Dynamic</p>
3	RW	0x0	<p>sw_init_int Indicates whether Software intervention is allowed via MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. 1'b0: Software intervention is not allowed. 1'b1: Software intervention is allowed. Programming Mode: Dynamic</p>
2	RW	0x0	<p>pda_en Indicates whether the mode register operation is MRS in PDA mode or not 1'b0: MRS 1'b1: MRS in Per DRAM Addressability mode Note that when pba_mode=1, PBA access is initiated instead of PDA access. Programming Mode: Dynamic</p>

Bit	Attr	Reset Value	Description
1	RW	0x0	mpr_en Indicates whether the mode register operation is MRS or WR/RD for MPR (only supported for DDR4) 1'b0: MRS 1'b1: WR/RD for MPR Programming Mode: Dynamic
0	RW	0x0	mr_type Indicates whether the mode register operation is read or write. Only used for LPDDR3/LPDDR4/DDR4. 1'b0: Write 1'b1: Read Programming Mode: Dynamic

**DDRC MRCTRL1**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	mr_data Mode register write data for all non-LPDDR3/non-LPDDR4 modes. For LPDDR3/LPDDR4, MRCTRL1[15:0] are interpreted as [15:8] MR Address [7:0] MR data for writes, don't care for reads. This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Programming Mode: Dynamic

**DDRC MRSTAT**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	pda_done The SoC core may initiate a MR write operation in PDA/PBA mode only if this signal is low. This signal goes high when three consecutive MRS commands related to the PDA/PBA mode are issued to the SDRAM. This signal goes low when MRCTRL0.pda_en becomes 0. Therefore, it is recommended to write MRCTRL0.pda_en to 0 after this signal goes high in order to prepare to perform PDA operation next time. 1'b0: Indicates that mode register write operation related to PDA/PBA is in progress or has not started yet. 1'b1: Indicates that mode register write operation related to PDA/PBA has completed. Programming Mode: Dynamic
7:1	RO	0x00	reserved



Bit	Attr	Reset Value	Description
0	RO	0x0	<p>mr_wr_busy</p> <p>The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when MRSTAT.mr_wr_busy is high.</p> <p>1'b0: Indicates that the SoC core can initiate a mode register write operation</p> <p>1'b1: Indicates that mode register write operation is in progress</p> <p>Programming Mode: Dynamic</p>

**DDRC MRCTRL2**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>mr_device_sel</p> <p>Indicates the device(s) to be selected during the MRS that happens in PDA mode. Each bit is associated with one device. For example, bit[0] corresponds to Device 0, bit[1] to Device 1 etc. A '1' should be programmed to indicate that the MRS command should be applied to that device.</p> <p>A '0' indicates that the MRS commands should be skipped for that device.</p> <p>Programming Mode: Dynamic</p>

**DDRC DERATEEN**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	<p>rc_derate_value</p> <p>Derate value of tRC for LPDDR4</p> <p>3'b000: Derating uses +1.</p> <p>3'b001: Derating uses +2.</p> <p>3'b010: Derating uses +3.</p> <p>3'b011: Derating uses +4.</p> <p>Present only in designs configured to support LPDDR4. The required number of cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding up the next integer.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:4	RW	0x0	<p>derate_byte</p> <p>Derate byte Present only in designs configured to support LPDDR3/LPDDR4.</p> <p>Indicates which byte of the MRR data is used for derating.</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	RW	0x0	derate_value Derate value 1'b0: Derating uses +1. 1'b1: Derating uses +2. Present only in designs configured to support LPDDR3/LPDDR4 For LPDDR3/4, if the period of core_ddrc_core_clk is less than 1.875ns, this register field should be set to 1; otherwise it should be set to 0. Programming Mode: Quasi-dynamic Group 2 and Group 4
0	RW	0x0	derate_enable Enables derating 1'b0: Timing parameter derating is disabled 1'b1: Timing parameter derating is enabled using MR4 read value. Present only in designs configured to support LPDDR3/LPDDR4 This field must be set to 0 for LPDDR3/LPDDR4 mode. Programming Mode: Dynamic

**DDRC\_DERATEINT**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycle. Programming Mode: Static

**DDRC\_PWRCTL**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	lpddr4_sr_allowed Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register field cannot be modified while PWRCTL.selfref_sw==1. 1'b0: SR-PD -> SR -> SR-PD not allowed 1'b1: SR-PD -> SR -> SR-PD allowed Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
7	RW	0x0	<p>dis_cam_drain_selfref</p> <p>Indicates whether skipping CAM draining is allowed when entering Self-Refresh.</p> <p>This register field cannot be modified while PWRCTL.selfref_sw==1.</p> <p>1'b0: CAMs must be empty before entering SR.</p> <p>1'b1: CAMs are not emptied before entering SR.</p> <p>Programming Mode: Dynamic</p>
6	RW	0x0	<p>stay_in_selfref</p> <p>Self refresh state is an intermediate state to enter to Selfrefresh power down state or exit Self refresh power down state for LPDDR4.</p> <p>This register controls transition from the Self refresh state.</p> <p>1'b1: Prohibit transition from Self refresh state</p> <p>1'b0: Allow transition from Self refresh state</p> <p>Programming Mode: Dynamic</p>
5	RW	0x0	<p>selfref_sw</p> <p>A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating_mode. This is referred to as Software Entry/Exit to Self Refresh.</p> <p>1'b1: Software Entry to Self Refresh</p> <p>1'b0: Software Exit from Self Refresh</p> <p>Programming Mode: Dynamic</p>
4	RW	0x0	<p>mpsm_en</p> <p>When this is 1, the uMCTL2 puts the SDRAM into maximum power saving mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of maximum power saving mode.</p> <p>Present only in designs configured to support DDR4. For non-DDR4, this register should not be set to 1.</p> <p>Programming Mode: Dynamic</p>
3	RW	0x0	<p>en_dfi_dram_clk_disable</p> <p>Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted.</p> <p>Assertion of dfi_dram_clk_disable is as follows:</p> <p>In DDR3, can only be asserted in Self Refresh.</p> <p>In DDR4, can be asserted in the Self Refresh and Maximum Power Saving Mode</p> <p>In LPDDR3, can be asserted in the Self Refresh, Power Down, Deep Power Down and Normal operation (Clock Stop)</p> <p>In LPDDR4, can be asserted in the Self Refresh Power Down, Power Down and Normal operation (Clock Stop)</p> <p>Programming Mode: Dynamic</p>

Bit	Attr	Reset Value	Description
2	RW	0x0	<p>deppowerdown_en</p> <p>When this is 1, uMCTL2 puts the SDRAM into deep powerdown mode when the transaction store is empty.</p> <p>This register must be reset to '0' to bring uMCTL2 out of deep power-down mode. Controller performs automatic SDRAM initialization on deep power-down exit.</p> <p>Present only in designs configured to support LPDDR3. For non-LPDDR3, this register should not be set to 1.</p> <p>Programming Mode: Dynamic</p>
1	RW	0x0	<p>powerdown_en</p> <p>If true then the uMCTL2 goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (PWRTMG.powerdown_to_x32).</p> <p>This register bit may be re-programmed during the course of normal operation.</p> <p>Programming Mode: Dynamic</p>
0	RW	0x0	<p>selfref_en</p> <p>If true then the uMCTL2 puts the SDRAM into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation.</p> <p>Programming Mode: Dynamic</p>

**DDRC PWRTMG**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x40	<p>selfref_to_x32</p> <p>After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en.</p> <p>Unit: Multiples of 32 DFI clocks.</p> <p>Programming Mode: Static</p>
15:8	RW	0x20	<p>t_dpd_x4096</p> <p>Minimum deep power-down time.</p> <p>For LPDDR3, value from the JEDEC specification is 500us.</p> <p>Unit: Multiples of 4096 DFI clocks.</p> <p>Programming Mode: Static</p>
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x10	<p>powerdown_to_x32</p> <p>After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into powerdown. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en.</p> <p>Unit: Multiples of 32 DFI clocks</p> <p>Programming Mode: Static</p>

**DDRC HWLPCTL**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	<p>hw_lp_idle_x32</p> <p>Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0.</p> <p>Unit: Multiples of 32 DFI clocks.</p> <p>Programming Mode: Static</p>
15:2	RO	0x0000	reserved
1	RW	0x1	<p>hw_lp_exit_idle_en</p> <p>When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw).</p> <p>Programming Mode: Static</p>
0	RW	0x1	<p>hw_lp_en</p> <p>Enable for Hardware Low Power Interface.</p> <p>Programming Mode: Quasi-dynamic Group 3</p>

**DDRC HWFFCCTL**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	reserved
6	RW	0x0	<p>target_vrcg</p> <p>Set target value of VRCG (MR13 OP[3]). This field value is used when HWFFC request has been issued.</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
5	RW	0x0	init_vrcg Set initial value of VRCG (MR13 OP[3]). This field value is used when HWFFCCTL.hwffc_en has been changed to 2'b11. Programming Mode: Static
4	RW	0x1	init_fsp Set initial value of FSP-OP (MR13 OP[7]). This field value is used when HWFFCCTL.hwffc_en has been changed to 2'b11. Programming Mode: Static
3:2	RO	0x0	reserved
1:0	RW	0x0	hwffc_en Enable HWFFC through Hardware Low Power Interface. The other fields of this register is used only when changing this field to 11. 2'b00: Disable HWFFC 2'b10: Intermediate, set only when disabling HWFFC 2'b11: Enable HWFFC 2'b01: Not allowed Programming Mode: Dynamic

**DDRC HWFFCSTAT**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	current_vrcg Indicates current value of VRCG (MR13 OP[3]). Programming Mode: Dynamic
8	RO	0x0	current_fsp Indicates current value of FSP-OP (MR13 OP[7]). Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RO	0x0	current_frequency Indicates the current frequency. 1'b0: Frequency 0/Normal 1'b1: Frequency 1/FREQ1 Programming Mode: Dynamic
3:2	RO	0x0	reserved
1	RO	0x0	hwffc_operating_mode Operating mode of HWFFC. 1'b0: Normal 1'b1: Self Refresh or SR-Powerdown Programming Mode: Dynamic
0	RO	0x0	hwffc_in_progress Indicates HWFFC is in progress. Programming Mode: Dynamic

**DDRC RFSHCTL0**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x2	<p>refresh_margin</p> <p>Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom_x32. Note that, in LPDDR3/LPDDR4, internally used t_rfc_nom_x32 may be equal to RFSHTMG.t_rfc_nom_x32 &gt; 2 if derating is enabled (DERATEEN.derate_enable=1). Otherwise, internally used t_rfc_nom_x32 will be equal to RFSHTMG.t_rfc_nom_x32.</p> <p>Unit: Multiples of 32 DFI clocks.</p> <p>Programming Mode: Dynamic - Refresh Related</p>
19:17	RO	0x0	reserved
16:12	RW	0x10	<p>refresh_to_x32</p> <p>If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, but it has not expired (RFSHCTL0.refresh_burst+1) times yet, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful, but before it is absolutely required. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2.</p> <p>Unit: Multiples of 32 DFI clocks.</p> <p>Programming Mode: Dynamic - Refresh Related</p>
11:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:4	RW	0x00	<p>refresh_burst</p> <p>The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worstcase latency associated with refreshes.</p> <p>5'h0: Single refresh 5'h1: Burst-of-2 refresh 5'h7: Burst-of-8 refresh</p> <p>For DDR2/3, the refresh is always per-rank and not perbank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst was due. In this situation, the refresh burst will be delayed until the PHYinitiated update is complete.</p> <p>Programming Mode: Dynamic - Refresh Related</p>
3	RO	0x0	reserved
2	RW	0x0	<p>per_bank_refresh</p> <p>1'b0: All bank refresh 1'b1: Per bank refresh</p> <p>Per bank refresh allows traffic to flow to other banks. Per bank refresh should be supported by all LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Static</p>
1:0	RO	0x0	reserved

**DDRC RFSHCTL1**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	<p>refresh_timer1_start_value_x32</p> <p>Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter.</p> <p>Unit: Multiples of 32 DFI clock cycles.</p> <p>Programming Mode: Dynamic - Refresh Related</p>
15:12	RO	0x0	reserved



Bit	Attr	Reset Value	Description
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Dynamic - Refresh Related

**DDRC\_RFSHCTL3**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	refresh_mode Fine Granularity Refresh Mode 3'b000: Fixed 1x (Normal mode) 3'b001: Fixed 2x 3'b010: Fixed 4x 3'b101: Enable on the fly 2x (not supported) 3'b110: Enable on the fly 4x (not supported) Everything else - reserved Note: Only Fixed 1x mode is supported if RFSHCTL3.dis_auto_refresh = 1. Note: The on-the-fly modes are not supported in this version of the uMCTL2. Note: This must be set up while the Controller is in reset or while the Controller is in self-refresh mode. Changing this during normal operation is not allowed. Making this a dynamic register will be supported in future version of the uMCTL2. Note: This register field has effect only if a DDR4 SDRAM device is in use (MSTR. ddr4 = 1). Programming Mode: Quasi-dynamic Group 2
3:2	RO	0x0	reserved
1	RW	0x0	refresh_update_level Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh register(s) have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). The refresh register(s) are automatically updated when exiting reset. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>dis_auto_refresh</p> <p>When '1', disable auto-refresh generated by the uMCTL2. When auto-refresh is disabled, the SoC core must generate refreshes using the registers DBGCMDB.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the uMCTL2. If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), disable autorefresh is not supported, and this bit must be set to '0'. (DDR4 only) If FGR mode is enabled (RFSHCTL3.refresh_mode &gt; 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly.</p> <p>Programming Mode: Dynamic - Refresh Related</p>

**DDRC RFSHTMG**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31	RW	0x0	<p>t_rfc_nom_x1_sel</p> <p>Specifies whether the t_rfc_nom_x1_x32 register value is x1 or x32.</p>
30:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x062	<p>t_rfc_nom_x1_x32</p> <p>tREFI: Average time interval between refreshes per rank (Specification: 7.8us for DDR3 and DDR4. See JEDEC specification for LPDDR3 and LPDDR4).</p> <p>For LPDDR3/LPDDR4:</p> <p>if using all-bank refreshes (RFSHCTL0.per_bank_refresh= 0), this register should be set to tREFIab</p> <p>if using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), this register should be set to tREFIpb</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tREFI/2), no rounding up.</p> <p>In DDR4 mode, tREFI value is different depending on the refresh mode. The user should program the appropriate value from the spec based on the value programmed in the refresh mode register.</p> <p>Note that if RFSHTMG.t_rfc_nom_x1_sel==1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min; if RFSHTMG.t_rfc_nom_x1_sel==0, RFSHTMG.t_rfc_nom_x1_x32*32 must be greater than RFSHTMG.t_rfc_min; RFSHTMG.t_rfc_nom_x32 must be greater than 0x1.</p> <p>Non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE.</p> <p>DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF.</p> <p>DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF.</p> <p>Unit: Clocks or multiples of 32 clocks, depending on RFSHTMG.t_rfc_nom_x1_sel.</p> <p>Programming Mode: Dynamic - Refresh Related</p>
15	RW	0x0	<p>lpddr3_trefbw_en</p> <p>Used only when LPDDR3 memory type is connected. Should only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not.</p> <p>1'b0: tREFBW parameter not used</p> <p>1'b1: tREFBW parameter used</p> <p>Programming Mode: Static</p>
14:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x08c	<p>t_rfc_min</p> <p>tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min should be set to RoundUp(RoundUp(tRFCmin/tCK)/2).</p> <p>In LPDDR3/LPDDR4 mode:</p> <p>if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab</p> <p>if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb</p> <p>In DDR4 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user should program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Dynamic - Refresh Related</p>

**DDRC CRCPARCTL0**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	<p>dfi_alert_err_cnt_clr</p> <p>DFI alert error count clear. Clear bit for DFI alert error counter. Asserting this bit will clear the DFI alert error counter, CRCPARSTAT.dfi_alert_err_cnt. When the clear operation is complete, the uMCTL2 automatically clears this bit.</p> <p>Programming Mode: Dynamic</p>
1	W1C	0x0	<p>dfi_alert_err_int_clr</p> <p>Interrupt clear bit for DFI alert error. If this bit is set, the alert error interrupt on CRCPARSTAT.dfi_alert_err_int will be cleared. When the clear operation is complete, the uMCTL2 automatically clears this bit.</p> <p>Programming Mode: Dynamic</p>
0	RW	0x0	<p>dfi_alert_err_int_en</p> <p>Interrupt enable bit for DFI alert error. If this bit is set, any parity/CRC error detected on the dfi_alert_n input will result in an interrupt being set on CRCPARSTAT.dfi_alert_err_int.</p> <p>Programming Mode: Dynamic</p>

**DDRC CRCPARCTL1**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>retry_add_rd_lat</p> <p>Retry additional read latency value. Delay value used is retry_add_rd_lat+1. Only used if CRCPARCTL1.retry_add_rd_lat_en is enabled.</p> <p>Selects the number of pipeline stages to dfi_rddata_valid/dfi_rddata/dfi_rddata_dbi before rest of internal uMCTL2 logic observes it.</p> <p>Required to compensate for fact delay in PHY/PCB for generating dfi_alert_n for retry may be more than the delay in PHY/PCB on read data path.</p> <p>Recommended settings (in terms of core_ddrc_core_clk):            (Maximum Alert delay through PHY/PCB from erroneous read command including tPAR_UNKNOWN) - (Minimum Read data delay through PHY/PCB from erroneous read command) + (PHY's max granularity of dfi_rddata beats that may be corrupted before erroneous Read)</p> <p>Note: This calculation depends on various items such as RL, tPAR_ALERT_ON/tPAR_UNKNOWN/RCD/PHY/PCB behavior.</p> <p>Unit: DFI clock cycles.</p> <p>Programming Mode: Static</p>
15	RW	0x0	<p>retry_add_rd_lat_en</p> <p>Retry additional read latency enable. Number of pipeline stages selected is defined as CRCPARCTL1.retry_add_lat+1. Only set if CRCPARCTL1.crc_parity_retry_enable = 1</p> <p>Programming Mode: Static</p>
14:13	RO	0x0	reserved
12	RW	0x1	<p>caparity_disable_before_sr</p> <p>If DDR4-SDRAM's CA parity is enabled by INIT6.mr5[2:0] != 0 and this register is set to 1, CA parity is automatically disabled before Self-Refresh entry and enabled after SelfRefresh exit by issuing MR5.</p> <p>1'b1: CA parity is disabled before Self-Refresh entry            1'b0: CA parity is not disabled before Self-Refresh entry</p> <p>If Geardown is used by MSTR.geardown_mode=1, this register must be set to 1.</p> <p>If this register set to 0, DRAMTMG5.t_ckesr and DRAMTMG5.t_cksre must be increased by PL(Parity latency)</p> <p>Programming Mode: Static</p>
11:8	RO	0x0	reserved
7	RW	0x0	<p>crc_inc_dm</p> <p>CRC Calculation setting register</p> <p>1'b1: CRC includes DM signal            1'b0: CRC not includes DM signal</p> <p>Present only in designs configured to support DDR4.</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
6:5	RO	0x0	reserved
4	RW	0x0	<p>crc_enable CRC enable Register 1'b1: Enable generation of CRC 1'b0: Disable generation of CRC The setting of this register should match the CRC mode register setting in the DRAM. Programming Mode: Static</p>
3:1	RO	0x0	reserved
0	RW	0x0	<p>parity_enable C/A Parity enable register 1'b1: Enable generation of C/A parity and detection of C/A parity error 1'b0: Disable generation of C/A parity and disable detection of C/A parity error If RCD's parity error detection or SDRAM's parity detection is enabled, this register should be 1. Programming Mode: Static</p>

**DDRC\_CRCPARSTAT**

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	<p>dfi_alert_err_fatal_int Fatal parity error interrupt. One or more these situation below happens, this interrupt bit is set: MPSMX caused parity error. (RCD's parity error detection only) Parity error happens again during software intervention time MRS was in retry_fifo_max_hold_timer_x4 window from alert_n=0 or STAT.operating_mode is Init. It remains set until cleared by CRCPARCTL0.dfi_alert_err_fatal_clr. If this interrupt is asserted, system reset is strongly recommended. Programming Mode: Static</p>
16	RO	0x0	<p>dfi_alert_err_int DFI alert error interrupt. If a parity/CRC error is detected on dfi_alert_n, and the interrupt is enabled by CRCPARCTL0.dfi_alert_err_int_en, this interrupt bit will be set. It will remain set until cleared by CRCPARCTL0.dfi_alert_err_int_clr Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	<p>dfi_alert_err_cnt</p> <p>DFI alert error count.</p> <p>If a parity/CRC error is detected on dfi_alert_n, this counter be incremented. This is independent of the setting of CRCPARCTL0.dfi_alert_err_int_en. It will saturate at 0xFFFF, and can be cleared by asserting CRCPARCTL0.dfi_alert_err_cnt_clr.</p> <p>Programming Mode: Static</p>

**DDRC\_INIT0**

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	<p>skip_dram_init</p> <p>If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed</p> <p>2'b00: SDRAM Intialization routine is run after power-up</p> <p>2'b01: SDRAM Intialization routine is skipped after powerup. Controller starts up in Normal Mode</p> <p>2'b11: SDRAM Intialization routine is skipped after powerup. Controller starts up in Self-refresh Mode</p> <p>2'b10: SDRAM Intialization routine is run after power-up.</p> <p>Programming Mode: Quasi-dynamic Group 2</p>
29:26	RO	0x0	reserved
25:16	RW	0x002	<p>post_cke_x1024</p> <p>Cycles to wait after driving CKE high to start the SDRAM initialization sequence.</p> <p>Unit: 1024 DFI clock cycles.</p> <p>LPDDR3 typically requires this to be programmed for a delay of 200 us.</p> <p>LPDDR4 typically requires this to be programmed for a delay of 2 us.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value.</p> <p>Programming Mode: Static</p>
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x04e	<p>pre_cke_x1024 Cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. LPDDR3: tINIT1 of 100 ns (min) LPDDR4: tINIT3 of 2 ms (min) When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Programming Mode: Static</p>

**DDRC\_INIT1**

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	<p>dram_rstn_x1024 Number of cycles to assert SDRAM reset signal during init sequence. This is only present for designs supporting DDR3, DDR4 or LPDDR4 devices. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 1024 DFI clock cycles. Programming Mode: Static</p>
15:4	RO	0x000	reserved
3:0	RW	0x0	<p>pre_ocrd_x32 Wait period before driving the OCD complete command to SDRAM. Unit: Counts of a global timer that pulses every 32 DFI clock cycles. There is no known specific requirement for this; it may be set to zero. Programming Mode: Static</p>

**DDRC\_INIT2**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved



Bit	Attr	Reset Value	Description
15:8	RW	0x0d	<p>idle_after_reset_x32</p> <p>Idle time after the reset command, tINIT4. Present only in designs configured to support LPDDR2.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value.</p> <p>Unit: 32 DFI clock cycles.</p> <p>Value After Reset: "(MEMC_LPDDR2_EN) ? 0xd : 0x0"</p> <p>Exists: MEMC_LPDDR2==1</p> <p>Programming Mode: Static</p>
7:4	RO	0x0	reserved
3:0	RW	0x5	<p>min_stable_clock_x1</p> <p>Time to wait after the first CKE high, tINIT2. Present only in designs configured to support LPDDR3.</p> <p>LPDDR3 typically requires 5 x tCK delay.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value.</p> <p>Unit: DFI clock cycles.</p> <p>Programming Mode: Static</p>

**DDRC INIT3**

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>mr</p> <p>DDR3/DDR4: Value loaded into MR0 register.</p> <p>LPDDR3/LPDDR4 - Value to write to MR1 register</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 4</p>
15:0	RW	0x0510	<p>emr</p> <p>DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. If PHY-evaluation mode training is enabled, this bit is set appropriately by the uMCTL2 during write leveling.</p> <p>LPDDR3/LPDDR4 - Value to write to MR2 register</p> <p>Programming Mode: Quasi-dynamic Group 4</p>

**DDRC INIT4**

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>emr2</p> <p>DDR3/DDR4: Value to write to MR2 register</p> <p>LPDDR3/LPDDR4: Value to write to MR3 register</p> <p>Programming Mode: Quasi-dynamic Group 4</p>

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	emr3 DDR3/DDR4: Value to write to MR3 register LPDDR3: Unused LPDDR4: Value to write to MR13 register Programming Mode: Quasi-dynamic Group 2 and Group 4

**DDRC INIT5**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x10	dev_zqinit_x32 ZQ initial calibration, tZQINIT. Present only in designs configured to support DDR3 or DDR4 or LPDDR3. DDR3 typically requires 512 SDRAM clock cycles. DDR4 requires 1024 SDRAM clock cycles. LPDDR3 requires 1 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 32 DFI clock cycles. Programming Mode: Static
15:10	RO	0x00	reserved
9:0	RW	0x004	max_auto_init_x1024 Maximum duration of the auto initialization, tINIT5. Present only in designs configured to support LPDDR3. LPDDR3 typically requires 10 us. Unit: 1024 DFI clock cycles. Programming Mode: Static

**DDRC INIT6**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4- Value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:0	RW	0x0000	mr5 DDR4- Value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Programming Mode: Quasi-dynamic Group 1 and Group 4

**DDRC INIT7**

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr6 DDR4- Value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	mr22 LPDDR4- Value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Programming Mode: Quasi-dynamic Group 4

**DDRC DIMMCTL**

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	mrs_bg1_en Enable for BG1 bit of MRS command. BG1 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs which do not have BG1 are attached and both the CA parity and the Output Inversion are enabled, this must be set to 0, so that the calculation of CA parity will not include BG1 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. If address mirroring is enabled, this is applied to BG1 of even ranks and BG0 of odd ranks. 1'b1: Enabled 1'b0: Disabled Programming Mode: Static
3	RW	0x0	mrs_a17_en Enable for A17 bit of MRS command. A17 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs which do not have A17 are attached and the Output Inversion are enabled, this must be set to 0, so that the calculation of CA parity will not include A17 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. 1'b1: Enabled 1'b0: Disabled Programming Mode: Static
2:0	RO	0x0	reserved

**DDRC RANKCTL**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x6	<p>diff_rank_wr_gap</p> <p>Only present for multi-rank configurations.</p> <p>Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks.</p> <p>This is used to switch the delays in the PHY to match the rank requirements. This value should consider both PHY requirement and ODT requirement.</p> <p>PHY requirement:</p> <p>tphy_wrsgap (see PHY databook for value of tphy_wrsgap)</p> <p>If CRC feature is enabled, should be increased by 1.</p> <p>If write preamble is set to 2tCK(DDR4 only), should be increased by 1.</p> <p>If write postamble is set to 1.5tCK(LPDDR4 only), should be increased by 1.</p> <p>ODT requirement:</p> <p>The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes.</p> <p>For LPDDR4, the requirement is <math>ODTL_{off} - ODTL_{on} - BL/2 + 1</math></p> <p>When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer.</p> <p>Programming Mode: Quasi-dynamic Group 2</p>
7:4	RW	0x6	<p>diff_rank_rd_gap</p> <p>Only present for multi-rank configurations.</p> <p>Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks.</p> <p>This is used to switch the delays in the PHY to match the rank requirements.</p> <p>This value should consider both PHY requirement and ODT requirement.</p> <p>PHY requirement:</p> <p>tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap)</p> <p>If read preamble is set to 2tCK(DDR4 only), should be increased by 1.</p> <p>If read postamble is set to 1.5tCK(LPDDR4 only), should be increased by 1.</p> <p>ODT requirement:</p> <p>The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads.</p> <p>When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer.</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
3:0	RW	0xf	<p>max_rank_rd</p> <p>Only present for multi-rank configurations.</p> <p>Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus.</p> <p>This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness.</p> <p>This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it.</p> <p>Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF.</p> <p>Programming Mode: Static</p>

**DDRC\_DRAMTMG0**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RW	0x0f	<p>wr2pre Minimum time between write and precharge to same bank. Unit: DFI Clocks Specifications: <math>WL + BL/2 + tWR = \text{approximately } 8 \text{ cycles} + 15 \text{ ns} = 14 \text{ clocks @400MHz}</math> and less for lower frequencies where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>
23:22	RO	0x0	reserved
21:16	RW	0x10	<p>t_faw tFAW Valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15	RO	0x0	reserved
14:8	RW	0x1b	<p>t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:2 frequency ratio mode, program this to (tRAS(max)-1)/2. No rounding up. Unit: Multiples of 1024 DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x0f	<p>t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank.</p> <p>When the controller is operating in 1:2 frequency mode, 1T mode, program this to tRAS(min)/2. No rounding up.</p> <p>When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, program this to (tRAS(min)/2) and round it up to the next integer value.</p> <p>Unit: DFI Clocks</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG1**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x08	<p>t_xp tXP: Minimum time after power-down exit to any operation. For DDR3, this should be programmed to tXPDLL if slow powerdown exit is selected in MR0[12].</p> <p>If C/A parity for DDR4 is used, set to (tXP+PL) instead.</p> <p>If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value.</p> <p>Units: DFI Clocks</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:14	RO	0x0	reserved
13:8	RW	0x04	<p>rd2pre tRTP: Minimum time from read to precharge of same bank.</p> <p>DDR3: tAL + max (tRTP, 4)</p> <p>DDR4: Max of following two equations: tAL + max (tRTP, 4) or, RL + BL/2 - tRP (*).</p> <p>LPDDR3: BL/2 + max(tRTP,4) - 4</p> <p>LPDDR4: BL/2 + max(tRTP,8) - 8</p> <p>(*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation.</p> <p>When the controller is operating in 1:2 mode, 1T mode, divide the above value by 2. No rounding up.</p> <p>When the controller is operating in 1:2 mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x14	<p>t_rc</p> <p>tRC: Minimum time between activates to same bank.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG2**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x03	<p>write_latency</p> <p>Set to WL. Time from write command to write data on SDRAM interface.</p> <p>When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer.</p> <p>This register field is not required for DDR3 (except if MEMC_TRAINING is set), as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols</p> <p>Unit: DFI clocks</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>
23:22	RO	0x0	reserved
21:16	RW	0x05	<p>read_latency</p> <p>Set to RL. Time from read command to read data on SDRAM interface.</p> <p>When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer.</p> <p>This register field is not required for DDR3 (except if MEMC_TRAINING is set), as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols</p> <p>Unit: DFI clocks</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>
15:14	RO	0x0	reserved



Bit	Attr	Reset Value	Description
13:8	RW	0x06	<p>rd2wr</p> <p>DDR3: <math>RL + BL/2 + 2 - WL</math></p> <p>DDR4: <math>RL + BL/2 + 1 + WR\_PREAMBLE - WL</math></p> <p>LPDDR3: <math>RL + BL/2 + RU(tDQSKmax/tCK) + 1 - WL</math></p> <p>LPDDR4(DQ ODT is Disabled): <math>RL + BL/2 + RU(tDQSKmax/tCK) + WR\_PREAMBLE + RD\_POSTAMBLE - WL</math></p> <p>LPDDR4(DQ ODT is Enabled) : <math>RL + BL/2 + RU(tDQSKmax/tCK) + RD\_POSTAMBLE - ODTLon - RU(tODTon(min))/tCK</math></p> <p>Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what should be included here.</p> <p>Unit: DFI Clocks.</p> <p>Where:</p> <p>WL = write latency</p> <p>BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM</p> <p>RL = read latency = CAS latency</p> <p>WR_PREAMBLE = write preamble. This is unique to DDR4 and LPDDR4.</p> <p>RD_POSTAMBLE = read postamble. This is unique to LPDDR4.</p> <p>For LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSKmax should be used.</p> <p>When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x0d	<p>wr2rd</p> <p>DDR4: <math>CWL + PL + BL/2 + tWTR\_L</math></p> <p>LPDDR3/4: <math>WL + BL/2 + tWTR + 1</math></p> <p>Others: <math>CWL + BL/2 + tWTR</math></p> <p>In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints.</p> <p>Unit: DFI Clocks.</p> <p>Where:</p> <p>CWL = CAS write latency</p> <p>WL = Write latency</p> <p>PL = Parity latency</p> <p>BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM</p> <p>tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification.</p> <p>tWTR = internal write to read command delay. This comes directly from the SDRAM specification.</p> <p>Add one extra cycle for LPDDR3/LPDDR4 operation.</p> <p>When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>

**DDRC DRAMTMG3**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x005	<p>t_mrw</p> <p>Time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR3 or LPDDR4. LPDDR3 typically requires value of 10.</p> <p>LPDDR4: Set this to the larger of tMRW and tMRWCKEL.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to the above values divided by 2 and round it up to the next integer value.</p> <p>For LPDDR3, this register is used for the time from a MRW/MRR to a MRW/MRR.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
19:18	RO	0x0	reserved

Bit	Attr	Reset Value	Description
17:12	RW	0x04	<p>t_mrd</p> <p>tMRD: Cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents:</p> <p>DDR3/4: Time from MRS to MRS command</p> <p>LPDDR3/4: Time from MRS to non-MRS command.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value.</p> <p>If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
11:10	RO	0x0	reserved
9:0	RW	0x00c	<p>t_mod</p> <p>tMOD: Parameter used only in DDR3 and DDR4. Cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead.</p> <p>If MPR writes for DDR4 are used, set to tMOD + AL (or tMPD_PAR + AL if C/A parity is also used).</p> <p>Set to tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG4**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x05	<p>t_rcd</p> <p>tRCD - tAL: Minimum time from activate to read or write command to same bank.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value.</p> <p>Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x4	<p>t_ccd</p> <p>DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group.</p> <p>Others: tCCD: This is the minimum time between two reads or two writes.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value.</p> <p>Unit: DFI clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:12	RO	0x0	reserved
11:8	RW	0x4	<p>t_rrd</p> <p>DDR4: tRRD_L: Minimum time between activates from bank "a" to bank "b" for same bank group.</p> <p>Others: tRRD: Minimum time between activates from bank "a" to bank "b".</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:5	RO	0x0	reserved
4:0	RW	0x05	<p>t_rp</p> <p>tRP: Minimum time from precharge to activate of same bank.</p> <p>When the controller is operating in 1:2 frequency ratio mode, t_rp should be set to RoundDown(RoundUp(tRP/tCK)/2) + 1.</p> <p>When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp should be set to RoundUp(RoundUp(tRP/tCK)/2).</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG5**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x5	<p>t_cksrx</p> <p>This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX.</p> <p>Recommended settings:</p> <p>LPDDR3: 2</p> <p>LPDDR4: tCKCKEH</p> <p>DDR3: tCKSRX</p> <p>DDR4: tCKSRX</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
23:20	RO	0x0	reserved
19:16	RW	0x5	<p>t_cksre</p> <p>This is the time after Self Refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE.</p> <p>Recommended settings:</p> <p>LPDDR3: 2</p> <p>LPDDR4: tCKELCK</p> <p>DDR3: max (10 ns, 5 tCK)</p> <p>DDR4: max (10 ns, 5 tCK) (+ PL(parity latency)(*))</p> <p>(*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register should be increased by PL.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:14	RO	0x0	reserved
13:8	RW	0x04	<p>t_ckesr</p> <p>Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles.</p> <p>Recommended settings:</p> <p>LPDDR3: tCKESR</p> <p>LPDDR4: max(tCKE, tSR)</p> <p>DDR3: tCKE + 1</p> <p>DDR4: tCKE + 1 (+ PL(parity latency)(*))</p> <p>(*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register should be increased by PL.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	<p>t_cke Minimum number of cycles of CKE HIGH/LOW during power-down and self refresh. LPDDR3 mode: Set this to the larger of tCKE or tCKESR LPDDR4 mode: Set this to the larger of tCKE or tSR. non-LPDDR3/non-LPDDR4 designs: Set this to tCKE value. When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG6**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x2	<p>t_ckdpde This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR3: 2 LPDDR4: tCKCKEH DDR3: tCKSRX DDR4: tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
23:20	RO	0x0	reserved
19:16	RW	0x2	<p>t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:4	RO	0x000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x5	<p>t_ckcsx</p> <p>This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit.</p> <p>Recommended settings:  LPDDR3: tXP + 2  LPDDR4: tXP + 2</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>This is only present for designs supporting LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG7**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x2	<p>t_ckpde</p> <p>This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE.</p> <p>Recommended settings:  LPDDR3: 2  LPDDR4: tCKELCK</p> <p>When using DDR3/4 SDRAM, this register should be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>This is only present for designs supporting LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x2	<p>t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: LPDDR3: 2 LPDDR4: 2</p> <p>When using DDR3/4 SDRAM, this register should be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>This is only present for designs supporting LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG8**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	<p>t_xs_fast_x32 tXS_FAST: Exit Self Refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
23	RO	0x0	reserved
22:16	RW	0x03	<p>t_xs_abort_x32 tXS_ABORT: Exit Self Refresh to commands not requiring a locked DLL in Self Refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15	RO	0x0	reserved



Bit	Attr	Reset Value	Description
14:8	RW	0x44	<p>t_xs_dll_x32</p> <p>tXSDLL: Exit Self Refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value.</p> <p>Unit: Multiples of 32 DFI clocks.</p> <p>Note: Used only for DDR3 and DDR4 SDRAMs.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7	RO	0x0	reserved
6:0	RW	0x05	<p>t_xs_x32</p> <p>tXS: Exit Self Refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value.</p> <p>Unit: Multiples of 32 DFI clocks.</p> <p>Note: Used only for DDR3 and DDR4 SDRAMs.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG9**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	<p>ddr4_wr_preamble</p> <p>DDR4 Write preamble mode</p> <p>1'b0: 1tCK preamble</p> <p>1'b1: 2tCK preamble</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
29:19	RO	0x000	reserved
18:16	RW	0x4	<p>t_ccd_s</p> <p>tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value.</p> <p>Present only in designs configured to support DDR4.</p> <p>Unit: DFI clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x4	<p>t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value.</p> <p>Present only in designs configured to support DDR4.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:6	RO	0x0	reserved
5:0	RW	0x0d	<p>wr2rd_s CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints.</p> <p>Present only in designs configured to support DDR4.</p> <p>Unit: DFI Clocks.</p> <p>Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification.</p> <p>When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4</p>

**DDRC DRAMTMG10**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x1c	<p>t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as <math>t_{MOD(min)} + 4nCK</math> <math>t_{MOD(min)}</math> is greater of 24nCK or 15ns <math>15ns / 0.625ns = 24</math> Max value for this register is <math>24 + 4 = 28</math> When the controller is operating in 1:2 mode, program this to <math>(t_{SYNC\_GEAR} / 2)</math> and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:13	RO	0x0	reserved
12:8	RW	0x18	<p>t_cmd_gear Sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as <math>t_{MOD(min)}</math>. <math>t_{MOD(min)}</math> is greater of 24nCK or 15ns <math>15ns / 0.625ns = 24</math> Max value for this register is 24 When the controller is operating in 1:2 mode, program this to <math>(t_{CMD\_GEAR} / 2)</math> and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:4	RO	0x0	reserved
3:2	RW	0x2	<p>t_gear_setup Geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks. When the controller is operating in 1:2 frequency ratio mode, program this to <math>(t_{GEAR\_setup} / 2)</math> and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
1:0	RW	0x2	<p>t_gear_hold Geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks. When the controller is operating in 1:2 frequency ratio mode, program this to <math>(t_{GEAR\_hold} / 2)</math> and round it up to the next integer value. Unit: DFI Clocks Value After Reset: 0x2 Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG11**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x44	<p>post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
23:21	RO	0x0	reserved
20:16	RW	0x0c	<p>t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
15:10	RO	0x00	reserved
9:8	RW	0x2	<p>t_mpx_s tMPX_S: Minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:5	RO	0x0	reserved
4:0	RW	0x1c	<p>t_ckmpe tCKMPE: Minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. Unit: DFI Clocks. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG12**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE. When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:5	RO	0x000	reserved
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4

**DDRC\_DRAMTMG13**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: tODTLoff: This is the latency from CAS-2 command to tODTOff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (tODTLoff/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:3	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x4	<p>t_ppd</p> <p>LPDDR4: tPPD: This is the minimum time from precharge to precharge command.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value.</p> <p>Unit: DFI Clocks.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC\_DRAMTMG14**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x0a0	<p>t_xsr</p> <p>tXSR: Exit Self Refresh to any command.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value.</p> <p>Note: Used only for LPDDR3/LPDDR4 mode.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC\_DRAMTMG15**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31	RW	0x0	<p>en_dfi_lp_t_stab</p> <p>1'b1: Enable using tSTAB when exiting DFI LP. Needs to be set when the PHY is stopping the clock during DFI LP to save maximum power.</p> <p>1'b0: Disable using tSTAB when exiting DFI LP.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
30:8	RO	0x000000	reserved
7:0	RW	0x00	<p>t_stab_x32</p> <p>tSTAB: Stabilization time.</p> <p>It is required in the following two cases for DDR3/DDR4 RDIMM : when exiting power saving mode, if the clock was stopped, after re-enabling it the clock must be stable for a time specified by tSTAB in the case of input clock frequency change (DDR4) after issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4)</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer.</p> <p>Unit: Multiples of 32 DFI clock cycles.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DRAMTMG17**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_vrcg_enable LPDDR4: tVRCG_ENABLE: VREF high current mode enable time. When the controller is operating in 1:2 frequency ratio mode, program this to (tVRCG_ENABLE/2) and round it up to the next integer value. Unit: DFI clocks Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x000	reserved
6:0	RW	0x00	t_vrcg_disable LPDDR4: tVRCG_DISABLE: VREF high current mode disable time. When the controller is operating in 1:2 frequency ratio mode, program this to (tVRCG_DISABLE/2) and round it up to the next integer value. Unit: DFI clocks Programming Mode: Quasi-dynamic Group 4

**DDRC ZQCTL0**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1'b1: Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module. 1'b0: Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024. This is only present for designs supporting DDR3/DDR4 or LPDDR3/LPDDR4 devices. Programming Mode: Dynamic
30	RW	0x0	dis_srx_zqcl 1'b1: Disable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR3 or LPDDR4 mode. 1'b0: Enable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR3 or LPDDR4 mode. This is only present for designs supporting DDR3/DDR4 or LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4

Bit	Attr	Reset Value	Description
29	RW	0x0	<p>zq_resistor_shared</p> <p>1'b1: Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap.</p> <p>1'b0: ZQ resistor is not shared.</p> <p>This is only present for designs supporting DDR3/DDR4 or LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Static</p>
28	RW	0x0	<p>dis_mpsmx_zqcl</p> <p>1'b1: Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode.</p> <p>1'b0: Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode.</p> <p>This is only present for designs supporting DDR4 devices.</p> <p>Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode.</p> <p>Programming Mode: Static</p>
27	RO	0x0	reserved
26:16	RW	0x200	<p>t_zq_long_nop</p> <p>tZQoper for DDR3/DDR4, tZQCL for LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM.</p> <p>When the controller is operating in 1:2 frequency ratio mode:</p> <p>DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value.</p> <p>LPDDR3: program this to tZQCL/2 and round it up to the next integer value.</p> <p>LPDDR4: program this to tZQCAL/2 and round it up to the next integer value.</p> <p>This is only present for designs supporting DDR3/DDR4 or LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Static</p>
15:10	RO	0x00	reserved



Bit	Attr	Reset Value	Description
9:0	RW	0x040	<p>t_zq_short_nop tZQCS for DDR3/DDR4/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value.</p> <p>This is only present for designs supporting DDR3/DDR4 or LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Static</p>

**DDRC\_ZQCTL1**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	<p>t_zq_reset_nop tZQReset: Number of DFI clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to tZQReset/2 and round it up to the next integer value.</p> <p>This is only present for designs supporting LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Static</p>
19:0	RW	0x00100	<p>t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR3/DDR4/LPDDR3/LPDDR4 devices.</p> <p>Meaningless, if ZQCTL0.dis_auto_zq=1.</p> <p>Unit: 1024 DFI clock cycles.</p> <p>This is only present for designs supporting DDR3/DDR4 or LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Static</p>

**DDRC\_ZQCTL2**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>zq_reset</p> <p>Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the uMCTL2 automatically clears this bit. It is recommended NOT to set this signal if in Init, Self-Refresh(except LPDDR4) or SRPowerdown(LPDDR4) or Deep power-down operating modes.</p> <p>This is only present for designs supporting LPDDR3/LPDDR4 devices.</p> <p>Programming Mode: Dynamic</p>

**DDRC ZQSTAT**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	<p>zq_reset_busy</p> <p>SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high.</p> <p>1'b0: Indicates that the SoC core can initiate a ZQ Reset operation.</p> <p>1'b1: Indicates that ZQ Reset operation is in progress.</p> <p>Programming Mode: Dynamic</p>

**DDRC DFITMG0**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	<p>dfi_t_ctrl_delay</p> <p>Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.</p> <p>Programming Mode: Quasi-dynamic Group 4</p>

Bit	Attr	Reset Value	Description
23	RW	0x0	<p>dfi_rddata_use_dfi_phy_clk</p> <p>Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles.</p> <p>1'b0: In terms of HDR (DFI clock) cycles, Only support HDR DFI clock.</p> <p>1'b1: In terms of SDR (DFI PHY clock) cycles</p> <p>Programming Mode: Static</p>
22:16	RW	0x02	<p>dfi_t_rddata_en</p> <p>Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en.</p> <p>Unit: DFI clock cycles</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 4</p>
15	RW	0x0	<p>dfi_wrdata_use_dfi_phy_clk</p> <p>Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values</p> <p>Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles</p> <p>Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles</p> <p>1'b0: In terms of HDR (DFI clock) cycles, Only support HDR DFI clock.</p> <p>1'b1: In terms of SDR (DFI PHY clock) cycles</p> <p>Programming Mode: Static</p>
14	RO	0x0	reserved
13:8	RW	0x00	<p>dfi_tphy_wrdata</p> <p>Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8.</p> <p>Unit: DFI clock cycles.</p> <p>Programming Mode: Quasi-dynamic Group 4</p>
7:6	RO	0x0	reserved
5:0	RW	0x02	<p>dfi_tphy_wrlat</p> <p>Write latency</p> <p>Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value.</p> <p>For LPDDR4, dfi_tphy_wrlat&gt;60 is not supported.</p> <p>Unit: DFI clock cycles</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 4</p>

**DDRC DFITMG1**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	<p>dfi_t_cmd_lat</p> <p>Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, should be set to '0' or the value which matches the CAL mode register setting in the DRAM. If the PHY can add the latency for CAL mode, this should be set to '0'.</p> <p>Valid Range: 0, 3, 4, 5, 6, and 8</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
27:26	RO	0x0	reserved
25:24	RW	0x0	<p>dfi_t_parin_lat</p> <p>Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven.</p> <p>Programming Mode: Quasi-dynamic Group 4</p>
23:21	RO	0x0	reserved
20:16	RW	0x00	<p>dfi_t_wrdata_delay</p> <p>Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. Refer to PHY specification for correct value.</p> <p>Value to be programmed is in terms of DFI clocks, not PHY clocks. In <math>FREQ\_RATIO=2</math>, divide PHY's value by 2 and round up to next integer.</p> <p>Programming Mode: Quasi-dynamic Group 4</p>
15:13	RO	0x0	reserved
12:8	RW	0x04	<p>dfi_t_dram_clk_disable</p> <p>Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value.</p> <p>Programming Mode: Quasi-dynamic Group 4</p>
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x04	<p>dfi_t_dram_clk_enable</p> <p>Specifies the number of DFI clock cycles from the deassertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value.</p> <p>Programming Mode: Quasi-dynamic Group 4</p>

**DDRC DFILPCFG0**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	<p>dfi_tlp_resp</p> <p>Setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, Self Refresh, Deep Power Down and Maximum Power Saving modes.</p> <p>DFI 2.1 specification onwards, recommends using a fixed value of 7 always.</p> <p>Programming Mode: Static</p>
23:20	RW	0x0	<p>dfi_lp_wakeup_dpd</p> <p>Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Deep Power Down mode is entered.</p> <p>Determines the DFI's tlp_wakeup time.</p> <p>4'h0: 16 cycles  4'h1: 32 cycles  4'h2: 64 cycles  4'h3: 128 cycles  4'h4: 256 cycles  4'h5: 512 cycles  4'h6: 1024 cycles  4'h7: 2048 cycles  4'h8: 4096 cycles  4'h9: 8192 cycles  4'hA: 16384 cycles  4'hB: 32768 cycles  4'hC: 65536 cycles  4'hD: 131072 cycles  4'hE: 262144 cycles  4'hF: Unlimited</p> <p>This is only present for designs supporting LPDDR3 devices.</p> <p>Programming Mode: Static</p>
19:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	<p>dfi_lp_en_dpd</p> <p>Enables DFI Low Power interface handshaking during Deep Power Down Entry/Exit.</p> <p>1'b0: Disabled</p> <p>1'b1: Enabled</p> <p>This is only present for designs supporting LPDDR3 devices.</p> <p>Programming Mode: Static</p>
15:12	RW	0x0	<p>dfi_lp_wakeup_sr</p> <p>Value in DFI clpck cycles to drive on dfi_lp_wakeup signal when Self Refresh mode is entered.</p> <p>Determines the DFI's tlp_wakeup time.</p> <p>4'h0: 16 cycles</p> <p>4'h1: 32 cycles</p> <p>4'h2: 64 cycles</p> <p>4'h3: 128 cycles</p> <p>4'h4: 256 cycles</p> <p>4'h5: 512 cycles</p> <p>4'h6: 1024 cycles</p> <p>4'h7: 2048 cycles</p> <p>4'h8: 4096 cycles</p> <p>4'h9: 8192 cycles</p> <p>4'hA: 16384 cycles</p> <p>4'hB: 32768 cycles</p> <p>4'hC: 65536 cycles</p> <p>4'hD: 131072 cycles</p> <p>4'hE: 262144 cycles</p> <p>4'hF: Unlimited</p> <p>Programming Mode: Static</p>
11:9	RO	0x0	reserved
8	RW	0x0	<p>dfi_lp_en_sr</p> <p>Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit.</p> <p>1'b0: Disabled</p> <p>1'b1: Enabled</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
7:4	RW	0x0	dfi_lp_wakeup_pd Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Power Down mode is entered. Determines the DFI's tlp_wakeup time. 4'h0: 16 cycles 4'h1: 32 cycles 4'h2: 64 cycles 4'h3: 128 cycles 4'h4: 256 cycles 4'h5: 512 cycles 4'h6: 1024 cycles 4'h7: 2048 cycles 4'h8: 4096 cycles 4'h9: 8192 cycles 4'hA: 16384 cycles 4'hB: 32768 cycles 4'hC: 65536 cycles 4'hD: 131072 cycles 4'hE: 262144 cycles 4'hF: Unlimited Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit. 1'b0: Disabled 1'b1: Enabled Programming Mode: Static

**DDRC DFILPCFG1**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	<p>dfi_lp_wakeup_mpsm</p> <p>Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Maximum Power Saving Mode is entered.</p> <p>Determines the DFI's tlp_wakeup time.</p> <p>4'h0: 16 cycles  4'h1: 32 cycles  4'h2: 64 cycles  4'h3: 128 cycles  4'h4: 256 cycles  4'h5: 512 cycles  4'h6: 1024 cycles  4'h7: 2048 cycles  4'h8: 4096 cycles  4'h9: 8192 cycles  4'hA: 16384 cycles  4'hB: 32768 cycles  4'hC: 65536 cycles  4'hD: 131072 cycles  4'hE: 262144 cycles  4'hF: Unlimited</p> <p>This is only present for designs supporting DDR4 devices.</p> <p>Programming Mode: Static</p>
3:1	RO	0x0	reserved
0	RW	0x0	<p>dfi_lp_en_mpsm</p> <p>Enables DFI Low Power interface handshaking during Maximum Power Saving Mode Entry/Exit.</p> <p>1'b0: Disabled  1'b1: Enabled</p> <p>This is only present for designs supporting DDR4 devices.</p> <p>Programming Mode: Static</p>

**DDRC DFIUPD0**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31	RW	0x0	<p>dis_auto_ctrlupd</p> <p>When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2. The core must issue the dfi_ctrlupd_req signal using register DBGCMD.ctrlupd. When '0', uMCTL2 issues dfi_ctrlupd_req periodically.</p> <p>Programming Mode: Quasi-dynamic Group 3</p>



Bit	Attr	Reset Value	Description
30	RW	0x0	dis_auto_ctrlupd_srx When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2 at self-refresh exit. When '0', uMCTL2 issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DFIUPD0.ctrlupd_pre_srx. Programming Mode: Static
29	RW	0x0	ctrlupd_pre_srx Selects dfi_ctrlupd_req requirements at SRX. 1'b0: Send ctrlupd after SRX 1'b1: Send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req will be issued when SRX. Programming Mode: Static
28:26	RO	0x0	reserved
25:16	RW	0x040	dfi_t_ctrlup_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Programming Mode: Static
15:10	RO	0x00	reserved
9:0	RW	0x003	dfi_t_ctrlup_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The uMCTL2 expects the PHY to respond within this time. If the PHY does not respond, the uMCTL2 will de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x3. Programming Mode: Static

**DDRC DFIUPD1**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between uMCTL2 initiated DFI update requests (which is executed whenever the uMCTL2 is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the uMCTL2 is idle. Minimum allowed value for this field is 1. Unit: 1024 DFI clock cycles Programming Mode: Static
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x01	<p>dfi_t_ctrlupd_interval_max_x1024</p> <p>This is the maximum amount of time between uMCTL2 initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1.</p> <p>Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024.</p> <p>Unit: 1024 DFI clock cycles</p> <p>Programming Mode: Static</p>

**DDRC DFIUPD2**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RW	0x1	<p>dfi_phyupd_en</p> <p>Enables the support for acknowledging PHY-initiated updates:</p> <p>1'b0: Disabled</p> <p>1'b1: Enabled</p> <p>Programming Mode: Static</p>
30:0	RO	0x00000000	reserved

**DDRC DFIMISC**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	<p>dfi_frequency</p> <p>Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY.</p> <p>Programming Mode: Quasi-dynamic Group 1</p>
7:6	RO	0x0	reserved
5	RW	0x0	<p>dfi_init_start</p> <p>PHY init start request signal. When asserted it triggers the PHY init start request.</p> <p>Programming Mode: Quasi-dynamic Group 3</p>
4	RW	0x0	<p>ctl_idle_en</p> <p>Enables support of ctl_idle signal, which is non-DFI related pin specific to certain Synopsys PHYs. See signal description of ctl_idle signal for further details of ctl_idle functionality.</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
3	RW	0x0	<p>share_dfi_dram_clk_disable</p> <p>Indicate dfi_dram_clk_disable is shared for two channels or not.</p> <p>1'b1: Share mode</p> <p>1'b0: Not share</p> <p>In Shared mode, Controller does not request PHY stop clock while any rank of any channel has not disable clock. Note: when dfi_dram_clk_disable is shared by two channels, an additional DFF is inserted, that will cause dram clock enable is delay one cycle.</p> <p>Suggest set dfi_t_dram_clk_enable value to Tdram_clk_enable+1. Tdram_clk_enable value is from PHY, which indicate how many cycles from dfi_dram_clk_disable de-assert to dram clock output.</p> <p>Programming Mode: Static</p>
2	RW	0x0	<p>dfi_data_cs_polarity</p> <p>Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals.</p> <p>1'b0: Signals are active low.</p> <p>1'b1: Signals are active high.</p> <p>Programming Mode: Static</p>
1	RW	0x0	<p>phy_dbi_mode</p> <p>DBI implemented in DDRC or PHY.</p> <p>1'b0: DDRC implements DBI functionality.</p> <p>1'b1: PHY implements DBI functionality. Present only in designs configured to support DDR4 and LPDDR4.</p> <p>Programming Mode: Static</p>
0	RW	0x1	<p>dfi_init_complete_en</p> <p>PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation.</p> <p>Programming Mode: Quasi-dynamic Group 3</p>

**DDRC DFITMG2**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x02	<p>dfi_tphy_rdcslat</p> <p>Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x02	<p>dfi_tphy_wrclat</p> <p>Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrclat. Refer to PHY specification for correct value.</p> <p>Programming Mode: Quasi-dynamic Group 2 and Group 4</p>

**DDRC DFITMG3**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RW	0x00	<p>dfi_t_geardown_delay</p> <p>The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value.</p> <p>When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value.</p> <p>Unit: DFI Clocks</p> <p>Programming Mode: Static</p>

**DDRC DFISTAT**

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	<p>dfi_lp_ack</p> <p>Stores the value of the dfi_lp_ack input to the controller.</p> <p>Programming Mode: Dynamic</p>
0	RO	0x0	<p>dfi_init_complete</p> <p>The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done.</p> <p>Programming Mode: Dynamic</p>

**DDRC DBICTL**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	rd_dbi_en Read DBI enable signal in DDRC. 1'b0: Read DBI is disabled. 1'b1: Read DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. LPDDR4: MR3[6] Programming Mode: Quasi-dynamic Group 1
1	RW	0x0	wr_dbi_en Write DBI enable signal in DDRC. 1'b0: Write DBI is disabled. 1'b1: Write DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. LPDDR4: MR3[7] Programming Mode: Quasi-dynamic Group 1
0	RW	0x1	dm_en DM enable signal in DDRC. 1'b0: DM is disabled. 1'b1: DM is enabled. This signal must be set the same logical value as DRAM's mode register. DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. LPDDR4: Set this to inverted value of MR13[5] which is opposite polarity from this signal. Programming Mode: Quasi-dynamic Group 3

**DDRC\_DFIPHYMSTR**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	dfi_phymstr_en Enables the PHY Master Interface. 1'b0: Disabled 1'b1: Enabled Programming Mode: Dynamic

**DDRC\_ADDRMAP0**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_dch_bit0 Selects the HIF address bit used as data channel address bit 0. Valid Range: 0 to 30, and 31 (Traffic constraints apply based on the register value when UMCTL2_EXCL_ACCESS>0. See Exclusive Access section for details.) Internal Base: 2 The selected address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then channel bit is set to 0. Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_cs_bit1 Selects the HIF address bit used as rank address bit 1. Valid Range: 0 to 28, and 31 Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 1 is set to 0. Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_cs_bit0 Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 29, and 31 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 0 is set to 0. Programming Mode: Static

**DDRC\_ADDRMAP1**

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	addrmap_bank_b2 Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 31 and 63 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Programming Mode: Static
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x00	addrmap_bank_b1 Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 32 and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bank_b0 Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 0 is set to 0. Programming Mode: Static

**DDRC ADDRMAP2**

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_col_b5 Full bus width mode: Selects the HIF address bit used as column address bit 5. Half bus width mode: Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_col_b4 Full bus width mode: Selects the HIF address bit used as column address bit 4. Half bus width mode: Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:8	RW	0x0	<p>addrmap_col_b3</p> <p>Full bus width mode: Selects the HIF address bit used as column address bit 3.</p> <p>Half bus width mode: Selects the HIF address bit used as column address bit 4.</p> <p>Valid Range: 0 to 7</p> <p>Internal Base: 3</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field.</p> <p>Note, if UMCTL2_INCL_ARB=1, MEMC_BURST_LENGTH=16, Full bus width (MSTR.data_bus_width=00) and BL16 (MSTR.burst_rdwr=1000), it is recommended to program this to 0.</p> <p>Programming Mode: Static</p>
7:4	RO	0x0	reserved



Bit	Attr	Reset Value	Description
3:0	RW	0x0	<p>addrmap_col_b2</p> <p>Full bus width mode: Selects the HIF address bit used as column address bit 2.</p> <p>Half bus width mode: Selects the HIF address bit used as column address bit 3.</p> <p>Valid Range: 0 to 7</p> <p>Internal Base: 2</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field.</p> <p>Note, if UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=8, it is required to program this to 0 unless:</p> <p>in Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and either</p> <p>In DDR4 and ADDRMAP8.addrmap_bg_b0==0 or</p> <p>In LPDDR4 and ADDRMAP1.addrmap_bank_b0==0</p> <p>If UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=16, it is required to program this to 0 unless:</p> <p>in Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and</p> <p>In DDR4 and ADDRMAP8.addrmap_bg_b0==0</p> <p>Otherwise, if MEMC_BURST_LENGTH=8 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2.</p> <p>If MEMC_BURST_LENGTH=16 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2.</p> <p>If MEMC_BURST_LENGTH=16 and Half Bus Width (MSTR.data_bus_width==01), it is recommended to program this to 0 so that HIF[2] maps to column address bit 3.</p> <p>Programming Mode: Static</p>

**DDRC ADDRMAP3**

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RW	0x00	<p>addrmap_col_b9</p> <p>Full bus width mode: Selects the HIF address bit used as column address bit 9.</p> <p>Half bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR3 mode).</p> <p>Valid Range: 0 to 7, and 31.</p> <p>Internal Base: 9</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0.</p> <p>Note: Per JEDEC DDR3 specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used.</p> <p>Programming Mode: Static</p>
23:21	RO	0x0	reserved
20:16	RW	0x00	<p>addrmap_col_b8</p> <p>Full bus width mode: Selects the HIF address bit used as column address bit 8.</p> <p>Half bus width mode: Selects the HIF address bit used as column address bit 9.</p> <p>Valid Range: 0 to 7, and 31.</p> <p>Internal Base: 8</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0.</p> <p>Note: Per JEDEC DDR3 specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used.</p> <p>Programming Mode: Static</p>
15:13	RO	0x0	reserved
12:8	RW	0x00	<p>addrmap_col_b7</p> <p>Full bus width mode: Selects the HIF address bit used as column address bit 7.</p> <p>Half bus width mode: Selects the HIF address bit used as column address bit 8.</p> <p>Valid Range: 0 to 7, and 31.</p> <p>Internal Base: 7</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0.</p> <p>Programming Mode: Static</p>

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_col_b6 Full bus width mode: Selects the HIF address bit used as column address bit 6. Half bus width mode: Selects the HIF address bit used as column address bit 7. Valid Range: 0 to 7, and 15 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

**DDRC ADDRMAP4**

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	addrmap_col_b11 Full bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR3 mode). Half bus width mode: Unused. To make it unused, this should be tied to 4'hF. Valid Range: 0 to 7, and 31. Internal Base: 11 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR3 specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	<p>addrmap_col_b10</p> <p>Full bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR3 mode).</p> <p>Half bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR3 mode).</p> <p>Valid Range: 0 to 7, and 31.</p> <p>Internal Base: 10</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0.</p> <p>Note: Per JEDEC DDR3 specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used.</p> <p>Programming Mode: Static</p>

**DDRC ADDRMAP5**

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	<p>addrmap_row_b11</p> <p>Selects the HIF address bit used as row address bit 11.</p> <p>Valid Range: 0 to 11, and 15</p> <p>Internal Base: 17</p> <p>The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 11 is set to 0.</p> <p>Programming Mode: Static</p>
23:20	RO	0x0	reserved
19:16	RW	0x0	<p>addrmap_row_b2_10</p> <p>Selects the HIF address bits used as row address bits 2 to 10.</p> <p>Valid Range: 0 to 11, and 15</p> <p>Internal Base: 8 (for row address bit 2), 9 (for row address bit 3), 10 (for row address bit 4) etc increasing to 16 (for row address bit 10)</p> <p>The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. When value 15 is used the values of row address bits 2 to 10 are defined by registers ADDRMAP9, ADDRMAP10, ADDRMAP11.</p> <p>Programming Mode: Static</p>
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b1 Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 11 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b0 Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 11 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static

**DDRC\_ADDRMAP6**

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31	RW	0x0	lpddr3_6gb_12gb Set this to 1 if there is an LPDDR3 SDRAM 6Gb or 12Gb device in use. 1'b1: LPDDR3 SDRAM 6Gb/12Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid. 1'b0: Non-LPDDR3 6Gb/12Gb device in use. All addresses are valid. Present only in designs configured to support LPDDR3. Programming Mode: Static
30:29	RW	0x0	lpddr4_6gb_12gb_24gb Indicates what type of LPDDR4 SDRAM device is in use. 2'b00: No LPDDR4 SDRAM 6Gb/12Gb/24Gb device in use. All addresses are valid. 2'b01: LPDDR4 SDRAM 6Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid. 2'b10: LPDDR4 SDRAM 12Gb device in use. Every address having row[15:14]==2'b11 is considered as invalid. 2'b11: LPDDR4 SDRAM 24Gb device in use. Unsupported. Present only in designs configured to support LPDDR4. Programming Mode: Static
28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	addrmap_row_b15 Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 11, and 15 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 15 is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b14 Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 11, and 15 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 14 is set to 0. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b13 Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 11, and 15 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 13 is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b12 Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 11, and 15 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 12 is set to 0. Programming Mode: Static

**DDRC\_ADDRMAP7**

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b17 Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 11, and 15 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 17 is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b16 Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 11, and 15 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 16 is set to 0. Programming Mode: Static

**DDRC\_ADDRMAP8**

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	addrmap_bg_b1 Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bg_b0 Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Programming Mode: Static

**DDRC\_ADDRMAP9**

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_row_b5 Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 11 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b4 Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 11 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b3 Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 11 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b2 Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 11 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

**DDRC ADDRMAP10**

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved



Bit	Attr	Reset Value	Description
27:24	RW	0x0	addrmap_row_b9 Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 11 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b8 Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 11 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b7 Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 11 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b6 Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 11 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

**DDRC\_ADDRMAP11**

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	<p>addrmap_row_b10</p> <p>Selects the HIF address bits used as row address bit 10.</p> <p>Valid Range: 0 to 11</p> <p>Internal Base: 16</p> <p>The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field.</p> <p>This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15.</p> <p>Programming Mode: Static</p>

**DDRC\_ODTCFG**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x4	<p>wr_odt_hold</p> <p>DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2.</p> <p>Recommended values:</p> <p>DDR3: BL8: 0x6</p> <p>DDR4: BL8: 5 + WR_PREAMBLE + CRC_MODE. WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). CRC_MODE = 0 (not CRC mode), 1 (CRC mode)</p> <p>LPDDR3: BL8: 7 + RU(tODTon(max)/tCK)</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 4</p>
23:21	RO	0x0	reserved
20:16	RW	0x00	<p>wr_odt_delay</p> <p>The delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2.</p> <p>Recommended values:</p> <p>DDR3: 0x0</p> <p>DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode)</p> <p>LPDDR3: WL - 1 - RU(tODTon(max)/tCK)</p> <p>Programming Mode: Quasi-dynamic Group 1 and Group 4</p>
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR3: BL8 - 0x6 DDR4: BL8: 5 + RD_PREAMBLE. RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) LPDDR3: BL8: 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
7	RO	0x0	reserved
6:2	RW	0x00	rd_odt_delay The delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode). WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). If (CL - CWL - RD_PREAMBLE + WR_PREAMBLE) < 0, uMCTL2 does not support ODT for read operation. LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
1:0	RO	0x0	reserved

**DDRC\_ODTMAP**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x2	rank1_rd_odt Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x2	rank1_wr_odt Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
7:6	RO	0x0	reserved
5:4	RW	0x1	rank0_rd_odt Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
3:2	RO	0x0	reserved
1:0	RW	0x1	rank0_wr_odt Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static

**DDRC\_SCHED**

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. Programming Mode: Static
23:13	RO	0x000	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x10	lpr_num_entries Number of entries in the low priority transaction store is this value + 1. (MEMC_NO_OF_ENTRY - (SCHED.lpr_num_entries + 1)) is the number of entries available for the high priority transaction store. Setting this to maximum value allocates all entries to low priority transaction store. Setting this to 0 allocates 1 entry to low priority transaction store and the rest to high priority transaction store. Programming Mode: Static
7:3	RO	0x00	reserved
2	RW	0x1	pageclose If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit will be executed with auto-precharge if SCHED1.pageclose_timer=0. Even if this register set to 1 and SCHED1.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The pageclose feature provides a midway between Open and Close page policies. Programming Mode: Quasi-dynamic Group 3
1:0	RO	0x0	reserved

**DDRC\_SCHED1**

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	<p>pageclose_timer</p> <p>This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer&gt;0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explicit precharge will be attempted to be scheduled.</p> <p>Programming Mode: Static</p>

**DDRC\_PERFLPR1**

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	<p>lpr_xact_run_length</p> <p>Number of transactions that are serviced once the LPR queue goes critical is the smaller of:</p> <p>(a) This number</p> <p>(b) Number of transactions available.</p> <p>Unit: Transaction.</p> <p>Programming Mode: Quasi-dynamic Group 3</p>
23:16	RO	0x00	reserved
15:0	RW	0x007f	<p>lpr_max_starve</p> <p>Number of DFI clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function should not be disabled as it will cause excessive latencies.</p> <p>Programming Mode: Quasi-dynamic Group 3</p>

**DDRC\_PERFWR1**

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	w_max_starve Number of DFI clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function should not be disabled as it will cause excessive latencies. Programming Mode: Quasi-dynamic Group 3

**DDRC\_DBG0**

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4	RW	0x0	dis_collision_page_opt When this is set to '0', auto-precharge is disabled for the flushed command in a collision case. Collision cases are write followed by read to same address, read followed by write to same address, or write followed by write to same address with DBG0.dis_wc bit = 1 (where same address comparisons exclude the two address bits representing critical word). Programming Mode: Static
3:0	RO	0x0	reserved

**DDRC\_DBG1**

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dis_hif When 1, uMCTL2 asserts the HIF command signal hif_cmd_stall. uMCTL2 will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>dis_dq</p> <p>When 1, uMCTL2 will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the uMCTL2, which makes it safe to modify certain register fields associated with reads and writes (see User Guide for details). After setting this bit, it is strongly recommended to poll DBGCAM.wr_data_pipeline_empty and DBGCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly.</p> <p>Programming Mode: Dynamic</p>

**DDRC\_DBGCAM**

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x1	<p>wr_data_pipeline_empty</p> <p>When 1, indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed.</p> <p>Programming Mode: Dynamic</p>
28	RO	0x1	<p>rd_data_pipeline_empty</p> <p>When 1 indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed.</p> <p>Programming Mode: Dynamic</p>
27	RO	0x0	reserved
26	RO	0x1	<p>dbg_wr_q_empty</p> <p>When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters SelfRefresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register should be 1 at that time.</p> <p>Programming Mode: Dynamic</p>



Bit	Attr	Reset Value	Description
25	RO	0x1	dbg_rd_q_empty When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters SelfRefresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register should be 1 at that time. Programming Mode: Dynamic
24	RO	0x0	dbg_stall Stall Programming Mode: Dynamic
23:20	RO	0x0	reserved
19:16	RO	0x0	dbg_w_q_depth Write queue depth The last entry of WR queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Programming Mode: Dynamic
15:12	RO	0x0	reserved
11:8	RO	0x0	dbg_lpr_q_depth Low priority read queue depth. The last entry of Lpr queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Programming Mode: Dynamic
7:0	RO	0x00	reserved

**DDRC DBGCMD**

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ctrlupd Setting this register bit to 1 indicates to the uMCTL2 to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
4	RW	0x0	<p>zq_calib_short</p> <p>Setting this register bit to 1 indicates to the uMCTL2 to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init operating mode. This register bit is ignored when in SelfRefresh(except LPDDR4) and SR-Powerdown(LPDDR4) and Deep power-down operating modes and Maximum Power Saving Mode.</p> <p>Programming Mode: Dynamic</p>
3:2	RO	0x0	reserved
1	RW	0x0	<p>rank1_refresh</p> <p>Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 1. Writing to this bit causes DBGSTAT.rank1_refresh_busy to be set. When DBGSTAT.rank1_refresh_busy is cleared, the command has been stored in uMCTL2.</p> <p>This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode.</p> <p>Programming Mode: Dynamic</p>
0	RW	0x0	<p>rank0_refresh</p> <p>Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 0. Writing to this bit causes DBGSTAT.rank0_refresh_busy to be set. When DBGSTAT.rank0_refresh_busy is cleared, the command has been stored in uMCTL2.</p> <p>This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode.</p> <p>Programming Mode: Dynamic</p>

**DDRC\_DBGSTAT**

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5	RO	0x0	<p>ctrlupd_busy</p> <p>SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the uMCTL2. It is recommended not to perform ctrlupd operations when this signal is high.</p> <p>1'b0: Indicates that the SoC core can initiate a ctrlupd operation.</p> <p>1'b1: Indicates that ctrlupd operation has not been initiated yet in the uMCTL2.</p> <p>Programming Mode: Dynamic</p>
4	RO	0x0	<p>zq_calib_short_busy</p> <p>SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the uMCTL2. It is recommended not to perform ZQCS operations when this signal is high.</p> <p>1'b0: Indicates that the SoC core can initiate a ZQCS operation.</p> <p>1'b1: Indicates that ZQCS operation has not been initiated yet in the uMCTL2.</p> <p>Programming Mode: Dynamic</p>
3:2	RO	0x0	reserved
1	RO	0x0	<p>rank1_refresh_busy</p> <p>SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after DBGCMD.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the uMCTL2. It is recommended not to perform rank1_refresh operations when this signal is high.</p> <p>1'b0: Indicates that the SoC core can initiate a rank1_refresh operation.</p> <p>1'b1: Indicates that rank1_refresh operation has not been stored yet in the uMCTL2.</p> <p>Programming Mode: Dynamic</p>
0	RO	0x0	<p>rank0_refresh_busy</p> <p>SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after DBGCMD.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the uMCTL2. It is recommended not to perform rank0_refresh operations when this signal is high.</p> <p>1'b0: Indicates that the SoC core can initiate a rank0_refresh operation.</p> <p>1'b1: Indicates that rank0_refresh operation has not been stored yet in the uMCTL2.</p> <p>Programming Mode: Dynamic</p>

**DDRC\_SWCTL**

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	sw_done Enable quasi-dynamic register programming outside reset. Program register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. Programming Mode: Dynamic

**DDRC\_SWSTAT**

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	sw_done_ack Register programming done. This register is the echo of SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. Programming Mode: Static

**DDRC\_POISONCFG**

Address: Operational Base + offset (0x036C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	rd_poison_intr_clr Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. Programming Mode: Dynamic
23:21	RO	0x0	reserved
20	RW	0x1	rd_poison_intr_en If set to 1, enables interrupts for read transaction poisoning. Programming Mode: Dynamic
19:17	RO	0x0	reserved
16	RW	0x1	rd_poison_slvrr_en If set to 1, enables SLVERR response for read transaction poisoning. Programming Mode: Dynamic
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	W1C	0x0	wr_poison_intr_clr Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RW	0x1	wr_poison_intr_en If set to 1, enables interrupts for write transaction poisoning. Programming Mode: Dynamic
3:1	RO	0x0	reserved
0	RW	0x1	wr_poison_slvrr_en If set to 1, enables SLVERR response for write transaction poisoning. Programming Mode: Dynamic

**DDRC POISONSTAT**

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	rd_poison_intr_0 Read transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Programming Mode: Dynamic
15:1	RO	0x0000	reserved
0	RO	0x0	wr_poison_intr_0 Write transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Programming Mode: Dynamic

**DDRC PSTAT**

Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	wr_port_busy_0 Indicates if there are outstanding writes for AXI port 0. Programming Mode: Dynamic
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RO	0x0	rd_port_busy_0 Indicates if there are outstanding reads for AXI port 0. Programming Mode: Dynamic

**DDRC\_PCCFG**

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	bl_exp_mode Burst length expansion mode. By default (i.e. bl_exp_mode==0) XPI expands every AXI burst into multiple HIF commands, using the memory burst length as a unit. If set to 1, then XPI will use half of the memory burst length as a unit. This applies to both reads and writes. When MSTR.data_bus_width==00, setting bl_exp_mode to 1 has no effect. This can be used in cases where Partial Writes is enabled (UMCTL2_PARTIAL_WR=1), in order to avoid or minimize t_ccd_l penalty in DDR4 and t_ccd_mw penalty in LPDDR4. Hence, bl_exp_mode=1 is only recommended if DDR4 or LPDDR4. Note that if DBICTL.dm_en=0, functionality is not supported in the following cases: UMCTL2_PARTIAL_WR=0 UMCTL2_PARTIAL_WR=1, MSTR.data_bus_width=01, MEMC_BURST_LENGTH=8 and MSTR.burst_rdwr=1000 (LPDDR4 only) UMCTL2_PARTIAL_WR=1, MSTR.data_bus_width=01, MEMC_BURST_LENGTH=4 and MSTR.burst_rdwr=0100 (DDR4 only), with either MSTR.burstchop=0 or CRCPARCTL1.crc_enable=1 Programming Mode: Static
7:5	RO	0x0	reserved
4	RW	0x0	pagematch_limit Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Programming Mode: Static
3:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>go2critical_en</p> <p>If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr / co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr / co_gs_go2critical_hpr signals at DDRC are driven to 1b'0.</p> <p>Programming Mode: Static</p>

**DDRC PCFGR 0**

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	<p>rd_port_pagematch_en</p> <p>If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register.</p> <p>Programming Mode: Static</p>
13	RW	0x0	<p>rd_port_urgent_en</p> <p>If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command).</p> <p>Programming Mode: Static</p>
12	RW	0x0	<p>rd_port_aging_en</p> <p>If set to 1, enables aging function for the read channel of the port.</p> <p>Programming Mode: Static</p>
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	<p>rd_port_priority</p> <p>Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition -Priority0). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority (2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00.</p> <p>Programming Mode: Static</p>

**DDRC PCFGW 0**

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	<p>wr_port_pagematch_en</p> <p>If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register.</p> <p>Programming Mode: Static</p>
13	RW	0x0	<p>wr_port_urgent_en</p> <p>If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command).</p> <p>Programming Mode: Static</p>
12	RW	0x0	<p>wr_port_aging_en</p> <p>If set to 1, enables aging function for the write channel of the port.</p> <p>Programming Mode: Static</p>
11:10	RO	0x0	reserved



Bit	Attr	Reset Value	Description
9:0	RW	0x000	<p>wr_port_priority</p> <p>Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00.</p> <p>Programming Mode: Static</p>

**DDRC PCTRL 0**

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	<p>port_en</p> <p>Enables AXI port 0.</p> <p>Programming Mode: Dynamic</p>

**DDRPHY REG0**

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	<p>Field0004</p> <p>Reserved.</p>
3	RW	0x1	<p>Field0003</p> <p>Reset digital core, active low.</p>
2	RW	0x1	<p>Field0002</p> <p>Reset analog logic, active low.</p>
1	RW	0x1	<p>Field0001</p> <p>The clock gate signal of DQ module. This signal will be used to disable the clk of the DQ module to save the power when the DDR3/4/LPDDR3/LPDDR4 SDRAM goes to power down mode.</p>
0	RW	0x1	<p>Field0000</p> <p>The digital core and analog logic reset. Active low.</p>

**DDRPHY REG1**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x1	Field0004 The clock gate the training value bypass logic. 1'b0: Clock gate 1'b1: Clock keep
6:5	RW	0x0	Field0003 Reserved. Please keep these bits to 2'h0.
4	RW	0x0	Field0002 The bypass enable signal of the rx odt bypass function. When enable this function, the user can use the register REGA9~REGAC and register REGD9~REGDC to adjust the timing of the rx odt.
3	RW	0x1	Field0001 Choose the burst type that phy can support. 1'b0: Support burst 8/burst16. 1'b1: Reserved.
2:0	RW	0x0	Field0000 Choose the SDRAM that the PHY need to support. 3'h2: DDR3 PHY mode. 3'h3: LPDDR3 PHY mode. 3'h4: DDR4 PHY mode. 3'h5: LPDDR4 PHY mode. Others: Reserved.

**DDRPHY\_REG2**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x2	Field0005 Write leveling CS select signal 2'b00: Select CS0 and CS1 2'b01: Select CS1 2'b10: Select CS0 2'b11: Reserved
5:4	RW	0x2	Field0004 DQS gating CS select signal 2'b00: Select CS0 and CS1. 2'b01: Select CS1. 2'b10: Select CS0.
3	RW	0x0	Field0003 Write leveling Bypass Mode enable signal. Active high. When enable the bypass mode, the user can use the register to adjust the TX DQS/DQ delay.
2	RW	0x0	Field0002 Write leveling Auto mode enable signal. Active high. When enable the auto mode, the PHY will complete to adjust the TX DQS/DQ delay automatically.

Bit	Attr	Reset Value	Description
1	RW	0x0	Field0001 DQS gating Bypass Mode enable signal. Active high. When enable the bypass mode, the user can use the register to adjust the DQS gating position.
0	RW	0x0	Field0000 DQS gating Auto Mode enable signal. Active high. When enable the Auto Mode, the PHY will complete to adjust the DQS gating window automatically.

**DDRPHY\_REG3**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 Write leveling load mode [7:0]. Related to the register REG2[2]. This register stores the load mode value when the user uses the write load mode to enable the write leveling.

**DDRPHY\_REG4**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	Field0001 Write leveling load mode select [1:0]. Related to the register REG2[2]. This register stores the load mode value when the user uses the write load mode to enable the write leveling.
5:0	RW	0x00	Field0000 Write leveling load mode [13:8]. Relate to the register REG2[2]. This register stores the load mode value when the user uses the write load mode to enable the write leveling.

**DDRPHY\_REG5**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x06	Field0000 CL value[FSP0] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM RL. Note: When the phy choose the DDRn mode, RL = CL+AL.

**DDRPHY\_REG6**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	Field0001 Reserved
4:0	RW	0x00	Field0000 AL value[FSP0] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM AL. When the phy choose the LPDDRn mode, this value should keep 5'h0.

**DDRPHY\_REGC**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	Field0006 Choose the read preamble mode when PHY is in LPDDR4 mode. 1'b0: Static. 1'b1: Toggle. Note: This setting should keep the same setting with the MR#1[3] of the LPDDR4.
6	RW	0x0	Field0005 Set to 1'b1 to enable the frequency fast change function for write training/write leveling result switch. When enable this function, PHY will choose the auto write training/write leveling result according to the frequency point setting (REGC[3:2]).
5	RW	0x0	Field0004 Set to 1'b1 to enable the frequency fast change function for DQS-Gating result switch. When enable this function, PHY will choose the auto DQS-Gating result according to the frequency point setting (REGC[3:2]).
4	RW	0x0	Field0003 Reserved. Please keep this bit to 1'b0.
3:2	RW	0x0	Field0002 Used for Fast Frequency Changing. 2'b00: Freq Point 0 2'b01: Freq Point 1 2'b10: Freq Point 2 2'b11: Freq Point 3 After choose the freq point using this register, the user can use the update register to switch the training result belong to this freq point fastly.

Bit	Attr	Reset Value	Description
1	RW	0x0	Field0001 The DQS-Gating model sel. 1'b1: Use the Read Preamble Training mode (Only used for DDR4 ). 1'b0: Use the Normal Read mode (Can used for DDR3/4 and LPDDR3). When the DQS Gating mode chooses the Normal Read mode for DDR4, the Read DQS will be pulling down to 1'b0. So the register REG114/REG124/REG1C4/REG1D4[1:0] should set to 2'b00 to pull down the Read DQS when it is in "high z" state.
0	RW	0x0	Field0000 Reserved. Please keep this bit to 1'b0.

**DDRPHY\_REGE**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x2	Field0001 Used to control the length of the RX ODT. The step is 1x clock cycle. When the value +1, the length of RX ODT will increase 1x clock cycle. Related register REGF. It combines with the register REGF to decide the range of the RX ODT. The default RX ODT length is 4*dfi_clk1x cycles.
3:0	RW	0x3	Field0000 Used to control the start point of the RX ODT. When the value +1, the start point of RX ODT will increase 1x clock cycle. If the user wants to keep the length of the RX ODT unchanged, the users need to increase 1x clock cycle of the length of the RX ODT using the register 0xREGE[7:4]. The default RX ODT start point is RL-2 in regard to the read command.

**DDRPHY\_REGF**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	Field0002 Enable the bypass mode to use the bypass register to control the timing that read out the read back data from the asynchronies FIFO. 1'b1: Enable the bypass mode. 1'b0: Disable the bypass mode. Related register REGF[6:4].
6:4	RW	0x2	Field0001 Choose the timing to get the read back data from the FIFO when the REG1[5] set to 1. When the valid + 1, it will delay 1x clock cycle to get the read back data from the FIFO.
3:0	RW	0xf	Field0000 The DQ width select signal.

**DDRPHY\_REG10**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	Field0006 reg_cab_bp_rank_sel Used to choose the rank when enable the bypass command bus train or only enable one rank of auto command bus train. 2'b10: Choose the Rank0 to do the command bus train. 2'b01: Choose the Rank1 to do the command bus train.
5	RW	0x0	Field0005 reg_cat_bp_cmd_send Used to send the command bus train command. Posedge is valid. When this signal change from low to high, it will send the command bus train command to the SDRAM. The command bus value depends on the reg_cat_bp_mode(REG10[3]), reg_cat_cs_train_value(REG21[5:0]) and reg_ca_train_value(REG22[5:0]).
4	RW	0x0	Field0004 reg_cat_bp_mode Choose the bypass command bus train mode. 1'b0: Choose the mode for CS train. 1'b1: Choose the mode for CA train.
3	RW	0x0	Field0003 reg_cat_bp_start The Bypass command bus train start signal. High is valid. When this bit set to high, the command bus module will go into the bypass command bus train flow.

Bit	Attr	Reset Value	Description
2	RW	0x0	Field0002 reg_cab_bp_en The Bypass command bus train enable signal. High is valid. When this bit set to high, the command path will choose the command bus train module and the perbit skew of command will be controlled by the register directly.
1	RW	0x0	Field0001 reg_cat_start The Auto command bus train start signal. High is valid. When this signal enable, it will begin the command bus train.
0	RW	0x0	Field0000 reg_cat_enable The Auto command bus train enable signal. High is valid. When this signal enable, the command path will switch to the command bus train module.

**DDRPHY\_REG11**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xf	Field0001 reg_tmrw[3:0] Used to control the delay between the MRW command and valid clock/CS requirement after CKE input LOW after MRW command. The delay $\geq \text{MAX}(14\text{ns}, 10\text{nCK})$ .
3:0	RW	0xc	Field0000 reg_tcacd[3:0] Used to control the CA Bus Training Command to CA Bus Training Command Delay( tCACD). The delay should $\geq \text{RU}(20\text{ns}/\text{tCK})$ .

**DDRPHY\_REG12**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x28	Field0000 reg_tvrefca_log[7:0] Used to control the Vref(CA) step time.

**DDRPHY\_REG13**

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x0f	Field0000 reg_tcaent[7:0] Used to control the first CA Bus Training Command following CKE Low(tCAENT). The delay should $\geq 250\text{ns}$ .

**DDRPHY\_REG14**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	Field0001 reg_tckelck[3:0] Used to control the clock and command valid after CKE low(tCKELCK). The delay should $\geq \max(7.5\text{ns}, 3\text{nCK})$ .
3:0	RW	0x1	Field0000 reg_tdstrain[3:0] Data Setup/Hold for Vref(CA) Training Mode.

**DDRPHY\_REG15**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xf	Field0001 reg_tadr[3:0] Used to control the check time of the read back data from the DQ. The delay should $\geq 20\text{ns}$ .
3:0	RW	0x4	Field0000 reg_txcbt[3:0] Used to control the timing parameter tcs_VREF/tCKCKEH/tMRZ. The delay should $\geq \text{MAX}(1.5\text{ns}, 2\text{nCK})$ .

**DDRPHY\_REG16**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	Field0000 reg_trfc[7:0] Used to control the frequency set point switching time(tFC). The delay should $\geq 250\text{ns}$ .

**DDRPHY\_REG17**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved



Bit	Attr	Reset Value	Description
7:0	RW	0x00	Field0000 reg_mr1 Used to control the load mode value of MR1 when command bus train.

**DDRPHY\_REG18**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_mr2 Used to control the load mode value of MR2 when command bus train.

**DDRPHY\_REG19**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_mr3 Used to control the load mode value of MR3 when command bus train.

**DDRPHY\_REG1A**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_mr11 Used to control the load mode value of MR11 when command bus train.

**DDRPHY\_REG1B**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_mr13 Used to control the load mode value of MR13 when command bus train.

**DDRPHY\_REG1C**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Field0000 reg_mr14 Used to control the load mode value of MR14 when command bus train.

**DDRPHY\_REG1D**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_mr22 Used to control the load mode value of MR22 when command bus train.

**DDRPHY\_REG1E**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	Field0000 reg_cha_cat_vref_bp_value[6:0] Used to control the CA VREF value of Channel A. If the user wants to change the CA_VREF value of Channel A at fast frequency change point ( not use the command bus train value). The user can use this register to set the desired value. Then use the reg_ca_perbit_skew_update and reg_freq_choose to update to the corresponding frequency point registers. When the user enable the fast frequency change, the value will be written to the load mode of SDRAM through the load mode command.

**DDRPHY\_REG1F**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	Field0000 reg_chb_cat_vref_bp_value[6:0] Used to control the CA VREF value of Channel B. If the user wants to change the CA_VREF value of Channel B at fast frequency change point ( not use the command bus train value). The user can use this register to set the desired value. Then use the reg_ca_perbit_skew_update and reg_freq_choose to update to the corresponding frequency point registers. When the user enable the fast frequency change, the value will be written to the load mode of SDRAM through the load mode command.

**DDRPHY\_REG20**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	Field0004 reg_cat_vref_bp_en Disable the CA_VREFv train when do the Auto command bus train. High is valid.
6	RW	0x0	Field0003 Choose the CA ODT control mode in LPDDR4 mode. 1'b1: Use the register reg_lpddr4_ca_odt[1:0] to control. 1'b0: Use the dfi_odt to control.
5:4	RW	0x0	Field0002 reg_lpddr4_ca_odt[1:0] When enable the register control mode of CA ODT, the PHY will use this register to control the CA_ODT.
3:1	RW	0x1	Field0001 reg_cat_vref_scan_steps Used to control the CA_VREF scan steps.
0	RW	0x0	Field0000 reg_cs_pwc_disable The disable signal of pulse width control of CS. High is valid. For command bus train, when the PHY do the command bus train of CS, if enable the pulse width control function, the pulse width will decrease 25% for command bus train. Before enter command bus train and after exit command bus train, the pulse width of CS will keep the normal pulse width.

**DDRPHY\_REG21**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x3	Field0001 reg_cat_rank_num[1:0] Define the rank number of the command bus train should support. 2'b11: Two ranks. 2'b01: Only one rank. Others: Not support.
5:0	RW	0x06	Field0000 reg_cat_cs_train_value[5:0] The signal is used to control the CS command bus train pattern.

**DDRPHY\_REG22**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	Field0001 reg_ca_perbit_skew_update Used to update the perbit skew of the command in the command bus train module through the registers. Posedge is valid. When this signal change from low to high, it will update the perbit skew value setting by the register to the command bus train module according to the current reg_freq_choose(REGC[3:2]).
5:0	RW	0x15	Field0000 reg_ca_train_value[5:0] The signal is used to control the CA command bus train pattern.

**DDRPHY REG23**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x3f	Field0000 reg_cat_vref_scan_max[6:0] Set the max value that the Vref train. When the Vref scan arrive to the reg_cat_vref_scan_max, it will stop the Vref scan.

**DDRPHY REG24**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0x3f	Field0000 reg_cat_ca_scan_max[6:0] Set the max value that the perbit skew train. When the perbit skew scan arrive to the reg_cat_ca_scan_max, it will stop the per-bit de-skew scan.

**DDRPHY REG25**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	Field0002 reg_cat_skip_fspy The disable signal to skip use the Auto Command Bus Train module to configure the value of the FSP[Y]. High is valid.
6	RW	0x0	Field0001 reg_cat_skip_cs_train The disable signal to skip the cs train flow of the auto command bus train.
5:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x3	Field0000 reg_cat_channel_number The command channel enable signal of command bus train. High is valid. 2'b11: Enable Channel A and Channel B. 2'b01: Only enable Channel A. 2'b10: Only enable Channel B.

**DDRPHY\_REG29**

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x1	Field005 Reserved.
4	RW	0x0	Field0001 The RX ODT timing bypass enable. 1'b1: Enable the bypass mode. 1'b0: Use the default value. The RX ODT will be open after (RL-1)>>1 dfi_clk1x clock cycles when detect the read command.
3:0	RW	0x0	Field0000 Use to control the RX ODT timing when enable the bypass mode. The RX ODT will be open after REG25[3:0] dfi_clk1x clock cycles when detect the read command.

**DDRPHY\_REG2A**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	Field0002 The power down signal of RAM VREF. 1'b1: Power Down. 1'b0: Open.
6:5	RO	0x0	reserved
4	RW	0x0	Field0001 The bypass mode of read rank switch point at 4x clock cycle precision. The user can use the register REGA6 and REGD6 to adjust the read rank switch point.
3:0	RW	0x0	Field0000 Reserved. Please keep these bits to 4'h0.

**DDRPHY\_REG2B**

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x1	Field0003 Reserved.
6:4	RW	0x1	Field0002 Reserved.
3	RW	0x0	Field0001 Reserved.
2:0	RW	0x1	Field0000 The delay ctrl of write rank switch point at 1x clock cycle precision. It doesn't need to open the bypass mode.

**DDRPHY\_REG2D**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x40	Field0000 Use to set the max number of the read command when do the DQS Gating. When the read commands are more than the max number, it is the DQS Gating Error and this state can be read from the register REG91[5].

**DDRPHY\_REG2E**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 The bit[7:0] of the timer used for DQS Gating. When the clock cycle exceed the bits[15:0] of the timer, it is the DQS Gating error and this state can be read from the register REG91[5].

**DDRPHY\_REG2F**

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	Field0000 The bit[15:8] of the timer used for DQS Gating. When the clock cycle exceed the bits[15:0] of the timer, it is the DQS Gating error and this state can be read from the register REG91[5].

**DDRPHY\_REG30**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	Field0000 The pin wrap sel of pad A0 for DDRn/LPDDRn.

**DDRPHY REG31**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x01	Field0000 The pin wrapsel of pad A1 for DDRn/LPDDRn.

**DDRPHY REG32**

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x02	Field0000 The pin wrapsel of pad A2 for DDRn/LPDDRn.

**DDRPHY REG33**

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x03	Field0000 The pin wrapsel of pad A3 for DDRn/LPDDRn.

**DDRPHY REG34**

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x04	Field0000 The pin wrapsel of pad A4 for DDRn/LPDDRn.

**DDRPHY REG35**

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x05	Field0000 The pin wrapsel of pad A5 for DDRn/LPDDRn.

**DDRPHY REG36**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x06	Field0000 The pin wrapsel of pad A6 for DDRn/LPDDRn.

**DDRPHY REG37**

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x07	Field0000 The pin wrap sel of pad A7 for DDRn/LPDDRn.

**DDRPHY\_REG38**

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x08	Field0000 The pin wrap sel of pad A8 for DDRn/LPDDRn.

**DDRPHY\_REG39**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x09	Field0000 The pin wrap sel of pad A9 for DDRn/LPDDRn.

**DDRPHY\_REG3A**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0a	Field0000 The pin wrap sel of pad A10 for DDRn/LPDDRn.

**DDRPHY\_REG3B**

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0b	Field0000 The pin wrap sel of pad A11 for DDRn/LPDDRn.

**DDRPHY\_REG3C**

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0c	Field0000 The pin wrap sel of pad A12 for DDRn/LPDDRn.

**DDRPHY\_REG3D**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved



Bit	Attr	Reset Value	Description
4:0	RW	0x0d	Field0000 The pin wrap sel of pad A13 for DDRn/LPDDRn.

**DDRPHY\_REG3E**

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0e	Field0000 The pin wrap sel of pad A14 for DDRn/LPDDRn.

**DDRPHY\_REG3F**

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	Field0000 The pin wrap sel of pad A15 for DDRn/LPDDRn.

**DDRPHY\_REG40**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x10	Field0000 The pin wrap sel of pad A16 for DDRn/LPDDRn.

**DDRPHY\_REG41**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x11	Field0000 The pin wrap sel of pad A17 for DDRn/LPDDRn.

**DDRPHY\_REG42**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	Field0000 The pin wrap sel of pad ACTn for DDRn/LPDDRn.

**DDRPHY\_REG43**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x13	Field0000 The pin wrap sel of pad BA0 for DDRn/LPDDRn.

**DDRPHY REG44**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x14	Field0000 The pin wrapssel of pad BA1 for DDRn/LPDDRn.

**DDRPHY REG45**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x15	Field0000 The pin wrapssel of pad BG0 for DDRn/LPDDRn.

**DDRPHY REG46**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x16	Field0000 The pin wrapssel of pad BG1 for DDRn/LPDDRn.

**DDRPHY REG47**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x17	Field0000 The pin wrapssel of pad CK for DDRn/LPDDRn.

**DDRPHY REG48**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x18	Field0000 The pin wrapssel of pad CKB for DDRn/LPDDRn.

**DDRPHY REG49**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x19	Field0000 The pin wrapssel of pad CKE0 for DDRn/LPDDRn.

**DDRPHY REG4A**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x1a	Field0000 The pin wrapssel of pad CSB0 for DDRn/LPDDRn.

**DDRPHY\_REG4B**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x1b	Field0000 The pin wrapssel of pad CSB1 for DDRn/LPDDRn.

**DDRPHY\_REG4C**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x1c	Field0000 The pin wrapssel of pad ODT0 for DDRn/LPDDRn.

**DDRPHY\_REG4D**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x1d	Field0000 The pin wrapssel of pad ODT1 for DDRn/LPDDRn.

**DDRPHY\_REG4E**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x1e	Field0000 The pin wrapssel of pad CKE1 for DDRn/LPDDRn.

**DDRPHY\_REG4F**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x3	Field0003 The pin wrapssel of BYTE 3.
5:4	RW	0x2	Field0002 The pin wrapssel of BYTE 2.
3:2	RW	0x1	Field0001 The pin wrapssel of BYTE 1.
1:0	RW	0x0	Field0000 The pin wrapssel of BYTE 0.

**DDRPHY\_REG50**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 The low 8 bits of CMD and DQ PLL Feedback divide parameter setting register.

**DDRPHY\_REG51**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:1	RW	0x03	Field0001 Reserved.
0	RW	0x0	Field0000 The bit[9] of CMD and DQ PLL Feedbackdivide. The feedback_divide of PLL = (REG51[0],REG50[7:0]).

**DDRPHY\_REG52**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x2	Field0001 Reserved.
4:0	RW	0x01	Field0000 The CMD and DQ PLL Pre-divide parameter setting register.

**DDRPHY\_REG53**

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	Field0002 The CMD and DQ PLL Post-divide parameter setting register.
4	RO	0x0	reserved
3	RW	0x1	Field0001 CMD and DQ PLL power down. Set to 1'b0 to enable the PLL.
2:0	RO	0x0	reserved

**DDRPHY\_REG57**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x8c	Field0000 reg_phy_trfc The value is Trfc/dfi_clk1x.

**DDRPHY\_REG60**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	Field0007 Reserved.
6	RW	0x1	Field0006 The gating control signal of 1x clock of PHY. Low is valid.
5	RW	0x0	Field0005 The low power disable signal. When high this signal, it will ignore the signals of dfi low power interface.
4	RW	0x1	Field0004 The deep low power mode enable signal. 1'b1: Enable the deep low power. 1'b0: Disable the deep low power.
3	RW	0x0	Field0003 Reserved. Please keep the default value.
2	RW	0x0	Field0002 The power down signal of VREF for Low 16bits when enable the bypass mode of the VREF control.
1	RW	0x0	Field0001 The power down signal of VREF for High 16bits when enable the bypass mode of the VREF control.
0	RW	0x1	Field0000 Disable the bypass mode of the VREF control. 1'b1: Using auto mode the disable VREF. 1'b0: Using the register REG16[2:1] to disable the VREF.

**DDRPHY\_REG61**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	Field0001 reg_max_refi_cnt It means how many auto refresh cmd can be accumulated at one time.the maximum is 8,and the larger the value ,the less time training takes if you set reg_phy_refresh_en to 1'b1.

Bit	Attr	Reset Value	Description
3:0	RW	0x9	Field0000 Configure the low power mode threshold. When the dfi_lp_wakeup ≤ threshold, it will go into the normal low power mode; when dfi_lp_wakeup > threshold, it will go into the deep low power mode.

**DDRPHY\_REG62**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x1	Field0006 Adjust the timing from disable the IO to disable the clock when begin the low power flow.
5	RW	0x1	Field0005 Choose the control mode of the DQ clock path when in low power mode. 1'b1: Auto mode. 1'b0: Bypass mode. Use the register REG0[1] to control.
4	RW	0x1	Field0004 Choose the control mode of the reset of the digital core. 1'b1: Auto mode. 1'b0: Not reset.
3	RW	0x1	Field0003 Choose the control mode of the clock tree of the pll. 1'b1: Auto mode. 1'b0: Not close.
2	RW	0x1	Field0002 Choose the control mode of the clock of the digital core. 1'b1: Auto mode. 1'b0: Not close.
1	RW	0x1	Field0001 Choose the control mode of the IO. 1'b1: Auto mode. 1'b0: Not close.
0	RW	0x1	Field0000 Choose the power down mode of the PLL. 1'b1: Auto mode. 1'b0: Not power down.

**DDRPHY\_REG63**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x88	Field0000 Reserved. Please keep the default value.

**DDRPHY\_REG64**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x13	Field0000 Reserved. Please keep the default value.

**DDRPHY\_REG65**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	Field0001 The response timing when detect the dfi_lp_req is high. Unit: dfi_clk1x.
3:0	RW	0x6	Field0000 The response timing when high the dfi_lp_ack. Unit: dfi_clk1x.

**DDRPHY\_REG66**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	Field0006 The clean signal of zqcalib module. High is valid.
5	RW	0x0	Field0005 The enable signal of zqcalib function. Related register REG5B.
4	RW	0x0	Field0004 The bypass enable of zqcalib function.
3	RW	0x0	Field0003 Reserved.
2:1	RW	0x0	Field0001 Choose the current zqcalib mode when enable the zqcalib function. 2'b00: Driver Pull-Down zqcalib mode. 2'b01: Drive Pull-Up zqcalib mode. 2'b10: ODT Pull-Down zqcalib mode. 2'b11: ODT Pull-Up zqcalib mode.
0	RW	0x1	Field0000 The power down signal of zqcalib module when enable the zqcalib function. 1'b1: Power down mode. 1'b0: Normal work mode.

**DDRPHY\_REG67**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0e	Field0000 The driver pull-down value when enable the zqcalib bypass function.

**DDRPHY\_REG68**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0e	Field0000 The driver pull-up value when enable the zqcalib bypass function.

**DDRPHY\_REG69**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x07	Field0000 The odt pull-down value when enable the zqcalib bypass function.

**DDRPHY\_REG6A**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x07	Field0000 The odt pull-up value when enable the zqcalib bypass function.

**DDRPHY\_REG6B**

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0xff	Field0000 Reserved. Please keep the default value.

**DDRPHY\_REG6C**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0xff	Field0000 Reserved. Please keep the default value.

**DDRPHY\_REG6D**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved



Bit	Attr	Reset Value	Description
7:0	RW	0x00	Field0000 Reserved. Please keep the default value.

**DDRPHY\_REG6E**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	Field0000 reg_phy_trefi[7:0] The value is Trefi/dfi_clk1x.

**DDRPHY\_REG6F**

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x09	Field0000 reg_phy_trfc The value is Trfc/dfi_clk1x.

**DDRPHY\_REG70**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	Field0005 Choose the check value of the read train. 1'b0: Use the fix mode. DDR3 = 8'b10101010 LPDDR3 = 16'hcc55 LPDDR4 = MR#40,MR#32 DDR4 = 8'haa/8'hcc/8'hf0/8'h00 1'b1: Use the register to configure.
6	RW	0x0	Field0007 reg_rd_train_predef_en The enable signal of the read predef training, predefine Mode. 1'b1: Enable the predef train of the read train. 1'b0: Exit the predef train of the read train
5	RW	0x0	Field0006 reg_phy_refresh_en When you want to enable phy auto refresh function in read training, you should set this to 1 at frist.
4	RW	0x0	Field0004 Set to 1'b1 to enable the frequency fast change function for Read train result switch. When enable this function, PHY will choose the auto read train result according to the frequency point setting (REGC[3:2]).

Bit	Attr	Reset Value	Description
3	RW	0x0	Field0003 The enable signal to setting the DQS scan range using the register. 1'b1: Enable to use the register to set the DQS scan range. 1'b0: Use the default DQS scan range[0~6'h3f].
2	RW	0x0	Field0002 The enable signal of the DQS Scan. 1'b1: The auto read train will complete the DQ perbit skew train and DQS-DQ Eye train. 1'b0: The auto read train will only complete the DQ perbit skew train.
1	RW	0x0	Field0001 The enable signal of the read training Auto Mode. 1'b1: Enable the auto train of the read train. 1'b0: Exit the auto train of the read train.
0	RW	0x0	Field0000 Choose the mode of the read train. 1'b1: Choose the read train auto mode. 1'b0: Choose the read train bypass mode.

**DDRPHY\_REG71**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	Field0002 Choose the rank of the read train. 2'b01: Choose Rank0. 2'b10: Choose Rank1.
5	RO	0x0	reserved
4:2	RW	0x2	Field0003 reg_train_vref_en (reuse for rd perdef training and wr training ) The enable signal of the vref training, predefine Mode. 1'b1: Enable the vref train of the read train. 1'b0: Exit the vref train of the read train.
1	RW	0x0	Field0001 reg_bypass_rd_train_cmd_start_en Generate the read train command when enable bypass read training mode. High pulse valid.
0	RW	0x0	Field0000 reg_bypass_rd_train_en Enable the bypass read train function. 1'b1: Enable the read train bypass mode. 1'b0: Disable the read train bypass mode.

**DDRPHY\_REG72**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x55	Field0000 The load mode value of MR15 when do the read train of LPDDR4.

**DDRPHY\_REG73**

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x55	Field0000 The load mode value of MR20 when do the read train of LPDDR4.

**DDRPHY\_REG74**

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 The load mode value of MR32 when do the read train of LPDDR4.

**DDRPHY\_REG75**

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 The load mode value of MR40 when do the read train of LPDDR4.

**DDRPHY\_REG76**

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x06	Field0000 reg_cha_cat_cs_check_value The check pattern of cs train mode for channel A.

**DDRPHY\_REG77**

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x06	Field0000 reg_chb_cat_cs_check_value The check pattern of cs train mode for channel B.

**DDRPHY\_REG78**

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x15	Field0000 reg_cha_cat_ca_check_value The check pattern of ca train mode for channel A.

**DDRPHY\_REG79**

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x15	Field0000 reg_chb_cat_ca_check_value The check pattern of ca train mode for channel B.

**DDRPHY\_REG7A**

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	Field0007 Set to 1'b1 to enable the frequency fast change function for Write Train result switch. When enable this function, PHY will choose the auto Write Train result according to the frequency point setting (REGC[3:2]).
6	RW	0x0	Field0006 DBI enable function of DDR4. 1'b1: Enable the DBI function. 1'b0: Disable the DBI function.
5	RW	0x0	Field0005 The wr train fsm clear signal. 1'b1: Reset the write train fsm. 1'b0: Keep the current state.
4	RW	0x0	Field0004 Choose the DQS default value when enable the write train( The DQS scan mode is disabled). 1'b0: Use the write-leveling value. 1'b1: Use the register to choose the default value.
3	RW	0x0	Field0003 The enable signal to setting the DQS scan range using the register. 1'b1: Enable to use the register to set the DQS scan range. 1'b0: Use the default DQS scan range [0~6'h3f].
2	RW	0x0	Field0002 The enable signal of the DQS Scan. When this bit set to "1", it will enable adjust the DQS to find the best window of the DQ. Only used for debug, because it will change the write-leveling result if the user enable the write leveling function.

Bit	Attr	Reset Value	Description
1	RW	0x0	Field0001 The enable signal of the write training Auto Mode. 1'b1: Enable the auto train of the read train. 1'b0: Exit the auto train of the read train.
0	RW	0x0	Field0000 Choose the mode of the write train. 1'b1: Choose the write train auto mode. 1'b0: Choose the write train bypass mode.

**DDRPHY\_REG7B**

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 The bit[7:0] of col address for write/read operation in DDR3/4 and LPDDR3 write training mode.

**DDRPHY\_REG7C**

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	Field0002 Choose the rank of the write train. 2'b01: Choose Rank0. 2'b10: Choose Rank1.
5	RW	0x1	Field0005 Reserved.
4:2	RW	0x0	Field0001 The bit[2:0] of bank address for write/read operation in DDR3/4 and LPDDR3 write training mode.
1:0	RW	0x0	Field0000 The bit[9:8] of col address for write/read operation in DDR3/4 and LPDDR3 write training mode.

**DDRPHY\_REG7D**

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	Field0000 The bit[7:0] of row address for write/read operation in DDR3/4 and LPDDR3 write training mode.

**DDRPHY\_REG7E**

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 The bit[15:8] of row address for write/read operation in DDR3/4 and LPDDR3 write training mode.

**DDRPHY\_REG90**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x02	Field003 Reserved.
2	RW	0x0	Field002 CMD and DQ PLL lock flag. High means PLL is lock.
1:0	RW	0x2	Field000 Reserved.

**DDRPHY\_REG91**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	Field0002 The error flag of the calibration. High is valid.
4	RO	0x0	Field0001 The end flag of the calibration flow. High means valid. When this bit change "1'b1". The complete flag of each channel will set to high, or it will have errors.
3:0	RO	0x0	Field0000 The calibration complete signal. 4'h0: The complete flag of left(low 8 bit) channel A. High valid. 4'h1: The complete flag of right(right 8 bit) channel A. High valid. 4'h2: The complete flag of left channel B. High valid. 4'h3: The complete flag of right channel B. High valid.

**DDRPHY\_REG92**

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	Field0004 Train_all_step_done (reuse for rd perdef training and wr training). This value equal to 1'b1 means training all step done .
6	RO	0x0	Field0003 Train_step1_delay_done (reuse for rd perdef training and wr training). This value equal to 1'b1 means step1 done.

Bit	Attr	Reset Value	Description
5	RO	0x0	Field0002 Train_step2_delay_done (reuse for rd perdef training and wr training). This value equal to 1'b1 means step2 done.
4	RO	0x0	Field0001 Train_step3_delay_done (reuse for rd perdef training and wr training). This value equal to 1'b1 means step3 done.
3:0	RO	0x0	Field0000 The Write leveling complete signal. 4'h0: The complete flag of left channel A. High valid. 4'h1: The complete flag of right channel A. High valid. 4'h2: The complete flag of left channel B. High valid. 4'h3: The complete flag of right channel B. High valid.

**DDRPHY\_REG93**

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	Field0001 reg_train_true_done When this reg's value equal to 1'b1, The read train done and refresh done, only used during mpr/mpc read train.
6:0	RO	0x00	reserved

**DDRPHY\_REG94**

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	Field0004 The bist result of the bist_reg mode. High means error.
3	RO	0x0	Field0003 The bist result of the command. High means error.
2	RO	0x0	Field0002 The bist result of the dm. High means error.
1	RO	0x0	Field0001 The bist result of the dq channel. High means error.
0	RO	0x0	Field0000 The bist complete flag. High valid.

**DDRPHY\_REG95**

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	Field0000 The complete flag of ZQCALIB.

**DDRPHY\_REG96**

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RO	0x00	Field0000 The calibration value of 40 Ohm pull-down resistance of the driver.

**DDRPHY\_REG97**

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RO	0x00	Field0000 The calibration value of 40 Ohm pull-up resistance of the driver.

**DDRPHY\_REG98**

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RO	0x00	Field0000 The calibration value of 160 Ohm pull-down resistance of the ODT.

**DDRPHY\_REG99**

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RO	0x00	Field0000 The calibration value of 160 Ohm pull-up resistance of the ODT.

**DDRPHY\_REG9A**

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5:0	RO	0x00	Field0000 When enable the command bus train bypass mode, after send the command bus train command though reg_cat_bp_cmd_send(REG10[3]), this register shows the back value of channel A.

**DDRPHY\_REG9B**

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved



Bit	Attr	Reset Value	Description
5:0	RO	0x00	Field0000 When enable the command bus train bypass mode, after send the command bus train command though reg_cat_bp_cmd_send(REG10[3]), this register shows the back value of channel B.

**DDRPHY REG105**

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	Field0000 This is used to control the RAM_VREF. $RAM\_VREF = (VDDQ/256)*REG105$ .

**DDRPHY REG118**

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_a_l_vref1_margsel[7:0] The register to control the PHY's vref(BYTE0).

**DDRPHY REG128**

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	Field0000 reg_a_r_vref1_margsel[7:0] The register to control the PHY's vref(BYTE1).

**DDRPHY REG138**

Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	Field0000 reg_b_l_vref1_margsel[7:0] The register to control the PHY's vref(BYTE2).

**DDRPHY REG148**

Address: Operational Base + offset (0x0520)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x80	Field0000 reg_b_r_vref1_margsel[7:0] The register to control the PHY's vref(BYTE3).

**DDRPHY\_REG150**

Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a0_invdelaysel Command per bit de-skew for A0 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG151**

Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a1_invdelaysel Command per bit de-skew for A1 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG152**

Address: Operational Base + offset (0x0548)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a2_invdelaysel Command per bit de-skew for A2 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG153**

Address: Operational Base + offset (0x054C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a3_invdelaysel Command per bit de-skew for A3 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG154**

Address: Operational Base + offset (0x0550)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a4_invdelayssel Command per bit de-skew for A4 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG155**

Address: Operational Base + offset (0x0554)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a5_invdelayssel Command per bit de-skew for A5 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG156**

Address: Operational Base + offset (0x0558)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a6_invdelayssel Command per bit de-skew for A6 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG157**

Address: Operational Base + offset (0x055C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a7_invdelayssel Command per bit de-skew for A7 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG158**

Address: Operational Base + offset (0x0560)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x07	Field0000 reg_a8_invdelayssel Command per bit de-skew for A8 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG159**

Address: Operational Base + offset (0x0564)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a9_invdelayssel Command per bit de-skew for A9 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG15A**

Address: Operational Base + offset (0x0568)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a10_invdelayssel Command per bit de-skew for A10 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG15B**

Address: Operational Base + offset (0x056C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a11_invdelayssel Command per bit de-skew for A11 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG15C**

Address: Operational Base + offset (0x0570)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_a12_invdelayssel Command per bit de-skew for A12 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG15D**

Address: Operational Base + offset (0x0574)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5:0	RW	0x07	Field0000 reg_a13_invdelayssel Command per bit de-skew for A13 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG15E**

Address: Operational Base + offset (0x0578)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5:0	RW	0x07	Field0000 reg_a14_invdelayssel Command per bit de-skew for A14 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG15F**

Address: Operational Base + offset (0x057C)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5:0	RW	0x07	Field0000 reg_a15_invdelayssel Command per bit de-skew for A15 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG160**

Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5:0	RW	0x07	Field0000 reg_a16_invdelayssel Command per bit de-skew for A16 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG161**

Address: Operational Base + offset (0x0584)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x07	Field0000 reg_a17_invdelayssel Command per bit de-skew for A17 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG162**

Address: Operational Base + offset (0x0588)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_ba0_invdelayssel Command per bit de-skew for BA0 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG163**

Address: Operational Base + offset (0x058C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_ba1_invdelayssel Command per bit de-skew for BA1 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG164**

Address: Operational Base + offset (0x0590)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_bg0_invdelayssel Command per bit de-skew for BG0 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG165**

Address: Operational Base + offset (0x0594)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_bg1_invdelayssel Command per bit de-skew for BG1 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG166**

Address: Operational Base + offset (0x0598)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_cke_invdelaysel Command per bit de-skew for CKE pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG167**

Address: Operational Base + offset (0x059C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_ck_invdelaysel Command per bit de-skew for CK pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG168**

Address: Operational Base + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_ckb_invdelaysel Command per bit de-skew for CKB pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG169**

Address: Operational Base + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_csb0_invdelaysel Command per bit de-skew for CSB0 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG16A**

Address: Operational Base + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x07	Field0000 reg_odt0_invdelaysel Command per bit de-skew for ODT0 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG16B**

Address: Operational Base + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_resetrn_invdelaysel Command per bit de-skew for RESETN pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG16C**

Address: Operational Base + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_actn_invdelaysel Command per bit de-skew for ACTN pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG16D**

Address: Operational Base + offset (0x05B4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_cke1_invdelaysel Not used.

**DDRPHY REG16E**

Address: Operational Base + offset (0x05B8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_csb1_invdelaysel Command per bit de-skew for CSB1 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY REG16F**



Address: Operational Base + offset (0x05BC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	Field0000 reg_odt1_invdelaysel Command per bit de-skew for ODT1 pad of DDR4. For other kind of SDRAM command per bit de-skew control, please refer to the default command IO map.

**DDRPHY\_REG230**

Address: Operational Base + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1f	Field0000 reg_l_rd_train_dqs_default[5:0] This register is used to control the start phase of the RX DQS when enable the read training for low 8 bits.

**DDRPHY\_REG231**

Address: Operational Base + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x3f	Field0000 Choose the max value of the A_DQS[0] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG232**

Address: Operational Base + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	Field0000 Choose the min value of the A_DQS[0] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG235**

Address: Operational Base + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x3f	Field0000 Choose the max value of the A_DQS[1] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG236**

Address: Operational Base + offset (0x08D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	Field0000 Choose the min value of the A_DQS[1] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG23C**

Address: Operational Base + offset (0x08F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0x00	Field0000 Channel A low 8 bits: the vref training result of rx vref's maximum value.

**DDRPHY\_REG240**

Address: Operational Base + offset (0x0900)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	Field0003 Channel A high 8 bits: Read training done.
2	RO	0x0	Field0002 Channel A low 8 bits: Read training done.
1	RO	0x0	Field0001 Channel A high 8 bits: Read training error.
0	RO	0x0	Field0000 Channel A low 8 bits: Read training error.

**DDRPHY\_REG2B0**

Address: Operational Base + offset (0x0AC0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1f	Field0000 reg_l_rd_train_dqs_default[5:0] This register is used to control the start phase of the RX DQS when enable the read training for low 8 bits.

**DDRPHY\_REG2B1**

Address: Operational Base + offset (0x0AC4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x3f	Field0000 Choose the max value of the B_DQS[0] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG2B2**

Address: Operational Base + offset (0x0AC8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	Field0000 Choose the min value of the B_DQS[0] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG2B5**

Address: Operational Base + offset (0x0AD4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x3f	Field0000 Choose the max value of the B_DQS[1] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG2B6**

Address: Operational Base + offset (0x0AD8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	Field0000 Choose the min value of the B_DQS[1] scan range when REG70[3] set to 1'b1.

**DDRPHY\_REG330**

Address: Operational Base + offset (0x0CC0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0x5a	Field0000 dq0_train_ckeck_data_value0[7:0] (reuse for rd perdefine training and wr training) The first BL8 data(dq0/dq8/dq16/dq24) write to SDRAM.

**DDRPHY\_REG331**

Address: Operational Base + offset (0x0CC4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0xa5	Field0000 dq0_train_ckeck_data_value1[7:0] (reuse for rd perdefine training and wr training) The second BL8 data(dq0/dq8/dq16/dq24) write to SDRAM.

**DDRPHY\_REG332**

Address: Operational Base + offset (0x0CC8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xc3	Field0000 dq0_train_ckeck_data_value2[7:0] (reuse for rd perdefine training and wr training) The third BL8 data(dq0/dq8/dq16/dq24) write to SDRAM.

**DDRPHY\_REG333**

Address: Operational Base + offset (0x0CCC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 dq0_train_ckeck_data_value3[7:0] (reuse for rd perdefine training and wr training) The fourth BL8 data(dq0/dq8/dq16/dq24) write to SDRAM.

**DDRPHY\_REG33A**

Address: Operational Base + offset (0x0CE8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xa5	Field0000 dq1_train_ckeck_data_value0[7:0] (reuse for rd perdefine training and wr training) The first BL8 data(dq1/dq9/dq17/dq25) write to SDRAM.

**DDRPHY\_REG33B**

Address: Operational Base + offset (0x0CEC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq1_train_ckeck_data_value1[7:0] (reuse for rd perdefine training and wr training) The second BL8 data(dq1/dq9/dq17/dq25) write to SDRAM.

**DDRPHY\_REG33C**

Address: Operational Base + offset (0x0CF0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 dq1_train_ckeck_data_value2[7:0] (reuse for rd perdefine training and wr training) The third BL8 data(dq1/dq9/dq17/dq25) write to SDRAM.

**DDRPHY\_REG33D**

Address: Operational Base + offset (0x0CF4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xc3	Field0000 dq1_train_ckeck_data_value3[7:0] (reuse for rd perdefine training and wr training) The fourth BL8 data(dq1/dq9/dq17/dq25) write to SDRAM.

**DDRPHY\_REG344**

Address: Operational Base + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq2_train_ckeck_data_value0[7:0] (reuse for rd perdefine training and wr training) The first BL8 data(dq2/dq10/dq18/dq26) write to SDRAM.

**DDRPHY\_REG345**

Address: Operational Base + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xa5	Field0000 dq2_train_ckeck_data_value1[7:0] (reuse for rd perdefine training and wr training) The second BL8 data(dq2/dq10/dq18/dq26) write to SDRAM.

**DDRPHY\_REG346**

Address: Operational Base + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc3	Field0000 dq2_train_ckeck_data_value2[7:0] (reuse for rd perdefine training and wr training) The third BL8 data(dq2/dq10/dq18/dq26) write to SDRAM.

**DDRPHY\_REG347**

Address: Operational Base + offset (0x0D1C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 dq2_train_ckeck_data_value3[7:0] (reuse for rd perdefine training and wr training) The fourth BL8 data(dq2/dq10/dq18/dq26) write to SDRAM.

**DDRPHY\_REG34E**

Address: Operational Base + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xa5	Field0000 dq3_train_ckeck_data_value0[7:0] (reuse for rd perdefine training and wr training) The first BL8 data(dq3/dq11/dq19/dq27) write to SDRAM.

**DDRPHY\_REG34F**

Address: Operational Base + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq3_train_ckeck_data_value1[7:0] (reuse for rd perdefine training and wr training) The second BL8 data(dq3/dq11/dq19/dq27) write to SDRAM.

**DDRPHY\_REG350**

Address: Operational Base + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 dq3_train_ckeck_data_value2[7:0] (reuse for rd predefine training and wr training) The third BL8 data(dq3/dq11/dq19/dq27) write to SDRAM.

**DDRPHY\_REG351**

Address: Operational Base + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc3	Field0000 dq3_train_ckeck_data_value3[7:0] (reuse for rd predefine training and wr training) The fourth BL8 data(dq3/dq11/dq19/dq27) write to SDRAM.

**DDRPHY\_REG358**

Address: Operational Base + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq4_train_ckeck_data_value0[7:0] (reuse for rd predefine training and wr training) The first BL8 data(dq4/dq12/dq20/dq28) write to SDRAM.

**DDRPHY\_REG359**

Address: Operational Base + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xa5	Field0000 dq4_train_ckeck_data_value1[7:0] (reuse for rd predefine training and wr training) The second BL8 data(dq4/dq12/dq20/dq28) write to SDRAM.

**DDRPHY\_REG35A**

Address: Operational Base + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc3	Field0000 dq4_train_ckeck_data_value2[7:0] (reuse for rd predefine training and wr training) The second BL8 data(dq4/dq12/dq20/dq28) write to SDRAM.

**DDRPHY\_REG35B**

Address: Operational Base + offset (0x0D6C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 dq4_train_ckeck_data_value3[7:0] (reuse for rd predefine training and wr training) The third BL8 data(dq4/dq12/dq20/dq28) write to SDRAM.

**DDRPHY\_REG362**

Address: Operational Base + offset (0x0D88)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xa5	Field0000 dq5_train_ckeck_data_value0[7:0] (reuse for rd predefine training and wr training) The first BL8 data(dq5/dq13/dq21/dq29) write to SDRAM.

**DDRPHY\_REG363**

Address: Operational Base + offset (0x0D8C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq5_train_ckeck_data_value1[7:0] (reuse for rd predefine training and wr training) The second BL8 data(dq5/dq13/dq21/dq29) write to SDRAM.

**DDRPHY\_REG364**

Address: Operational Base + offset (0x0D90)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x3c	Field0000 dq5_train_ckeck_data_value2[7:0] (reuse for rd predefine training and wr training) The third BL8 data(dq5/dq13/dq21/dq29) write to SDRAM.

**DDRPHY\_REG365**

Address: Operational Base + offset (0x0D94)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc3	Field0000 dq5_train_ckeck_data_value3[7:0] (reuse for rd predefine training and wr training) The fourth BL8 data(dq5/dq13/dq21/dq29) write to SDRAM.

**DDRPHY\_REG36C**

Address: Operational Base + offset (0x0DB0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq6_train_ckeck_data_value0[7:0] (reuse for rd predefine training and wr training) The first BL8 data(dq6/dq14/dq22/dq30) write to SDRAM.

**DDRPHY\_REG36D**

Address: Operational Base + offset (0x0DB4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xa5	Field0000 dq6_train_ckeck_data_value1[7:0] (reuse for rd predefine training and wr training) The second BL8 data(dq6/dq14/dq22/dq30) write to SDRAM.

**DDRPHY\_REG36E**

Address: Operational Base + offset (0x0DB8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc3	Field0000 dq6_train_ckeck_data_value2[7:0] (reuse for rd predefine training and wr training) The third BL8 data(dq6/dq14/dq22/dq30) write to SDRAM.

**DDRPHY\_REG36F**

Address: Operational Base + offset (0x0DBC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved



Bit	Attr	Reset Value	Description
7:0	RW	0x3c	Field0000 dq6_train_ckeck_data_value3[7:0] (reuse for rd predefine training and wr training) The fourth BL8 data(dq6/dq14/dq22/dq30) write to SDRAM.

**DDRPHY\_REG376**

Address: Operational Base + offset (0x0DD8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xa5	Field0000 dq7_train_ckeck_data_value0[7:0] (reuse for rd predefine training and wr training) The first BL8 data(dq7/dq15/dq23/dq31) write to SDRAM.

**DDRPHY\_REG377**

Address: Operational Base + offset (0x0DDC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	Field0000 dq7_train_ckeck_data_value1[7:0] (reuse for rd predefine training and wr training) The second BL8 data(dq7/dq15/dq23/dq31) write to SDRAM.

**DDRPHY\_REG378**

Address: Operational Base + offset (0x0DE0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3c	Field0000 dq7_train_ckeck_data_value2[7:0] (reuse for rd predefine training and wr training) The third BL8 data(dq7/dq15/dq23/dq31) write to SDRAM.

**DDRPHY\_REG379**

Address: Operational Base + offset (0x0DE4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc3	Field0000 dq7_train_ckeck_data_value3[7:0] (reuse for rd predefine training and wr training) The fourth BL8 data(dq7/dq15/dq23/dq31) write to SDRAM.

**DDRPHY\_REG380**

Address: Operational Base + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x40	Field0000 reg_rdtrain_wait_vref_valid_cnt[7:0] When set a new rx vref value, we should wait 800ns ,then it works. So the reg's value = 800ns/dfi_1xclk

**DDRPHY\_REG381**

Address: Operational Base + offset (0x0E04)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x08	Field0001 reg_train_vref_step_max (reuse for rd predefinetraining and wr training ) How many step at a time, when A rough vref scanning.
2	RO	0x0	reserved
1:0	RW	0x1	Field0000 reg_rdtrain_wait_vref_valid_cnt[9:8] When set a new rx vref value, we should wait 800ns ,then it works. So the reg's value = 800ns/dfi_1xclk.

**DDRPHY\_REG382**

Address: Operational Base + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x21	Field0000 reg_train_vref_step_min (reuse for rd predefine training and wr training ) How many step at a time, when A fine vref scanning.

**DDRPHY\_REG387**

Address: Operational Base + offset (0x0E1C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x06	Field0000 CL value[FSP1] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM RL. Note: When the phy choose the DDRn mode, RL = CL+AL.

**DDRPHY\_REG388**

Address: Operational Base + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	Field0000 AL value[FSP1] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM AL. When the phy choose the LPDDRn mode, this value should keep 5'h0.

**DDRPHY\_REG389**

Address: Operational Base + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	Field0000 CWL value[FSP1] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CWL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM WL. When the phy choose the DDRn mode, WL=CWL+AL.

**DDRPHY\_REG38A**

Address: Operational Base + offset (0x0E28)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x06	Field0000 CL value[FSP2] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM RL.

**DDRPHY\_REG38B**

Address: Operational Base + offset (0x0E2C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	Field0000 AL value[FSP2] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAMAL. When the phy choose the LPDDRn mode, this value should keep 5'h0.

**DDRPHY\_REG38C**

Address: Operational Base + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	Field0000 CWL value[FSP2] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CWL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM WL. When the phy choose the DDRn mode, WL=CWL+AL.

**DDRPHY REG38D**

Address: Operational Base + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x06	Field0000 CL value[FSP3] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM RL. Note: When the phy choose the DDRn mode, RL = CL+AL.

**DDRPHY REG38E**

Address: Operational Base + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	Field0000 AL value[FSP3] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAMAL. When the phy choose the LPDDRn mode, this value should keep 5'h0.

**DDRPHY REG38F**

Address: Operational Base + offset (0x0E3C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	Field0000 CWL value[FSP3] When the phy choose the DDRn mode, this value should keep the same value to the value of the SDRAM CWL. When the phy choose the LPDDRn mode, this value should keep the same value to the value of the SDRAM WL. When the phy choose the DDRn mode, WL=CWL+AL.

**DDRPHY REG3A0**

Address: Operational Base + offset (0x0E80)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CSB0_A.

**DDRPHY\_REG3A1**

Address: Operational Base + offset (0x0E84)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CSB1_A.

**DDRPHY\_REG3A2**

Address: Operational Base + offset (0x0E88)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA0_A(Rank0).

**DDRPHY\_REG3A3**

Address: Operational Base + offset (0x0E8C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA1_A(Rank0).

**DDRPHY\_REG3A4**

Address: Operational Base + offset (0x0E90)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA2_A(Rank0).

**DDRPHY\_REG3A5**

Address: Operational Base + offset (0x0E94)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA3_A(Rank0).

**DDRPHY\_REG3A6**

Address: Operational Base + offset (0x0E98)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA4_A(Rank0).

**DDRPHY\_REG3A7**

Address: Operational Base + offset (0x0E9C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA5_A(Rank0).

**DDRPHY\_REG3A8**

Address: Operational Base + offset (0x0EA0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA0_A(Rank1).

**DDRPHY\_REG3A9**

Address: Operational Base + offset (0x0EA4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA1_A(Rank1).

**DDRPHY\_REG3AA**

Address: Operational Base + offset (0x0EA8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA2_A(Rank1).

**DDRPHY\_REG3AB**

Address: Operational Base + offset (0x0EAC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA3_A(Rank1).

**DDRPHY\_REG3AC**

Address: Operational Base + offset (0x0EB0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA4_A(Rank1).

**DDRPHY\_REG3AD**

Address: Operational Base + offset (0x0EB4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA5_A(Rank1).

**DDRPHY\_REG3AE**

Address: Operational Base + offset (0x0EB8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min CA_VREF command bus train value of Channel A( Rank0).

**DDRPHY\_REG3AF**

Address: Operational Base + offset (0x0EBC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min CA_VREF command bus train value of Channel A( Rank1).

**DDRPHY\_REG3B0**

Address: Operational Base + offset (0x0EC0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CSB0_A.

**DDRPHY\_REG3B1**

Address: Operational Base + offset (0x0EC4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CSB1_A.

**DDRPHY REG3B2**

Address: Operational Base + offset (0x0EC8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA0_A(Rank0).

**DDRPHY REG3B3**

Address: Operational Base + offset (0x0ECC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA1_A(Rank0).

**DDRPHY REG3B4**

Address: Operational Base + offset (0x0ED0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA2_A(Rank0).

**DDRPHY REG3B5**

Address: Operational Base + offset (0x0ED4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA3_A(Rank0).

**DDRPHY REG3B6**

Address: Operational Base + offset (0x0ED8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA4_A(Rank0).

**DDRPHY REG3B7**

Address: Operational Base + offset (0x0EDC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved



Bit	Attr	Reset Value	Description
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA5_A(Rank0).

**DDRPHY REG3B8**

Address: Operational Base + offset (0x0EE0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA0_A(Rank1).

**DDRPHY REG3B9**

Address: Operational Base + offset (0x0EE4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA1_A(Rank1).

**DDRPHY REG3BA**

Address: Operational Base + offset (0x0EE8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA2_A(Rank1).

**DDRPHY REG3BB**

Address: Operational Base + offset (0x0EEC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA3_A(Rank1).

**DDRPHY REG3BC**

Address: Operational Base + offset (0x0EF0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA4_A(Rank1).

**DDRPHY REG3BD**

Address: Operational Base + offset (0x0EF4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA5_A(Rank1).

**DDRPHY\_REG3BE**

Address: Operational Base + offset (0x0EF8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max CA_VREF command bus train value of Channel A(Rank0).

**DDRPHY\_REG3BF**

Address: Operational Base + offset (0x0EFC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max CA_VREF command bus train value of Channel A( Rank1).

**DDRPHY\_REG3C0**

Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CSB0_B.

**DDRPHY\_REG3C1**

Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CSB1_B.

**DDRPHY\_REG3C2**

Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA0_B(Rank0).

**DDRPHY\_REG3C3**

Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA1_B(Rank0).

**DDRPHY\_REG3C4**

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA2_B(Rank0).

**DDRPHY\_REG3C5**

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA3_B(Rank0).

**DDRPHY\_REG3C6**

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA4_B(Rank0).

**DDRPHY\_REG3C7**

Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA5_B(Rank0).

**DDRPHY\_REG3C8**

Address: Operational Base + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA0_B(Rank1).

**DDRPHY REG3C9**

Address: Operational Base + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA1_B(Rank1).

**DDRPHY REG3CA**

Address: Operational Base + offset (0x0F28)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA2_B(Rank1).

**DDRPHY REG3CB**

Address: Operational Base + offset (0x0F2C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA3_B(Rank1).

**DDRPHY REG3CC**

Address: Operational Base + offset (0x0F30)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA4_B(Rank1).

**DDRPHY REG3CD**

Address: Operational Base + offset (0x0F34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min per-bit de-skew command bus train value of CA5_B(Rank1).

**DDRPHY REG3CE**

Address: Operational Base + offset (0x0F38)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min CA_VREF command bus train value of Channel A( Rank0).

**DDRPHY\_REG3CF**

Address: Operational Base + offset (0x0F3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The min CA_VREF command bus train value of Channel A( Rank1).

**DDRPHY\_REG3D0**

Address: Operational Base + offset (0x0F40)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CSB0_B.

**DDRPHY\_REG3D1**

Address: Operational Base + offset (0x0F44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CSB1_B.

**DDRPHY\_REG3D2**

Address: Operational Base + offset (0x0F48)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA0_B(Rank0).

**DDRPHY\_REG3D3**

Address: Operational Base + offset (0x0F4C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA1_B(Rank0).

**DDRPHY\_REG3D4**

Address: Operational Base + offset (0x0F50)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	Field0000 The max per-bit de-skew command bus train value of CA2_B(Rank0).

**DDRPHY\_REG3D5**

Address: Operational Base + offset (0x0F54)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA3_B(Rank0).

**DDRPHY\_REG3D6**

Address: Operational Base + offset (0x0F58)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA4_B(Rank0).

**DDRPHY\_REG3D7**

Address: Operational Base + offset (0x0F5C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA5_B(Rank0).

**DDRPHY\_REG3D8**

Address: Operational Base + offset (0x0F60)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA0_B(Rank1).

**DDRPHY\_REG3D9**

Address: Operational Base + offset (0x0F64)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA1_B(Rank1).

**DDRPHY\_REG3DA**

Address: Operational Base + offset (0x0F68)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA2_B(Rank1).

**DDRPHY\_REG3DB**

Address: Operational Base + offset (0x0F6C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA3_B(Rank1).

**DDRPHY\_REG3DC**

Address: Operational Base + offset (0x0F70)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA4_B(Rank1).

**DDRPHY\_REG3DD**

Address: Operational Base + offset (0x0F74)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max per-bit de-skew command bus train value of CA5_B(Rank1).

**DDRPHY\_REG3DE**

Address: Operational Base + offset (0x0F78)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max CA_VREF command bus train value of Channel B( Rank0).

**DDRPHY\_REG3DF**

Address: Operational Base + offset (0x0F7C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	Field0000 The max CA_VREF command bus train value of Channel B( Rank1).

**DDRPHY\_REG3E0**

Address: Operational Base + offset (0x0F80)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved



Bit	Attr	Reset Value	Description
5:0	RO	0x07	<p>Field0000</p> <p>The current perbit skew state of the command bus. Using the reg_cmd_invdelay_sel_sel(reg386[5:0]) to choose the observe command.</p> <p>6'h0: The perbit skew state of the CA0 for channel A(RANK0)</p> <p>6'h1: The perbit skew state of the CA1 for channel A(RANK0)</p> <p>6'h2: The perbit skew state of the CA2 for channel A(RANK0)</p> <p>6'h3: The perbit skew state of the CA3 for channel A(RANK0)</p> <p>6'h4: The perbit skew state of the CA4 for channel A(RANK0)</p> <p>6'h5: The perbit skew state of the CA5 for channel A(RANK0)</p> <p>6'h6: The perbit skew state of the CA0 for channel B(RANK0)</p> <p>6'h7: The perbit skew state of the CA1 for channel B(RANK0)</p> <p>6'h8: The perbit skew state of the CA2 for channel B(RANK0)</p> <p>6'h9: The perbit skew state of the CA3 for channel B(RANK0)</p> <p>6'ha: The perbit skew state of the CA4 for channel B(RANK0)</p> <p>6'hb: The perbit skew state of the CA5 for channel B(RANK0)</p> <p>6'hc: The perbit skew state of the CA0 for channel A(RANK1)</p> <p>6'hd: The perbit skew state of the CA1 for channel A(RANK1)</p> <p>6'he: The perbit skew state of the CA2 for channel A(RANK1)</p> <p>6'hf: The perbit skew state of the CA3 for channel A(RANK1)</p> <p>6'h10: The perbit skew state of the CA4 for channel A(RANK1)</p> <p>6'h11: The perbit skew state of the CA5 for channel A(RANK1)</p> <p>6'h12: The perbit skew state of the CA0 for channel B(RANK1)</p> <p>6'h13: The perbit skew state of the CA1 for channel B(RANK1)</p> <p>6'h14: The perbit skew state of the CA2 for channel B(RANK1)</p> <p>6'h15: The perbit skew state of the CA3 for channel B(RANK1)</p> <p>6'h16: The perbit skew state of the CA4 for channel B(RANK1)</p> <p>6'h17: The perbit skew state of the CA5 for channel B(RANK1)</p> <p>6'h18: The perbit skew state of the CK for channel A</p> <p>6'h19: The perbit skew state of the CKB for channel A</p> <p>6'h1a: The perbit skew state of the CKE0 for channel A</p> <p>6'h1b: The perbit skew state of the CKE1 for channel A</p> <p>6'h1c: The perbit skew state of the CSB0 for channel A</p> <p>6'h1d: The perbit skew state of the CSB1 for channel A</p> <p>6'h1e: The perbit skew state of the ODT0 for channel A</p> <p>6'h1f: The perbit skew state of the ODT1 for channel A</p> <p>6'h20: The perbit skew state of the CK for channel B</p> <p>6'h21: The perbit skew state of the CKB for channel B</p> <p>6'h22: The perbit skew state of the CKE0 for channel B</p> <p>6'h23: The perbit skew state of the CKE1 for channel B</p> <p>6'h24: The perbit skew state of the CSB0 for channel B</p> <p>6'h25: The perbit skew state of the CSB1 for channel B</p> <p>6'h26: The perbit skew state of the ODT0 for channel B</p> <p>6'h27: The perbit skew state of the ODT1 for channel B</p>

### 1.4.3 Registers Summary For DDR Standby

Name	Offset	Size	Reset Value	Description
DDRSTDBY_CON0	0x0000	W	0x00002000	control register0
DDRSTDBY_CON1	0x0004	W	0x00000000	control register1
DDRSTDBY_STATUS0	0x0008	W	0x00000000	status register0

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 1.4.4 Detail Registers Description

#### DDRSTDBY\_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	idle_th Idle threshold time. Measured by clk_ddr_stdby(General is ddrphy4x/4). When the time of both memory scheduler and PCTL in idle status exceed idle_th, it will request PCTL to enter self-refresh.
15:14	RO	0x0	reserved
13	RW	0x1	reserved
12:8	RO	0x00	reserved
7	RW	0x0	msch_gate_en 1'b0: Disable memory scheduler gated 1'b1: Enable memory scheduler gated
6	RW	0x0	ddrphy4x_gate_en 1'b0: Disable ddrphy4x gated 1'b1: Enable ddrphy4x gated
5	RW	0x0	upctl_core_clk_gate_en 1'b0: Disable PCTL core_clk gated 1'b1: Enable PCTL core_clk gated
4	RW	0x0	upctl_aclk_gate_en 1'b0: Disable PCTL aclk gated 1'b1: Enable PCTL aclk gated
3	RO	0x0	reserved
2	RW	0x0	sysack_ext_dis 1'b0: Exit standby mode need to wait assertion of sysack 1'b1: Exit standby mode not need to wait assertion of sysack
1	RW	0x0	ctl_idle_en 1'b0: Disable PCTL idle when DDRSTDBY is enabled. 1'b1: Enable PCTL idle when DDRSTDBY is enabled.
0	RW	0x0	stdby_en 1'b0: Disable DDRSTDBY function 1'b1: Enable DDRSTDBY function

#### DDRSTDBY\_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cg_exit_th Clk gated exit threshold time. Measured by clk_ddr_stdby(General is ddrphy4x/4). If ddrphy4x_gate_en=1, cg_exit_th need consider the dll lock time of ddr phy.
15:0	RW	0x0000	cg_wait_th Clk gated wait threshold time. Measured by clk_ddr_stdby(General is ddrphy4x/4). Set this value to 0x0.

**DDRSTDBY STATUS0**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	sysactive 1'b0: PCTL is idle. 1'b1: PCTL is active.
12	RO	0x0	sysack 1'b0: Acknowledge the request of sysreq enter self-refresh. 1'b1: Acknowledge the request of sysreq exit self-refresh.
11	RO	0x0	sysreq 1'b0: Request PCTL enter self-refresh. 1'b1: Request PCTL exit self-refresh.
10	RO	0x0	upctl_idle 1'b0: PCTL is active. 1'b1: PCTL Controller is idle.
9	RO	0x0	pwract 1'b0: Memory scheduler is not active. 1'b1: Memory scheduler is active.
8	RO	0x0	ddrstdby_gate 1'b0: DDRSTDBY global gated is disabled. 1'b1: DDRSTDBY global gated is enabled.
7	RO	0x0	stdby_en 1'b0: DDRSTDBY is disabled. 1'b1: DDRSTDBY is enabled.
6:0	RO	0x00	state 7'b0000001: ST_NORMAL 7'b0000010: ST_STDBY_WAIT_EN 7'b0000100: ST_STDBY_SR_ENTRY 7'b0001000: ST_STDBY_WAIT 7'b0010000: ST_STDBY 7'b0100000: ST_STDBY2 7'b1000000: ST_STDBY_SR_EXIT

**1.4.5 Registers Summary For DDR Monitor**

Name	Offset	Size	Reset Value	Description
<u>DDRMON_IP_VERSION</u>	0x0000	W	0x00000023	DDR Monitor IP Version
<u>DDRMON_CTRL</u>	0x0004	W	0x00000008	DDR Monitor Control Register
<u>DDRMON_INT_STATUS</u>	0x0008	W	0x00000000	Interrupt Status
<u>DDRMON_INT_MASK</u>	0x000c	W	0x00007FFF	Interrupt mask control
<u>DDRMON_TIMER_COUNT</u>	0x0010	W	0x00000000	The DFI Timer Threshold
<u>DDRMON_FLOOR_NUMBER</u>	0x0014	W	0x00000000	The Low Threshold in the Comparison of DDR Access
<u>DDRMON_TOP_NUMBER</u>	0x0018	W	0x00000000	The High Threshold in the Comparison of DDR Access
<u>DDRMON_DFI_ACT_NUM</u>	0x001c	W	0x00000000	DFI Active Command Number
<u>DDRMON_DFI_WR_NUM</u>	0x0020	W	0x00000000	DFI Write Command Number
<u>DDRMON_DFI_RD_NUM</u>	0x0024	W	0x00000000	DFI Read Command Number
<u>DDRMON_COUNT_NUM</u>	0x0028	W	0x00000000	Timer Count Number
<u>DDRMON_DFI_ACCESS_NUM</u>	0x002c	W	0x00000000	DFI Read And Write Command Number
<u>DDRMON_TOP_LP_NUMBER</u>	0x0030	W	0x00000000	The High Threshold In The Comparison Of DDR Cke Low

Name	Offset	Size	Reset Value	Description
<u>DDRMON_FLOOR_LP_NUMBER</u>	0x0034	W	0x00000000	The Low Threshold In The Comparison Of DDR Cke Low
<u>DDRMON_DFI_SREX_NUM</u>	0x0038	W	0x00000000	Number Of Cke Low For DFI Self-refresh
<u>DDRMON_DFI_PDEX_NUM</u>	0x003c	W	0x00000000	Number Of Cke Low For DFI Power Down
<u>DDRMON_DFI_CLKSTOP_NUM</u>	0x0040	W	0x00000000	Number Of Cke Low For DFI Clkstop
<u>DDRMON_DFI_LP_NUM</u>	0x0044	W	0x00000000	Total Number Of Cke Low
<u>DDRMON_DFI_PHY_LP_NUM</u>	0x0048	W	0x00000000	DDR Phy Low Power
<u>DDRMON_IF_CTRL</u>	0x0200	W	0x00000000	DDR Interface Control Register
<u>DDRMON_MSTID</u>	0x0204	W	0x00000000	Master And AXI ID Of DDR Command
<u>DDRMON_IDMSK</u>	0x0208	W	0x00000000	Master And AXI ID MASK Of DDR Command
<u>DDRMON_WR_START_ADDR</u>	0x020c	W	0x00000000	Write Start Address
<u>DDRMON_WR_END_ADDR</u>	0x0210	W	0x00000000	Write End Address
<u>DDRMON_RD_START_ADDR</u>	0x0214	W	0x00000000	Read Start Address
<u>DDRMON_RD_END_ADDR</u>	0x0218	W	0x00000000	Read End Address
<u>DDRMON_FIFO0_ADDR</u>	0x0240	W	0x00000000	DDR Controller Interface Address FIFO0
<u>DDRMON_FIFO0_ID</u>	0x0244	W	0x00000000	DDR Controller Interface Command ID FIFO0
<u>DDRMON_FIFO1_ADDR</u>	0x0248	W	0x00000000	DDR Controller Interface Address FIFO1
<u>DDRMON_FIFO1_ID</u>	0x024c	W	0x00000000	DDR Controller Interface Command ID FIFO1
<u>DDRMON_FIFO2_ADDR</u>	0x0250	W	0x00000000	DDR Controller Interface Address FIFO2
<u>DDRMON_FIFO2_ID</u>	0x0254	W	0x00000000	DDR Controller Interface Command ID FIFO2
<u>DDRMON_FIFO3_ADDR</u>	0x0258	W	0x00000000	DDR Controller Interface Address FIFO3
<u>DDRMON_FIFO3_ID</u>	0x025c	W	0x00000000	DDR Controller Interface Command ID FIFO3

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 1.4.6 Detail Registers Description

#### DDRMON\_IP\_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x23	ip_version DDR monitor IP version

#### DDRMON\_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:6	RO	0x000	reserved
5	RW	0x0	ddr4_en 1'b1: Enable 1'b0: Disable
4	RW	0x0	lpddr4_en 1'b1: Enable 1'b0: Disable
3	RW	0x1	hardware_en 1'b1: Enable 1'b0: Disable
2	RW	0x0	lpddr23_en Enable lpddr3 1'b1: Enable 1'b0: Disable
1	RW	0x0	software_en 1'b1: Enable 1'b0: Disable
0	RW	0x0	timer_cnt_en 1'b1: Enable 1'b0: Disable

**DDRMON\_INT\_STATUS**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
12	RW	0x0	rd_addr_hit This is the interrupt status read address hit the setting range.
11	RW	0x0	wr_addr_hit This is the interrupt status write address hit the setting range.
10	RW	0x0	over_int_phy_dfilp This is the interrupt status of DDR PHY DFI power down number over than high threshold.
9	RW	0x0	below_int_phy_dfilp This is the interrupt status of DDR PHY DFI power down number less than low threshold.
8	RW	0x0	over_int_clkstop This is the interrupt status of DDR clk stop number over than high threshold. Only valid for lpddr3/lpddr4.
7	RW	0x0	below_int_clkstop This is the interrupt status of DDR clk stop number less than low threshold. Only valid for lpddr3/lpddr4.
6	RO	0x0	over_int_pdex This is the interrupt status of DDR power down number over than high threshold.
5	RO	0x0	below_int_pdex This is the interrupt status of DDR power down number less than low threshold.

Bit	Attr	Reset Value	Description
4	RW	0x0	compare_statistics This is the interrupt status to statistics the number of activate, write or read command and so on.
3	RW	0x0	over_int_srex This is the interrupt status of DDR self refresh number over than high threshold.
2	RW	0x0	below_int_srex This is the interrupt status of DDR self refresh number less than low threshold.
1	RO	0x0	over_int This is the interrupt status of DDR read and write burst number more than high threshold.
0	RO	0x0	below_int This is the interrupt status of DDR read and write burst number less than low threshold.

**DDRMON\_INT\_MASK**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	write_enable When bit 16=1, bit 0 can be written by softwar. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15	RO	0x0	reserved
14	RW	0x1	reserved
13	RW	0x1	reserved
12	RW	0x1	rd_addr_hit_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
11	RW	0x1	wr_addr_hit_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
10	RW	0x1	over_int_phy_lp_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
9	RW	0x1	below_int_phy_lp_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
8	RW	0x1	over_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

Bit	Attr	Reset Value	Description
7	RW	0x1	below_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
6	RO	0x1	over_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
5	RO	0x1	below_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
4	RW	0x1	compare_statistics_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
3	RW	0x1	over_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
2	RW	0x1	below_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
1	RO	0x1	over_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RO	0x1	below_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

**DDRMON\_TIMER\_COUNT**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	timer_count The timer counter threshold, the statistics of DDR access only be done when timer counter is less then this threshold in hardware mode, in OSC clock cycle.

**DDRMON\_FLOOR\_NUMBER**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_number The low threshold in the comparison of DDR access.

**DDRMON\_TOP\_NUMBER**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_number The high threshold in the comparison of DDR access.

**DDRMON\_DFI\_ACT\_NUM**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_act_num DFI active command number in the statistics range.

**DDRMON DFI WR NUM**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_wr_num DFI write command number in the statistics range.

**DDRMON DFI RD NUM**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rd_num DFI read command number in the statistics range.

**DDRMON COUNT NUM**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_count_num The DFI counter number in the statistics range, in DDR clock cycle.

**DDRMON DFI ACCESS NUM**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_access_num DFI read and write command number in the statistics range.

**DDRMON TOP LP NUMBER**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_lp_number The high threshold in the comparison of DDR self-refresh, power down or clkstop.

**DDRMON FLOOR LP NUMBER**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_lp_number The low threshold in the comparison of DDR self-refresh, power down or clkstop.

**DDRMON DFI SREX NUM**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_srex_num DFI self-refresh number during cke low.

**DDRMON DFI PDEX NUM**

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_pdex_num DFI power down number during cke low.



**DDRMON DFI CLKSTOP\_NUM**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_clkstop_num DFI clkstop number during cke low. Only valid for lpddr3/4.

**DDRMON DFI LP\_NUM**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_lp_num The sum of DFI self-refresh, power down and clkstop number during cke low.

**DDRMON DFI PHY\_LP\_NUM**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_phy_lp_num Phy low power count number during the time both dfi_lp_req and dfi_lp_ack assert.

**DDRMON IF\_CTRL**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:3	RO	0x0000	reserved
2	RW	0x0	if_mon_en 1'b1: Enable 1'b0: Disable
1	RO	0x0	reserved
0	RW	0x0	direction 1'b1: Read 1'b0: Write

**DDRMON MSTID**

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	ddr_mstid High 7 bits: Master ID Low 10 bits: AXI command ID

**DDRMON IDMSK**

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	ddr_idmsk When bit set to high, this bit of MSTID will be masked, and does not take part in the ID comparison.

**DDRMON WR START ADDR**

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_start_addr Write start address for address comparison.

**DDRMON WR END ADDR**

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_end_addr Write end address for address comparison.

**DDRMON RD START ADDR**

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_start_addr Read start address for address comparison.

**DDRMON RD END ADDR**

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_end_addr Read end address for address comparison.

**DDRMON FIFO0 ADDR**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo0_addr DDR controller interface address FIFO0.

**DDRMON FIFO0 ID**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo0_id DDR controller interface command ID FIFO0.

**DDRMON FIFO1 ADDR**

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo1_addr DDR controller interface address FIFO1.

**DDRMON FIFO1 ID**

Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo1_id DDR controller interface command ID FIFO1.

**DDRMON FIFO2 ADDR**

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo2_addr DDR controller interface address FIFO2.

**DDRMON\_FIFO2\_ID**

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo2_id DDR controller interface command ID FIFO2.

**DDRMON\_FIFO3\_ADDR**

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo3_addr DDR controller interface address FIFO3.

**DDRMON\_FIFO3\_ID**

Address: Operational Base + offset (0x025c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo3_id DDR controller interface command ID FIFO3.

**1.5 Interface Description**

DDR IOs from DDR PHY are listed as following Table.

Table 1-1DDR IO description

Pin Name	Description
CK	Positive differential clock
CKB	Negative differential clock
CKE	Active-high clock enable signal for two chip select.
CSBi (i=0,1)	Active-low chip select signal. There are two chip select.
ACTN	Activation command input.
BA[1:0] BG[1:0]	Bank address signal. For DDR3, BA0 should connect to the BA0. BA1 should connect to BA1. BG0 should connect to BA2. For DDR4, please connect directly. Unused for LPDDRn.
A[17:0]	Address signal.
DQ[31:0]	Bidirectional data line
DQS[3:0]	Positive differential bidirectional data strobes
DQSB[3:0]	Negative differential bidirectional data strobes.
DM[3:0]	Active-low data mask signal.
ODTi (i=0,1)	On-Die Termination output signal for two chip select.
RESETN	Reset signal.

The DDR PHY supports more than one SDRAM type and the command pad of DDR PHY is named in the format of DDR4. The PHY supports different command map for different SDRAM type and also supports to use the register to control the map between the commands, and then the user can be very conveniently to design the Combo Memory System based on the different command map function. The default command map relationship shows in the following table. When the user uses the mem\_select[2:0](reg01[2:0]) to choose the memory type, the command will change to the default command map. The user should accord to the following table to connect the command pad to the SDRAM pad.

Table 1-2 DDR IO Mapping Table

CMD PAD OF PHY (DDR4)	DDR3	LPDDR3	LPDDR4
A0	A3	A3	CKE1_A
A1	BA1	-	CKE0_B
A2	A9	A9	A4_A
A3	A15	-	A5_B
A4	A6	A6	CK_A
A5	A12	-	ODT0_B
A6	BA2	-	A0_A
A7	A4	A4	ODT0_A
A8	A1	A1	CKE0_A
A9	A5	A5	A5_A
A10	A8	A8	CLKB_A
A11	A7	A7	CA2_A
A12	RASN	-	CA1_A
A13	A13	-	CA3_A
A14	A14	-	CSB1_B
A15	A10	-	CA0_B
A16	A11	-	CSB0_B
A17	-	-	-
ACTN	CKE	CKE	CA3_B
BA0	CSB1	CSB1	CSB0_A
BA1	WEN	-	CKE1_B
BG0	ODT1	ODT1	CSB1_A
BG1	A2	A2	ODT1_A
CKE	CASB	-	CA1_B
CKB	CKB	CKB	CKB_B
CK	CK	CK	CK_B
CSB0	ODT0	ODT0	CA2_B
CSB1	BA0	-	-
ODT0	CSB0	CSB0	CA4_B
ODT1	A0	A0	ODT1_B
RESETN	RESETN	-	RESETN

At the PHY top-level, the mapping relationships between the DQ pads and dfi\_wrdata/dfi\_rddata shows in the following table. When connecting a DDR3/DDR4/LPDDR3 memory to the interface, there is a default mapping between the DDR3/DDR4/LPDDR3 signals to the PHY top-level pins.

Table 1-3 Default DDR DQ IO Mapping Table for DDR3/DDR4/LPDDR3

PHY TOP-LEVEL PINS	SDRAM	dfi_wrdata/dfi_rddata
A_DQ[7:0]	DQ[7:0]	dfi_wrdata[7:0]/dfi_rddata[7:0]
A_DQ[15:8]	DQ[15:8]	dfi_wrdata[15:8]/dfi_rddata[15:8]
B_DQ[7:0]	DQ[15:8]	dfi_wrdata[23:16]/dfi_rddata[23:16]
B_DQ[15:8]	DQ[31:24]	dfi_wrdata[31:24]/dfi_rddata[31:24]

When connecting a LPDDR4 memory to the PHY top-level, there is a fixed mapping between the LPDDR4 DQ signals to the PHY top-level pins.

Table 1-4 Default DDR DQ IO Mapping Table for LPDDR4

PHY TOP-LEVEL PINS	SDRAM	dfi_wrdata/dfi_rddata
A_DQ[7:0]	DQ[15:8]	dfi_wrdata[7:0]/dfi_rddata[7:0]
A_DQ[15:8]	DQ[23:16]	dfi_wrdata[15:8]/dfi_rddata[15:8]
B_DQ[23:16]	DQ[7:0]	dfi_wrdata[23:16]/dfi_rddata[23:16]
B_DQ[31:24]	DQ[31:24]	dfi_wrdata[31:24]/dfi_rddata[31:24]

## 1.6 Application Notes

## 1.6.1 Initialization

### 1. PCTL & DDR PHY Initialization

1. Assert the resets (presn, core\_ddrc\_rstn and aresetn\_0 of PCTL)
2. Configure PLL of DDR PHY and wait PLL lock.
3. De-assert presn if clocks are active and stable.
4. Initial PCTL register and PHY Register
5. Start PHY initialization with DFIMISC[5] register of PCTL
6. De-assert the remaining resets (core\_ddrc\_rstn and aresetn\_0 of PCTL)
7. Wait PCTL initialization done (STAT.operation\_mode==normal)
8. Start PHY dqs calibration with PHYREG2 register and wait calibration finish with PHY REG91 register.
9. (Optional) After dqs calibration, start write levelling training with PHYREG2 register and wait write levelling training finish with PHY REG92 register.
10. Start to write and read

### 2. DDR3/DDR3L Initialization Sequence

The initialization steps for DDR3/DDR3L SDRAMs are as follows:

1. Power-up.
2. Maintain dfi\_reset\_n low for duration specified by INIT1.dram\_rstn\_x1024. Specification requires at least 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre\_cke\_x1024. Specification requires at least 500us.
4. Assert CKE and issue NOP/deselect for INIT0.post\_cke\_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR2 with INIT4.emr2 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
6. Issue MRS command to load MR3 with INIT4.emr3 followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
7. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
8. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration of DRAMTMG3.t\_mod.
9. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev\_zqinit\_x32.
10. Wait for INIT5.dev\_zqinit\_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
11. The PCTL controller is now ready for normal operation.

### 3. DDR4 Initialization Sequence

The initialization steps for DDR4 SDRAMs are as follows:

1. Power-up.
2. Maintain dfi\_reset\_n low for duration specified by INIT1.dram\_rstn\_x1024. Specification requires at least 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre\_cke\_x1024. Specification requires at least 500 us.
4. Assert CKE and issue NOP/deselect for INIT0.post\_cke\_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR3 with INIT4.emr3 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
6. Issue MRS (mode register set) command to load MR6 with INIT7.mr6 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
7. Issue MRS (mode register set) command to load MR5 with INIT6.mr5 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
8. Issue MRS (mode register set) command to load MR4 with INIT7.mr4 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
9. Issue MRS command to load MR2 with INIT4.emr2 followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
10. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.

11. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration of DRAMTMG3.t\_mod.
12. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev\_zqinit\_x32.
13. Wait for INIT5.dev\_zqinit\_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
14. The PCTL controller is now ready for normal operation.

#### 4. LPDDR3 Initialization Sequence

The initialization steps for LPDDR3 SDRAMs are as follows:

1. Power-up.
2. CKE is held low for a duration specified by INIT0.pre\_cke\_x1024. The clock is checked to be stable for duration specified by INIT2.min\_stable\_clock\_x1 (minimum of 5 clock cycles) prior to the first low to high transition of CKE.
3. Assert CKE for INIT0.post\_cke\_x1024 (specification requires at least 200 us).
4. A MRW (Reset) command is issued to MRW63 register. Values of MA<7:0> = 3FH and OP<7:0> = 00H is used for this command. The MRW reset command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence.
5. Issue NOP/deselect for duration specified by INIT2.idle\_after\_reset\_x32 (specification requires 1 us minimum) and INIT5.max\_auto\_init\_x1024 (specification requires maximum time of 10 us).
6. An MRW ZQ initialization calibration command is issued to the memory to register MR10 to initiate the ZQ calibration. Values of MA<7:0> = 0AH and OP<7:0> = FFH is used for this command.
7. Issue NOP/deselect for duration specified by INIT5.dev\_zqinit\_x32 (specification requires a minimum time of 1us).
8. Program MR2 register by setting MR2 register to INIT3.emr followed by a NOP/deselect for a duration specified by DRAMTMG3.t\_mrw (typical value of 5 clock cycles).
9. Program MR1 register by setting MR1 register to INIT3.mr followed by a NOP/deselect for a duration specified by DRAMTMG3.t\_mrw (typical value of 5 clock cycles).
10. Program MR3 register by setting MR3 register to INIT4.emr2 followed by a NOP/deselect for a duration specified by DRAMTMG3.t\_mrw (typical value of 5 clock cycles).
11. Schedule multiple all bank refresh.
12. The PCTL controller is now ready for normal operation.

#### 5. LPDDR4 Initialization Sequence

The initialization steps for LPDDR4 SDRAMs are as follows:

1. Power-up.
2. Maintain dfi\_reset\_n and dfi\_reset\_n\_ref low for duration specified by INIT1.dram\_rstn\_x1024. Specification requires at least 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre\_cke\_x1024. Specification requires at least 2ms.
4. Assert CKE and issue NOP/deselect for INIT0.post\_cke\_x1024. Specification requires at least 2 us.
5. Issue MRS (mode register set) command to load MR13 with INIT4.emr3 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrw.
6. Issue MRS (mode register set) command to load MR1 with INIT3.mr value followed by NOP/deselect for duration of DRAMTMG3.t\_mrw.
7. Issue MRS (mode register set) command to load MR2 with INIT3.emr value followed by NOP/deselect for duration of DRAMTMG3.t\_mrw.
8. Issue MRS (mode register set) command to load MR3 with INIT4.emr2 value followed by NOP/deselect for duration of DRAMTMG3.t\_mrd.
9. Issue ZQCal Start command and wait for ZQCTL0.t\_zq\_long\_nop.
10. Issue ZQCal Latch command and wait for ZQCTL0.t\_zq\_short\_nop.
11. Schedule multiple refresh.
12. The PCTL controller is now ready for normal operation.

### 1.6.2 High Speed IO Drive Strength

The register related to the CMD IO drive strength shows in the following table.

Table 1-5 The related register of the CMD IO drive strength

ADDR	BIT	DEFAULT	DESCRIPTIONS
0x400	[4:0]	0xe	The pull-down resistance of CMD except CK. The resistance relation with the configuration show in CMD driver strength table.
0x404	[4:0]	0xe	The pull-up resistance of CMD except CK. The resistance relation with the configuration show in CMD driver strength table.
0x408	[4:0]	0xe	The pull-down resistance of CK and CKB. The resistance relation with the configuration show in CMD driver strength table.
0x40c	[4:0]	0xe	The pull-up resistance of CK and CKB. The resistance relation with the configuration show in CMD driver strength table.

Table 1-6 DDR4/LPDDR3 CMD drive strength table

Control bit	5'b00000	5'b00001	5'b00010	5'b00011	units
Pull-up/down	+∞	569.8	284.9	189.9	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	142.4	114	94.97	81.4	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	71.23	63.31	56.98	51.8	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	47.48	43.83	40.7	37.99	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	71.23	63.31	56.98	51.8	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	47.48	43.83	40.7	37.99	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	35.61	33.52	31.66	29.99	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	28.49	27.13	25.9	24.77	ohm

Table 1-7 DDR3 CMD drive strength table

Control bit	5'b00000	5'b00001	5'b00010	5'b00011	units
Pull-up/down	+∞	506.1	253.1	168.7	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	126.5	101.2	84.36	72.31	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	63.27	56.24	50.62	46.02	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	42.18	38.94	36.15	33.74	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	63.27	56.24	50.62	46.02	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	42.18	38.94	36.15	33.74	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	31.64	29.77	28.12	26.64	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	25.31	24.1	23.01	22.01	ohm

Table 1-8 LPDDR4 CMD drive strength table

Control bit	5'b00000	5'b00001	5'b00010	5'b00011	units
Pull-up/down	+∞	606.3	303.1	202.1	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	151.6	121.3	101	86.61	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm

Pull-up/down	75.79	67.37	60.63	55.12	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	50.52	46.64	43.31	40.42	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	75.79	67.37	60.63	55.12	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	50.52	46.64	43.31	40.42	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	37.89	35.66	33.68	31.91	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	30.31	28.87	27.56	26.36	ohm

Table 1-9 DDR4/LPDDR3 DQ/DQS drive strength table

<b>Control bit</b>	<b>5'b00000</b>	<b>5'b00001</b>	<b>5'b00010</b>	<b>5'b00011</b>	<b>units</b>
Pull-up/down	+∞	569.8	284.9	189.9	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	142.4	114	94.97	81.4	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	71.23	63.31	56.98	51.8	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	47.48	43.83	40.7	37.99	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	71.23	63.31	56.98	51.8	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	47.48	43.83	40.7	37.99	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	35.61	33.52	31.66	29.99	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	28.49	27.13	25.9	24.77	ohm

Table 1-10 DDR4/LPDDR3 DQ/DQSODT resistance table

<b>Control bit</b>	<b>5'b00000</b>	<b>5'b00001</b>	<b>5'b00010</b>	<b>5'b00011</b>	<b>units</b>
Pull-up/down	+∞	973.1	493.2	327.3	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	246.6	196.8	164.4	140.7	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	123.3	109.4	98.65	89.57	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	82.21	75.8	70.46	65.71	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	123.3	109.4	98.65	89.57	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	82.21	75.8	70.46	65.71	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	61.65	57.98	54.8	51.88	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	49.32	46.94	44.84	42.86	ohm

Table 1-11 DDR3 DQ/DQS drive strength table

<b>Control bit</b>	<b>5'b00000</b>	<b>5'b00001</b>	<b>5'b00010</b>	<b>5'b00011</b>	<b>units</b>
Pull-up/down	+∞	506.1	253.1	168.7	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	126.5	101.2	84.36	72.31	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	63.27	56.24	50.62	46.02	ohm



<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	42.18	38.94	36.15	33.74	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	63.27	56.24	50.62	46.02	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	42.18	38.94	36.15	33.74	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	31.64	29.77	28.12	26.64	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	25.31	24.1	23.01	22.01	ohm

Table 1-12 DDR3 DQ/DQS ODT resistance table

<b>Control bit</b>	<b>5'b00000</b>	<b>5'b00001</b>	<b>5'b00010</b>	<b>5'b00011</b>	<b>units</b>
Pull-up/down	+∞	952.8	482.7	320.4	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	241.4	192.6	160.9	137.7	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	120.7	107.1	96.54	87.66	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	80.45	74.19	68.96	64.31	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	120.7	107.1	96.54	87.66	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	80.45	74.19	68.96	64.31	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	60.34	56.75	53.63	50.78	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	48.27	45.94	43.88	41.95	ohm

Table 1-13 LPDDR4 DQ/DQS drive strength table

<b>Control bit</b>	<b>5'b00000</b>	<b>5'b00001</b>	<b>5'b00010</b>	<b>5'b00011</b>	<b>units</b>
Pull-up/down	+∞	606.3	303.1	202.1	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	151.6	121.3	101	86.61	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	75.79	67.37	60.63	55.12	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm
Pull-up/down	50.52	46.64	43.31	40.42	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	75.79	67.37	60.63	55.12	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	50.52	46.64	43.31	40.42	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	37.89	35.66	33.68	31.91	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	30.31	28.87	27.56	26.36	ohm

Table 1-14 LPDDR4 DQ/DQS ODT resistance table

<b>Control bit</b>	<b>5'b00000</b>	<b>5'b00001</b>	<b>5'b00010</b>	<b>5'b00011</b>	<b>units</b>
Pull-up/down	+∞	997.9	506.1	335.8	ohm
<b>Control bit</b>	<b>5'b00100</b>	<b>5'b00101</b>	<b>5'b00110</b>	<b>5'b00111</b>	ohm
Pull-up/down	253.1	201.9	168.7	144.3	ohm
<b>Control bit</b>	<b>5'b01000</b>	<b>5'b01001</b>	<b>5'b01010</b>	<b>5'b01011</b>	ohm
Pull-up/down	126.5	112.3	101.2	91.91	ohm
<b>Control bit</b>	<b>5'b01100</b>	<b>5'b01101</b>	<b>5'b01110</b>	<b>5'b01111</b>	ohm

Pull-up/down	84.36	77.79	72.31	67.42	ohm
<b>Control bit</b>	<b>5'b10000</b>	<b>5'b10001</b>	<b>5'b10010</b>	<b>5'b10011</b>	ohm
Pull-up/down	126.5	112.3	101.2	91.91	ohm
<b>Control bit</b>	<b>5'b10100</b>	<b>5'b10101</b>	<b>5'b10110</b>	<b>5'b10111</b>	ohm
Pull-up/down	84.36	77.79	72.31	67.42	ohm
<b>Control bit</b>	<b>5'b11000</b>	<b>5'b11001</b>	<b>5'b11010</b>	<b>5'b11011</b>	ohm
Pull-up/down	63.27	59.5	56.24	53.24	ohm
<b>Control bit</b>	<b>5'b11100</b>	<b>5'b11101</b>	<b>5'b11110</b>	<b>5'b11111</b>	ohm
Pull-up/down	50.62	48.17	46.02	43.99	ohm

### 1.6.3 Per bit de-skew tuning

Per-bit de-skew is designed for compensating PCB trace mismatch, DDR PHY support skew individually adjustable for all PHY signals. There are 64 steps for each bit de-skew adjusting, and the adjust resolution under different corners is shown below:

Table 1-15 Per-bit de-skew tuning resolution

	<b>ff</b>	<b>tt</b>	<b>ss</b>
de-skew resolution	16ps	20ps	30ps

Pre-bit de-skew is realized with inverter chain delay, per-bit de-skew control signals select how much inverters are connected to data path, the minimum resolution is determined by the two inverters minimum delay.

$$\text{DELAY} = \text{REG\_CFG} * \text{DE\_SKEW}$$

TX path de-skew and RX path de-skew employ same delay line, and they have same de-skew tuning resolution. RX de-skew tuning resolution can be about 20ps in tt corner, and we can re-design tuning resolution according to system and customer requirement.

### 1.6.4 Command Perbit De-Skew Control

The DDR PHY supports to use the per-bit de-skew to adjust the delay of the command PAD to change the phase of the command which will be sent to the SDRAM.

For DDR4, the user can use the register to change the per-bit de-skew of the command directly.

Because the PHY supports the default command pad mapping, the user needs to change the corresponding register after the command pad mapping.

For example, if the user chooses DDR4 SDRAM mode, it can change the phase A0 directly through the reg\_a0\_invdelayssel register. The following table gives the detail description about the relationship between the control register and SDRAM PAD.

Table 1-16 The CMD Per Bit De-skew Control Map for SDRAM

NAME	DEFAULT	SDRAM PAD			
		DDR4	DDR3	LPDDR3	LPDDR4
reg_a0_invdelayssel	0x7	A0	A3	A3	CKE1_A
reg_a1_invdelayssel	0x7	A1	BA1	-	CKE0_B
reg_a2_invdelayssel	0x7	A2	A9	A9	A4_A
reg_a3_invdelayssel	0x7	A3	A15	-	A5_B
reg_a4_invdelayssel	0x7	A4	A6	A6	CK_A
reg_a5_invdelayssel	0x7	A5	A12	-	ODT0_B
reg_a6_invdelayssel	0x7	A6	BA2	-	A0_A
reg_a7_invdelayssel	0x7	A7	A4	A4	ODT0_A
reg_a8_invdelayssel	0x7	A8	A1	A1	CKE0_A
reg_a9_invdelayssel	0x7	A9	A5	A5	A5_A
reg_a10_invdelayssel	0x7	A10	A8	A8	CLKB_A
reg_a11_invdelayssel	0x7	A11	A7	A7	CA2_A
reg_a12_invdelayssel	0x7	A12	RASN	-	CA1_A
reg_a13_invdelayssel	0x7	A13	A13	-	CA3_A
reg_a14_invdelayssel	0x7	A14	A14	-	CSB1_B
reg_a15_invdelayssel	0x7	A15	A10	-	CA0_B
reg_a16_invdelayssel	0x7	A16	A11	-	CSB0_B

NAME	DEFAULT	SDRAM PAD			
		DDR4	DDR3	LPDDR3	LPDDR4
reg_a17_invdelayssel	0x7	A17	-	-	-
reg_ba0_invdelayssel	0x7	ACTN	CKE	CKE	CA3_B
reg_ba1_invdelayssel	0x7	BA0	CSB1	CSB1	CSB0_A
reg_bg0_invdelayssel	0x7	BA1	WEN	-	CKE1_B
reg_bg1_invdelayssel	0x7	BG0	ODT1	ODT1	CSB1_A
reg_cke0_invdelayssel	0x7	BG1	A2	A2	ODT1_A
reg_ck_invdelayssel	0x7	CKE	CASB	-	CA1_B
reg_ckb_invdelayssel	0x7	CKB	CKB	CKB	CKB_B
reg_csb0_invdelayssel	0x7	CK	CK	CK	CK_B
reg_odt0_invdelayssel	0x7	CSB0	ODT0	ODT0	CA2_B
reg_resetn_invdelayssel	0x7	CSB1	BA0	-	-
reg_actn_invdelayssel	0x7	ODT0	CSB0	CSB0	CA4_B
reg_cke1_invdelayssel	0x7	ODT1	A0	A0	ODT1_B
reg_csb1_invdelayssel	0x7	RESETN	RESETN	-	RESETN
reg_odt1_invdelayssel	0x7	A0	A3	A3	CKE1_A

For LPDDR4, the SDRAM supports the command bus train function, so the command per-bit de-skew can be controlled by the register directly or it can be control by the command bus train module. The command per-bit de-skew control path shows in the following figure.

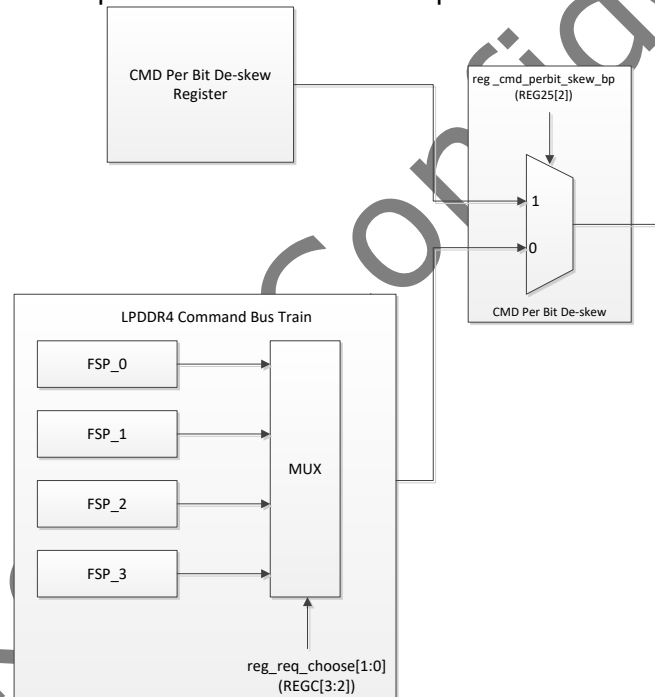


Fig.1-3 CMD Per Bit De-skew Ctrl Path of LPDDR4

After power up, apb reset and phy reset, reg\_cmd\_perbit\_skew\_bp(REG25[2]) is 1'b0. The PHY will choose the command bus train reset value to control the command per-bit de-skew. When set reg\_cmd\_perbit\_skew\_bp(REG25[2]) to 1'b1, then the user can use the register to control the command per-bit de-skew directly.

The FSP\_0/FSP\_1/FSP\_2/FSP\_3 blocks in the command bus train module are used to control the command per-bit de-skew for different frequency groups. When enable the auto command bus train function, the FSP\_n will control the command per-bit de-skew according to the

reg\_freq\_choose[1:0](REGC[3:2]) automatically. After complete the auto command bus

train, the train value will be locked in the FSP\_n module, then the user

can use the reg\_freq\_choose[1:0](REGC[3:2]) to switch frequency quickly. The user also

can use the register to update the FSP\_n lock value after the command bus train. The steps show below:

1. Configure the per-bit de-skew value of the command through the corresponding register. For example, if you want to change the per-bit de-skew of the CA1\_A, configure the desired

value to the reg\_a13\_invdelaysel.

2. Use the register reg\_freq\_choose[1:0](REGC[3:2]) to choose the frequency point.

For example, if you want to change the per-bit de-skew of the command at frequency point 2,

configure the 0x02 to reg\_freq\_choose[1:0](REGC[3:2]).

3. Set the reg\_ca\_perbit\_skew\_update(REG22[6]) to 1'b1 to update the lock value andrecover to 1'b0.

4. After these steps, the per-bit de-sew of command belong to frequency point 2 will change and be locked again.

The above configure path is enabled when reg\_cmd\_perbit\_skew\_bp(REG25[2]) set to 1'b0.

When reg\_cmd\_perbit\_skew\_bp(REG25[2]) set to 1'b1, the user can use the register to control the per-bit de-skew directly. The register directly control path is useful when enable the command bus train bypass mode.

### 1.6.5 Data Perbit De-Skew Control

The address offset of different data channels shows in following table.

Table 1-17 The address offset of each channel

CHANNEL	ADDRESS_OFFSET
A(CS0)	10'h170
A(CS1)	10'h1a0
B(CS0)	10'b1d0
B(CS1)	10'h200

The registers of per-bit de-skew for data show in following table.

Table 1-18 Per bit de-skew for data

ADDR	BIT	DEFAULT	DESCRIPTION
0x000	[5:0]	0x7	reg_dml_invdelayselrx, DM0 de-skew for RX path.
0x004	[5:0]	0x7	reg_dq0_invdelayselrx, DQ0 de-skew for RX path.
0x008	[5:0]	0x7	reg_dq1_invdelayselrx, DQ1 de-skew for RX path.
0x001	[5:0]	0x7	reg_dq2_invdelayselrx, DQ2 de-skew for RX path.
0x010	[5:0]	0x7	reg_dq3_invdelayselrx, DQ3 de-skew for RX path.
0x014	[5:0]	0x7	reg_dq4_invdelayselrx, DQ4 de-skew for RX path.
0x018	[5:0]	0x7	reg_dq5_invdelayselrx, DQ5 de-skew for RX path.
0x01c	[5:0]	0x7	reg_dq6_invdelayselrx, DQ6 de-skew for RX path.
0x020	[5:0]	0x7	reg_dq7_invdelayselrx, DQ7 de-skew for RX path.
0x024	[5:0]	0x7	reg_dqs0_invdelayselrx, DQS0 de-skew for RX path.
0x028	[5:0]	0x7	reg_dqsbl_invdelayselrx, DQSB0 de-skew for RX path.
0x02c	[5:0]	0x7	reg_dmr_invdelayselrx, DM1 de-skew for RX path.
0x030	[5:0]	0x7	reg_dq8_invdelayselrx, DQ8 de-skew for RX path.
0x034	[5:0]	0x7	reg_dq9_invdelayselrx, DQ9 de-skew for RX path.
0x038	[5:0]	0x7	reg_dq10_invdelayselrx, DQ10 de-skew for RX path.
0x03c	[5:0]	0x7	reg_dq11_invdelayselrx, DQ11 de-skew for RX path.
0x040	[5:0]	0x7	reg_dq12_invdelayselrx, DQ12 de-skew for RX path.
0x044	[5:0]	0x7	reg_dq13_invdelayselrx, DQ13 de-skew for RX path.
0x048	[5:0]	0x7	reg_dq14_invdelayselrx, DQ14 de-skew for RX path.
0x04c	[5:0]	0x7	reg_dq15_invdelayselrx, DQ15 de-skew for RX path.
0x050	[5:0]	0x7	reg_dqs1_invdelayselrx, DQS1 de-skew for RX path.
0x054	[5:0]	0x7	reg_dqsbr_invdelayselrx, DQSB1 de-skew for RX path.
0x058	[5:0]	0x7	reg_dml_invdelaysel_t, DM0 de-skew for TX path.
0x05c	[5:0]	0x7	reg_dq0_invdelaysel_t, DQ0 de-skew for TX path.
0x060	[5:0]	0x7	reg_dq1_invdelaysel_t, DQ1 de-skew for TX path.
0x064	[5:0]	0x7	reg_dq2_invdelaysel_t, DQ2 de-skew for TX path.
0x068	[5:0]	0x7	reg_dq3_invdelaysel_t, DQ3 de-skew for TX path.
0x06c	[5:0]	0x7	reg_dq4_invdelaysel_t, DQ4 de-skew for TX path.
0x070	[5:0]	0x7	reg_dq5_invdelaysel_t, DQ5 de-skew for TX path.
0x074	[5:0]	0x7	reg_dq6_invdelaysel_t, DQ6 de-skew for TX path.

ADDR	BIT	DEFAULT	DESCRIPTION
0x078	[5:0]	0x7	reg_dq7_invdelaysel_t, DQ7 de-skew for TX path.
0x07c	[5:0]	0x7	reg_dqsl_invdelaysel_t, DQS0 de-skew for TX path.
0x080	[5:0]	0x7	reg_dqsb1_invdelaysel_t, DQSB0 de-skew for TX path.
0x084	[5:0]	0x7	reg_dmr_invdelaysel_t, DM1 de-skew for TX path.
0x088	[5:0]	0x7	reg_dmr_invdelaysel_t, DM1 de-skew for TX path.
0x08c	[5:0]	0x7	reg_dq9_invdelaysel_t, DQ9 de-skew for TX path.
0x090	[5:0]	0x7	reg_dq10_invdelaysel_t, DQ10 de-skew for TX path.
0x094	[5:0]	0x7	reg_dq11_invdelaysel_t, DQ11 de-skew for TX path.
0x098	[5:0]	0x7	reg_dq12_invdelaysel_t, DQ12 de-skew for TX path.
0x09c	[5:0]	0x7	reg_dq13_invdelaysel_t, DQ13 de-skew for TX path.
0x0a0	[5:0]	0x7	reg_dq14_invdelaysel_t, DQ14 de-skew for TX path.
0x0a4	[5:0]	0x7	reg_dq15_invdelaysel_t, DQ15 de-skew for TX path.
0x0a8	[5:0]	0x7	reg_dqsr_invdelaysel_t, DQS1 de-skew for TX path.
0x0ac	[5:0]	0x7	reg_dqsr_invdelaysel_t, DQSB1 de-skew for TX path.
0x0b0	[5:0]	0x7	reg_l_loop_invdelaysel. Used to select the observed TX/RX perbit skew value of Low 8 bits DATA. Then the user can use the register 0x0b8 to get the current using value of de-skew(need to add the ADDR_OFFSET). 5'h0: The current TX de-skew value of DQ0 5'h1: The current TX de-skew value of DQ1 5'h2: The current TX de-skew value of DQ2 5'h3: The current TX de-skew value of DQ3 5'h4: The current TX de-skew value of DQ4 5'h5: The current TX de-skew value of DQ5 5'h6: The current TX de-skew value of DQ6 5'h7: The current TX de-skew value of DQ7 5'h8: The current TX de-skew value of DM0 5'h9: The current TX de-skew value of DQS0 5'ha: The current TX de-skew value of DQSB0 5'h10: The current TX de-skew value of DQ0 5'h11: The current TX de-skew value of DQ1 5'h12: The current TX de-skew value of DQ2 5'h13: The current TX de-skew value of DQ3 5'h14: The current TX de-skew value of DQ4 5'h15: The current TX de-skew value of DQ5 5'h16: The current TX de-skew value of DQ6 5'h17: The current TX de-skew value of DQ7 5'h18: The current TX de-skew value of DM0 5'h19: The current TX de-skew value of DQS0 5'h1a: The current TX de-skew value of DQSB0
0x0b4	[5:0]	0x7	reg_r_loop_invdelaysel. Used to select the observed TX/RX per-bit skew value of High 8 bits DATA. Then the user can use the register 0x0bc to get the current using value of de-skew(need to add the ADDR_OFFSET). 5'h0: The current TX de-skew value of DQ8 5'h1: The current TX de-skew value of DQ9 5'h2: The current TX de-skew value of DQ10 5'h3: The current TX de-skew value of DQ11 5'h4: The current TX de-skew value of DQ12 5'h5: The current TX de-skew value of DQ13 5'h6: The current TX de-skew value of DQ14 5'h7: The current TX de-skew value of DQ15 5'h8: The current TX de-skew value of DM1 5'h9: The current TX de-skew value of DQS1 5'ha: The current TX de-skew value of DQSB1

ADDR	BIT	DEFAULT	DESCRIPTION
			5'h10: The current RX de-skew value of DQ8 5'h11: The current RX de-skew value of DQ9 5'h12: The current RX de-skew value of DQ10 5'h13: The current RX de-skew value of DQ11 5'h14: The current RX de-skew value of DQ12 5'h15: The current RX de-skew value of DQ13 5'h16: The current RX de-skew value of DQ14 5'h17: The current RX de-skew value of DQ15 5'h18: The current RX de-skew value of DM1 5'h19: The current RX de-skew value of DQS1 5'h1a: The current RX de-skew value of DQSB1
0x0b8	[5:0]	0x7	The only read register. Used to observe the current per-bit skew of the TX/RX of Data Channel for low 8 bits.
0x0bc	[5:0]	0x7	The only read register. Used to observe the current per-bit skew of the TX/RX of Data Channel for high 8 bits.

There are three paths to control the TX data Perbit de-skew show in the following table.

Table 1-19 TX data Perbit de-skew path

PATH	DESCRIPTION	CONFIGURE
Register	Using the register to update the TX data Perbit de-skew directly.	reg_dq_wr_train_en(REG7A[1]) set to 0. reg_wl_bypass(REG2[3]) set to 1. Generate the posedge of reg_wl_freq_update(REGC[6])
Write Levelling	Using the write levelling result.	reg_wl_bypass(REG2[3]) set to 0.
Write Training	Using the write training result.	reg_dq_wr_train_en(REG7A[1]) set to 1. reg_wl_bypass(REG2[3]) set to 1.

There are two paths to control the RX data Perbit de-skew show in the following table.

Table 1-20 RX data Perbit de-skew path

PATH	DESCRIPTION	CONFIGURE
Register	Using the register to update the RX data Perbit de-skew directly.	reg_dq_rd_train_en(REG70[1]) set to 0 and reg_rd_train_predef_en(REG70[6]) set to 0. Generate the posedge of reg_rd_train_freq_update(REG70[4])
Read Training	Using the read training result.	reg_dq_rd_train_en(REG70[1]) set to 1 or reg_rd_train_predef_en(REG70[6]) set to 1.

### 1.6.6 DDR PHY Command Bus Training

The LPDDR4-SDRAM command bus must be trained before enabling termination for high-frequency operation. The DDR PHY supports the auto command bus train function to center the internal VREF(ca) in the CA data eye and adjustment of the CS and CA signals to meet setup/hold requirements.

When enable the auto command bus train function, the PHY will complete the train of the VREF(ca), CS and CA automatically. The auto command bus train flow shows in the following steps.

1. Configure timing parameters for auto command bus train such as REG11~REG16.
2. Configure reg\_mr1(REG17)/reg\_mr2(REG18)/reg\_mr3(REG19)/reg\_mr11(REG1A)/reg\_mr13(REG1B)/reg\_mr14(REG1C)/reg\_mr22(REG1D) to configure the load mode value of FSP[Y](the default is FSP[X]).
3. Configure reg\_cat\_rank\_num(REG21[7:6]) to 2'b11 to choose the ca train rank0 and rank1. Configure reg\_lpddr4\_ca\_odt(REG20[5:4]) to terminate rank0 or rank1.
4. Configure reg\_cat\_cs\_train\_value(REG21[5:0]) and reg\_cat\_ca\_train\_value(REG22[5:0]) to choose the cs and ca training pattern.
5. Configure reg\_cha\_cat\_cs\_check\_value(REG76[5:0])/reg\_chb\_cat\_cs\_check\_value(REG77[5:0])/reg\_cha\_cat\_ca\_check\_value(REG78[5:0])/reg\_chb\_cat\_ca\_check\_value(REG79[5:0]) to choose the cs and ca training pattern.

6. Configure `reg_cat_vref_scan_max(REG23[6:0])` and `reg_cat_ca_scan_max(REG24[7:0])` to choose the vref scan max and command per-bit de-skew scan max. Configure `reg_cat_vref_bp_en(REG20[7])` to 1 to skip the vref train. Configure `reg_cat_vref_scan_steps(REG20[3:1])` to choose the vref scan steps. Configure `reg_cat_skip_cs_train(REG25[6])` to skip the cs train. All of these 4 configurations can be skipped individually. Step 6 is optional which can be skipped to step 7 directly.

7. Configure `reg_freq_choose(REGC[3:2])` to set the current frequency point(FSP[X]-Low speed).

8. Configure `reg_cat_enable(REG10[0])` to 1 to enable the auto command bus train.

9. Configure `reg_freq_choose(REGC[3:2])` to set the command bus train frequency point(FSP[Y]-Train speed).

10. Configure `reg_cat_start(REG10[1])` to 1 to start the auto command bus train.

11. Wait `GRF_DDR_STATUS8[19]` change to high. It means the DDR PHY is ready to do the frequency change.

12. The PCTL should complete the frequency change. Set `GRF_DDR_CON2[10]` to 1 to acknowledge the frequency change request from the DDR PHY.

13. Wait `GRF_DDR_STATUS8[19]` change to low. It means the DDR PHY complete frequency change. Set `GRF_DDR_CON2[10]` to 0 to begin the high frequency CA training.

14. Wait auto command bus train done by reading `REG93[1:0]`, when it equals to 2'b11(for two ranks), it means complete the auto command bus train.

15. Configure `reg_cat_start(REG10[0])` to 0 to exit the auto command bus train.

16. Configure `reg_freq_choose(REGC[3:2])` to set the current frequency point(FSP[X]-Low speed).

17. Configure `reg_cat_enable(REG10[0])` to 0 to disable the auto command bus train.

18. Read register `REG3A0~REG3DF` to get the ca train result.

The command bus train not only adjusts the phase of the CA bus but also adjusts the phase of the CS. The user can use the `reg_cat_skep_cs_train(REG25[6])` to control the enable or disable of the cs train. When this signal sets to 1, the PHY will skip the cs train; when this signal sets to 0, the PHY will enable the cs train.

The PHY support two modes cs train controlled by the `reg_cs_pwc_disable(REG20[0])`: Normal cs train ( `reg_cs_pwc_disable = 1`): When choose the normal cs train mode, the pulse

width of the CS will keep the same width of the CK period.

Modulation cs train ( `reg_cs_pwc_disable = 0`): It is the default mode. When choose this mode,

the pulse width of the CS will the 75% of the CK period when the CS is in the train mode (after

the frequency changes from the FSP[X] to FSP[Y]). The state shows in the following figure.

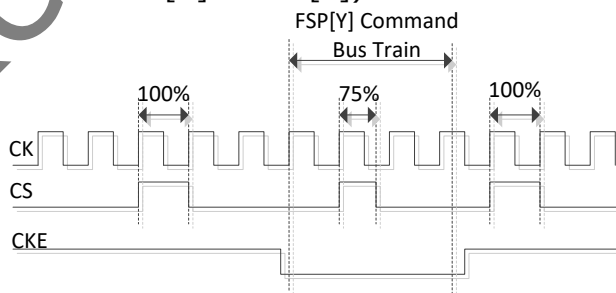


Fig.1-4 Modulation cs train mode

If the user enables the Modulation cs train mode, the CS Train is based on the 75% pulse width of the normal CS. So the cs train result has fixed 25% offset and need to compensate 12.5% offset using the special register after the command bus train. After that, the CS will go to the best point of the cs train.

The user uses the following registers to complete the compensation of the cs train result.

Table 1-21 Compensation of the cs train result

ADDR	SIGNAL	DESCRIPTION
0x154[7:4]	<code>reg_cs_perbit_sekw_offset_fsp0</code>	Used to compensate the train result of CS at the frequency point 0.

ADDR	SIGNAL	DESCRIPTION
		Value = (fsp0_ck_period * 0.125/20ps)
0x154[3:0]	reg_cs_perbit_sekw_offset_fsp1	Used to compensate the train result of CS at the frequency point 1. Value = (fsp1_ck_period * 0.125/20ps)
0x158[7:4]	reg_cs_perbit_sekw_offset_fsp2	Used to compensate the train result of CS at the frequency point 2. Value = (fsp2_ck_period * 0.125/20ps)
0x158[3:0]	reg_cs_perbit_sekw_offset_fsp3	Used to compensate the train result of CS at the frequency point 3. Value = (fsp3_ck_period * 0.125/20ps)

This register should be set after the command bus train and before change the frequency to the train frequency point.

### 1.6.7 DDR PHY RX DQS Calibration

DDR PHY auto dqs calibration function has been implemented in the PHY. The entire training processes only need to configure the register to start and wait for finish.

The entire training process is as follows:

1. PHY's register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHY's register beginning calibration.

ADDR	BIT	DEFAULT	DESCRIPTION
0x8	5~4	0x0	DQS gating calibration CS select signal 2'b00: select CS0 and CS1    2'b01: select CS1 2'b10: select CS0
	1	0x0	set calibration bypass mode(1:bypass mode; 0:normal)
	0	0x0	set calibration start (1:start; 0: stop)

4. Wait for the calibration finish by PHYREG91.
5. Normal read and writes operation can begin.

### 1.6.8 DDR PHY Write Levelling Training

DDR PHY auto write levelling training function has been implemented in the PHY. The entire training processes only need to configure the register to start and wait for finish.

The entire training process is as follows:

1. PHY's register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHYREG3 and REG4 to configure the dram mode register which used to enable dram write levelling training function.
4. Set the PHY's register to begin training.

ADDR	BIT	DEFAULT	DESCRIPTION
0x8	7~6	0x0	Write levelling CS select signal 2'b00: select CS0 and CS1    2'b01: select CS1 2'b10: select CS0
	3	0x0	Write levelling calibration bypass mode, active high.
	2	0x0	The enable signal of the write-levelling function. High valid.

5. Wait for the calibration finish by polling PHY REG92. The write levelling results can be read from the following registers.

Table 1-22 The write levelling result for channel A

ADDR	BIT	DEFAULT	DESCRIPTION
0x318	[4:0]	0x0	The cs0 write levelling result of the channel low 8 bits.
0x31c	[4:0]	0x0	The cs0 write levelling result of the channel high 8 bits.
0x320	[4:0]	0x0	The cs1 write levelling result of the channel low 8 bits.
0x324	[4:0]	0x0	The cs1 write levelling result of the channel high 8 bits.

Table 1-23 The write levelling result for channel B



ADDR	BIT	DEFAULT	DESCRIPTION
0x3d8	[4:0]	0x0	The cs0 write levelling result of the channel low 8 bits.
0x3dc	[4:0]	0x0	The cs0 write levelling result of the channel high 8 bits.
0x3e0	[4:0]	0x0	The cs1 write levelling result of the channel low 8 bits.
0x3e4	[4:0]	0x0	The cs1 write levelling result of the channelhigh 8 bits.

6. Normal read and writes operation can begin.

### 1.6.9 DDR PHY Read Train

The DDR PHY supports the read training. It includes three modes:

- Auto MPR/MPC Mode( Only support for DDR3/DDR4/LPDDR3/LPDDR4)
- Predefined mode (Only support DDR3/DDR4/LPDDR3/LPDDR4)
- Bypass Mode( Only support LPDDR3 and LPDDR4)

Auto MPR/MPC Mode: When the PHY chooses the DDR3/DDR4, it will use the MPR command to complete the read training of the Auto-Mode. When the PHY chooses the LPDDR3/LPDDR4, it will use the RD DQ Calibration command to complete the read training of the Auto-Mode and BP-Mode.

Predefine mode: you should write data to SDRAM and make sure the data has been written to the SDRAM at the specified location. For example, you can write data when SDRAM working at low frequency. Then the PHY read the data which you write to SDRAM.

When we enable the read training, the PHY will adjust the per-bit de-skew to change the delay of the RX DQS and RX DQ to find the optimal position. The adjust range of the per-bit de-skew is from 6'h0 to 6'h3f.

In rx vref training, we change the value of phy's vref. When set a new vref value to PHY, we should wait 800ns to update it. And the adjust range of the vref is from 8'h00 to 8'hff. You can

change the PHY's vref value yourself by configuring the associated register.

For predefined mode, the phy can support rx vref training. If you enable the vref training function, the predefined read training have 3 steps, step1 adjust per-bit de-skew (step1\_delay), step2 adjust vref(step2\_vref), step3 adjust per-bit de-skew(step3\_delay) again. When you disable vref training function, the predefined read training only have step1. When step1 done, all steps done.

During the training, if you set reg\_phy\_refresh\_en to 1'b1, the PHY support to do auto refresh

by itself. If you use this function, the controller should send a refresh (both rank in the meantime) after training enable, otherwise the PHY will keep waiting.

When the user enables the normal read training function, it will complete the read training automatically. The normal read training using the following steps.

1. Open PHY auto refresh function in training(if you need) by configuring reg\_phy\_refresh\_en=0x1.
2. Choose the read training rank using the reg\_rdtrain\_cs\_sel=2'b10(rank0).
3. Configure the MR15/MR20/MR32/MR40 through reg\_lpddr4\_mr15\_value/reg\_lpddr4\_mr20\_value/reg\_lpddr4\_mr32\_value/reg\_lpddr4\_mr40\_value to choose the read training pattern(Only for lpddr4).
4. choose the dqs phase before read training by setting cha\_reg\_l\_rd\_train\_dqs\_default/cha\_reg\_r\_rd\_train\_dqs\_default/chb\_reg\_l\_rd\_train\_dqs\_default/chb\_reg\_r\_rd\_train\_dqs\_default=0xe.
5. Enable the read training by setting reg\_dq\_rd\_train\_en=0x1.
6. Send a auto refresh(rank0 and rank1 in the meantime) if you open PHY auto refresh function.
7. Wait the train done by polling the reg\_train\_true\_done=0x1.
8. Check the read train state by read cha(b)\_train\_done\_for\_rd\_to\_reg[1:0]. High means error.
9. Exit the Read train by setting reg\_dq\_rd\_train\_en=0x0.

### 1.6.10 DDR PHY Write Train

The DDR PHY supports the write training. It only supports the auto mode. When the PHY

chooses the DDR3/DDR4/LPDDR3, it will use the normal write and readcommand to complete the write training. When the PHY chooses the LPDDR4, it will use theDQS-DQ training mode command to complete the write training.

When we enable the write training, the PHY will adjust the per-bit de-skew to change the delay ofthe TX DQ to find the optimal position(The dqs will keep to the phase find by the write-levellingwhen enable the write levelling function). The adjust range of the per-bit de-skew is from 6'h0 to6'h3f.

The PHY can support tx vref training(only for LPDDR4). If you enable the vref training function, the wr training have 3 steps, step1 adjust per-bit de-skew(step1\_delay), step2 adjust vref(step2\_vref), step3 adjust per-bit de-skew(step3\_delay) again. When you close vref trainingfunction, the wr training only have step1, when step1 done, all step done.

When the user enables the normal write training function, it will complete the write trainingautomatically. The normal write training using steps shows below.

1. Configure the initial address(write data to this address)  
reg\_train\_col\_address/reg\_train\_ba\_address/reg\_train\_row\_address.
2. If you set reg\_wrtrain\_check\_data\_value\_random\_gen=0x0, configure the check data value as the data you want to write to SDRAM(10\*BL8).
3. If you need the PHY do refresh in training, you should configure the reg\_phy\_trefi, reg\_phy\_trfc, reg\_max\_refi\_cnt. Then enable the reg\_phy\_refresh\_en=0x1.
4. Choose the write training rank using the reg\_wrtrain\_cs\_sel=0x2(rank0).
5. If you need the PHY do tx vref training, you should configure reg\_train\_vref\_step\_max, reg\_train\_vref\_step\_min, reg\_wrtrain\_lpddr4\_vref\_range, reg\_wrtrain\_vref\_wait\_vref\_cnt\_50ns.
6. If you enable the DBI function, and want to do wr training with DBI function open, you should set reg\_ddr4\_dbi=0x1 first(Only for DDR4).
7. Choose the dqs phase before write training by setting reg\_wr\_train\_dqs\_default\_bypass=0x1. Otherwise PHY will choose the write levelling training result.
8. Choose the write training auto mode by setting reg\_dq\_wr\_train\_auto=0x1.
9. Enable the tx vref training by setting(if need) reg\_train\_vref\_en=0x1. Enable the write training by setting reg\_dq\_wr\_train\_en=0x1.
10. Send a auto refresh if you open PHY auto refresh function.
11. Wait the wr train done by polling the train\_all\_step\_done=0x1.
12. Check the wr train state by read train\_step1\_error, train\_step2\_error, train\_step3\_error. High means error.
13. Exit the write training by setting reg\_dq\_wr\_train\_en=0x0.

### 1.6.11 DDR Standby Mode

The standby mode is enabled by register DDR\_STDBY\_CONTROL0 [0].When DDR controller is idle, and after a period of waiting time, the standby mode will be activated, the clocks of DDR controller, PHY and memory scheduler can be gated.The waiting time is determined by the register DDR\_STDBY\_CONTROL0 [31:16]. It is the counter threshold by controller clock. The register DDR\_STDBY\_CONTROL0[7:4] is used to determine if the clock of memory schedule, PHYCTL or DDR controller will be gated when in standby status.

### 1.6.12 DDR Monitor

#### 1. DDR read or write address monitor

DDR monitor module can store 4 consecutive read or write addresses in real time. We can read these addresses by APB bus for debug when system enters abnormal state.

The steps of configuration to monitor DDR read or write address:

- Configure DDRMON\_DDR\_IF\_CTRL.direction to select storing read or write address.
- Set DDRMON\_DDR\_IF\_CTRL.if\_mon\_en to '1' to enable DDR monitor.
- When system is abnormal, we can read the register to get the current four addresses.

#### 2. DDR access address monitor within a specified range

Sometimes we want to confirm whether DDR read or write within a specified address range, then we can configure the address range and enable this function.

The steps of configuration to monitor DDR access address within a specified range:

Configure the write address range registers DDRMON\_WR\_START\_ADDR, DDRMON\_WR\_END\_ADDR, and read address registers DDRMON\_RD\_START\_ADDR, DDRMON\_RD\_END\_ADDR.

- Enable interrupt by configure the register DDRMON\_INT\_MASK[12:11] to 0.
- Set DDRMON\_DDR\_IF\_CTRL.if\_mon\_en to '1' to enable DDR address monitor.
- If the read or write addresses hit the range, then interrupt will assert, and we can read the interrupt status register DDRMON\_INT\_STATUS.

### 3. DDR access command statistics

This module can do the statistics about DDR access command, like write, read and active by monitoring DFI interface. There are two mode to do statistics, hardware mode and software mode. Two thresholds can be set, if read and write command number is more than high threshold, or less than low threshold, the interrupt will be asserted.

### 4. DDR low power statistics

It does the statistics the low power period such as DDR self-refresh, power down, clkstop and PHY low power. After compare statistics interrupt asserts, the low power period represent in correspond count register will be updated and can be accessed through APB bus interface.

#### Hardware mode

In hardware mode, a dfi timer is used to specify a statistics period, the command statistics is done in the statistics period. The dfi timer is running in 24MHz. After dfi timer counts to the threshold, and update the statistics value, the dfi timer will restart automatically, and count again.

The steps of hardware mode of DDR access command statistics:

- Configure register DDRMON\_CTRL.hardware\_en as '1' to enable hardware mode.
- Configure register DDRMON\_TIMER\_COUNT to set the dfi timer count threshold, the statistics is done in the period of timer being less than the value of DDRMON\_TIMER\_COUNT.
- Configure register DDRMON\_CTRL.lpddr23\_en and DDRMON\_CTRL.lpddr4\_en to set the DDR mode:

DDRMON_CTRL.lpddr23_en	DDRMON_CTRL.lpddr4_en	DDR mode
1	0	LPDDR3
0	0	DDR3
0	1	LPDDR4

- Configure register DDRMON\_FLOOR\_NUMBER to specify the low threshold of interrupt, and configure register DDRMON\_TOP\_NUMBER to specify the high threshold of interrupt.
- Configure register DDRMON\_CTRL.timer\_cnt\_en as '1' to start hardware mode.
- Wait for the interrupt to do following process. We also can read the read, write and active command number separately.

#### Software mode

In software mode, the statistics is controlled by software.

The steps of hardware mode of DDR access command statistics:

- Configure register DDRMON\_CTRL.lpddr23\_en and DDRMON\_CTRL.lpddr4\_en to set the DDR mode like hardware mode.
- Configure register DDRMON\_CTRL.software\_en as '1' to enable software mode statistics.
- Configure register DDRMON\_CTRL.software\_en as '0' to stop the statistics, and generate the statistics result. We can read the read, write and active command number separately.

## Chapter 2 DDR Converter of Frequency (DCF)

### 2.1 Overview

DDR Converter of Frequency (DCF) is used to implement DDR frequency conversion without the participation of CPU. DCF is connected to SOC through an AXI Master and an APB Slave, with a DMAC and instruction buffer inside. Beforehand, software puts into SRAM formulary pieces of instructions which consist of all the register-related configurations in the process of frequency conversion. When started-up, DCF automatically reads instructions to the inside buffer by means of DMA, and implement register configuration after analysis. A done signal will be provided for CPU after all the instructions are analyzed.

DCF supports the following features:

- AMBA 32-bit AXI compliant
- Support DMA operation from SRAM to buffer
  - Support burst8 only
  - LLP not supported
- Support 2 internal instruction registers : r0 & r1
- Support following software instructions:
  - IDL (delay)
  - LDR (read register)
  - STR (write register)
  - ISB (write with flush)
  - Bitwise AND
  - Bitwise OR
  - Bitwise INV
  - LSR (left shift)
  - RSR (right shift)
  - ADD
  - SUB
  - POLLEQ (poll a register until the value match)
  - POLLNEQ (poll a register until the value mismatch)
  - CMPEQ (compare if equal)
  - CMPNEQ (compare if unequal)
  - BL (jump upwards or downwards, 8bytes align)
- Support following program functions through combination of basic instructions
  - If-else
  - while
  - loop
  - for

### 2.2 Block Diagram

DCF comprises with:

- An AXI Master Interface
- An APB Slave Interface
- A DMA controller
- An Instruction Buffer
- Instruction analyzer

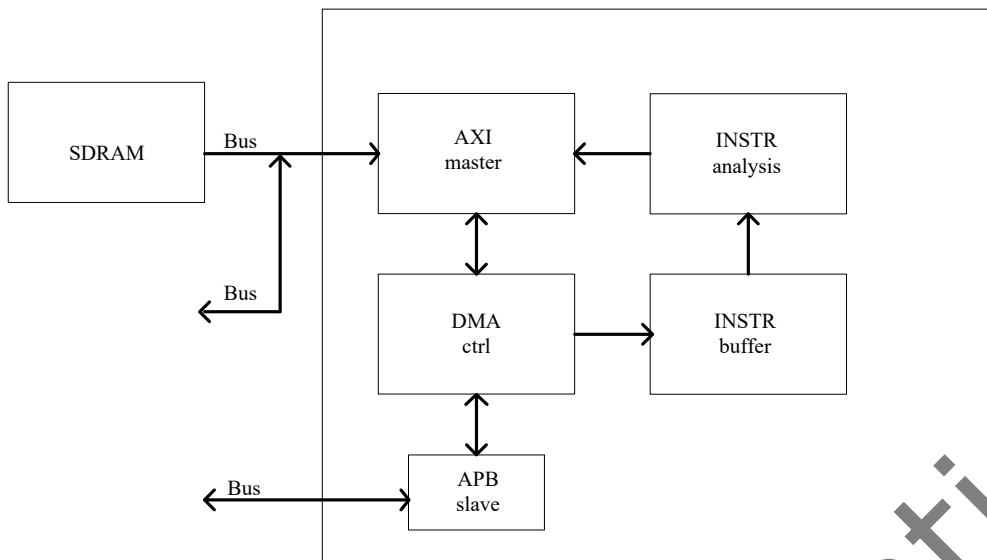


Fig. 2-1 DCF Block Diagram

## 2.3 Register Description

### 2.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 2.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
<u>DCF_CTRL</u>	0x0000	W	0x00000000	DCF Control Register
<u>DCF_STATUS</u>	0x0004	W	0x00000001	DCF Internal Status Register
<u>DCF_ADDR</u>	0x0008	W	0x00000000	DCF Instruction Start Address Register
<u>DCF_ISR</u>	0x000c	W	0x00000000	DCF Interrupt Status Register
<u>DCF_TIMEOUT_CYC</u>	0x0014	W	0xffffffff	DCF Instruction Timeout Cycle Register
<u>DCF_CURR_R0</u>	0x0020	W	0x00000000	Current Internal R0 Value Register
<u>DCF_CURR_R1</u>	0x0024	W	0x00000000	Current Internal R1 Value Register
<u>DCF_CMD_COUNTER</u>	0x0028	W	0x00000000	Current Command Counter Value Register
<u>DCF_LAST_ADDR1</u>	0x0030	W	0x00000000	Last 1 Instruction Address Register
<u>DCF_LAST_ADDR2</u>	0x0034	W	0x00000000	Last 2 Instruction Address Register
<u>DCF_LAST_ADDR3</u>	0x0038	W	0x00000000	Last 3 Instruction Address Register
<u>DCF_LAST_ADDR4</u>	0x003c	W	0x00000000	Last 4 Instruction Address Register

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 2.3.3 Detail Registers Description

#### DCF\_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	vop_hw_en 1'b1 : Enable 1'b0 : Disable

Bit	Attr	Reset Value	Description
1	WO	0x0	timeout_en 1'b1: Enable 1'b0: Disable
0	WO	0x0	start This bit will be auto cleared when DCF is done. 1'b1: Start DCF 1'b0: Stop DCF

**DCF STATUS**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	WO	0x0	dma_done_st 1'b1: DCF has fetched all the instructions.
6	WO	0x0	instr_done_st 1'b1: DCF has done all the instructions analysis.
5	WO	0x0	dma_error_st 1'b1 : Error response received when DCF is fetching instructions.
4	WO	0x0	instr_error_st 1'b1 : Error response received when DCF is handling instructions.
3	WO	0x0	dcf_timeout_st 1'b1: DCF timeout
2	WO	0x0	dcf_edge_trigger_st 1'b1 : DCF is triggered by dma_finish from vop.
1	WO	0x0	dcf_level_trigger_st 1'b1 : DCF is triggered by one of the following sources: vop_standby / vop_clockgating / vop_powdown
0	RO	0x1	dcf_idle_st 1'b1 : DCF is idle 1'b0 : DCF is busy

**DCF ADDR**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr DCF instruction fetch start address

**DCF\_ISR**

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	dcf_error 1'b1: Error response or timeout during DDR change frequency.
0	WO	0x0	dcf_done 1'b1: DDR change frequency completed. 1'b0: DDR change frequency not completed.

**DCF\_TIMEOUT\_CYC**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	timeout Calculated by axi clock

**DCF\_CURR\_R0**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r0 R0 value is sampled when dcf_done or dcf_error occurs.

**DCF CURR R1**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r1 R1 value is sampled when dcf_done or dcf_error occurs.

**DCF CMD COUNTER**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cmd_counter cmd_counter value is sampled when dcf_done or dcf_error occurs. it records the number of pieces of instructions among DCF.

**DCF LAST ADDR1**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr1 Value is sampled when dcf_done or dcf_error occurs. it records the last 1 instruction address.

**DCF LAST ADDR2**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	last_addr2 Value is sampled when dcf_done or dcf_error occurs. it records the last 2 instruction address.

**DCF LAST ADDR3**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr3 Value is sampled when dcf_done or dcf_error occurs. it records the last 3 instruction address.

**DCF LAST ADDR4**

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr4 Value is sampled when dcf_done or dcf_error occurs. it records the last 4 instruction address.

**2.4 Application Notes****2.4.1 DCF Work Flow**

- 1、 Software needs to open up a separate space in SRAM and loads a series of instructions in advance. The instruction should consists of:
  - a、 Configure msch and cpu idle.
  - b、 Configure Memory Controller to move DDR into Low-power State.
  - c、 Reset DDRPHY if needed.
  - d、 Configure Clock frequency, wait for PLL lock.
  - e、 Configure all the Timing-relative registers.

- f、 De-assert DDRPHY reset if needed.
- g、 Initialize DDRPHY, do calibration.
- h、 Configure Memory Controller to move DDR into Access State.
- 2、 Software configure DCF, notifying the start\_addr, and then start DCF.
- 3、 DCF will transfer instruction data through DMA from SRAM to an internal buffer.
- 4、 In the meanwhile, An instruction analysis module will read these instructions from buffer, and transform them to corresponding bus-relative operations, including Write&Read registers, delay some clock cycles, arithmetic operation and so on.
- 5、 By Axi master, DCF will configure uPCTL、 DDRPHY、 CRU module to implement the procedure of DDR frequency conversion.
- 6、 DCF will recognize the last command, and generate a dcf\_done interrupt for CPU.

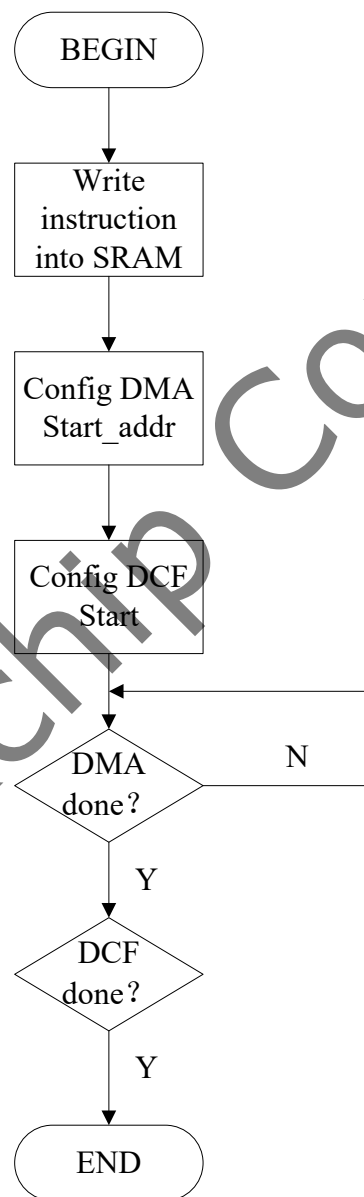


Fig. 2-2 DCF work flow

### 2.4.2 Instruction Format

One piece of instruction, which is 64bit, should consist of the information of:

- 1、 Address



- 2、 Data
- 3、 Command

63:59	58:34	33:32	31:0
cmd[4:0]	addr[26:2]	(r1,r0)	data

The overall principle of instruction information is:

- 1、 Address[31:27] is reserved for 5bit command, which represents the corresponding operation.
- 2、 Address[1:0] is used to indicate operation of r0 or r1.
- 3、 Address[26:2] is the real bus address. If 0, it means no bus operation ; if not 0, it means a combination of 2 instructions with a bus operation ahead and an arithmetic c operation followed in order to improve efficiency.

For example, let us analyze the instruction: 0f620002\_00000003

- 1、 Command is 1, which represents an bitwise AND operation.
- 2、 Address is 0xff620000, represents a bus-read operation.
- 3、 R1 is indicated, represents that the middle result is stored into internal register r1.
- 4、 Data is 0x00000003, represents that the operation value is 0x3.

So, this instruction will do following operations:

- LDR #0xff620000, r1 ; //read register 0xff620000, and store value into r1
- AND r1, 0x00000003 ; //r1 is bitwise AND with 0x3, and re-store the result

The following table lists all the supported command

INSTR	cmd[4:0]	addr[26:2]	R1	R0	Data[31:0]	
IDLE	5'h00	NA	NA	NA	#data	IDL #data
AND	5'h01	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; AND r0 #data
			1	0	#data	ldr #addr r1 ; AND r1 #data
			1	1	NA	ldr #addr r1 ; AND r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	AND r0 #data
			1	0	#data	AND r1 #data
			1	1	NA	AND r1 r0
OR	5'h02	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; OR r0 #data
			1	0	#data	ldr #addr r1 ; OR r1 #data
			1	1	NA	ldr #addr r1 ; OR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	OR r0 #data
			1	0	#data	OR r1 #data
			1	1	NA	OR r1 r0
INV	5'h03	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; XOR r0 ^#data
			1	0	#data	ldr #addr r1 ; XOR r1 ^#data
			1	1	#data	ldr #addr r1 ; XOR r1 ^r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	NA	INV r0
			1	0	NA	INV R1
			1	1	NA	SWP r0 r1
LSR	5'h04	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; LSR r0 #data
			1	0	#data	ldr #addr r1 ; LSR r1 #data
			1	1	NA	ldr #addr r1 ; LSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1

INSTR	cmd[4:0]	addr[26:2]	R1	R0	Data[31:0]	
			0	1	#data	LSR r0 #data
			1	0	#data	LSR r1 #data
			1	1	NA	LSR r1 r0
RSR	5'h05	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; RSR r0 #data
			1	0	#data	ldr #addr r1 ; RSR r1 #data
			1	1	NA	ldr #addr r1 ; RSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	RSR r0 #data
			1	0	#data	RSR r1 #data
			1	1	NA	RSR r1 r0
CMPEQ	5'h06	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPEQ r0 #data,flag
			1	0	#data	ldr #addr r0 ; CMPEQ r1 #data,flag
			1	1	NA	ldr #addr r0 ; CMPEQ r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPEQ r0 #data, flag
			1	0	#data	CMPEQ r1 #data, flag
			1	1	NA	CMPEQ r1 r0, flag
CMPNE	5'h07	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPNE r0 #data,flag
			1	0	#data	ldr #addr r1 ; CMPNE r1 #data,flag
			1	1	NA	ldr #addr r1 ; CMPNE r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPNE r0 #data, flag
			1	0	#data	CMPNE r1 #data, flag
			1	1	NA	CMPNE r1 r0, flag
ADD	5'h08	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; ADD r0 #data
			1	0	#data	ldr #addr r0 ; ADD r1 #data
			1	1	NA	ldr #addr r0 ; ADD r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	ADD r0 #data
			1	0	#data	ADD r1 #data
			1	1	NA	ADD r1 r0
SUB	5'h09	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; SUB r0 #data
			1	0	#data	ldr #addr r0 ; SUB r1 #data
			1	1	NA	ldr #addr r0 ; SUB r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	SUB r0 #data
			1	0	#data	SUB r1 #data
			1	1	NA	SUB r1 r0
STR	5'h0a	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1

INSTR	cmd[4:0]	addr[26:2]	R1	R0	Data[31:0]	
			1	1	#data	STR #addr #data
ISB	5'h0b	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data
POLEQ	5'h0c	NA	0	1	#data	poll r0=#data,repeat last command
			1	0	#data	poll r1=#data,repeat last command
			1	1	NA	poll r1=r0,repeat last command
POLNEQ	5'h0d	NA	0	1	#data	poll r0!=#data,repeat last command
			1	0	#data	poll r1!=#data,repeat last command
			1	1	NA	poll r1!=r0,repeat last command
BL_U	5'h0e	ALL 0	NA	NA	#data	brr #data,?flag (upwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (upwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
BL_D	5'h0f	ALL 0	NA	NA	#data	brr #data,?flag (downwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (downwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
DMA_S	5'h10	NA	NA	NA	#data	set dma_start_addr = #data
DMA_D	5'h11	NA	NA	NA	#data	set dma_end_addr = #data
DMA_DO	5'h12	NA	NA	NA	#data	set dma_length = #data (byte) dma_start
END	5'h13	NA	NA	NA	NA	End of instruction

### 2.4.3 Hardware Trigger Flow

When DCF\_CTRL.vop\_hw\_en is enabled, DCF can be triggered by any of the followed three sources: dma\_finish 、 vop\_standby、 vop\_clkgate\_en.

DCF is edge sensitive for dma\_finish signal, and level sensitive for vop\_standby and vop\_clkgate\_en signal.

When DCF is working, a dcf\_idle is driven to low to indicate vop not to exit vop\_standby status. And when DCF is not working, dcf\_idle is driven to high for SOC and VOP to inquire.

## Chapter 3 NAND Flash Controller (NANDC)

### 3.1 Overview

NAND Flash Controller (NANDC) is used to control data transmission from host to NAND Flash device or from NAND Flash device to host. NANDC is connected to AHB BUS through an AHB Master and an AHB Slave. The data transmission between host and external memory can be done through AHB Master interface or AHB Slave interface.

NANDC supports the following features:

- Software Interface Type
  - Support directly mode
- Flash Interface Type
  - Support Asynchronous Flash Interface with 8bits data width ("Asyn8x" for short)
  - Support 1NAND Flash devices(1 chip select)
- Flash Type
  - Support SLC Flash
- Flash Interface Timing
  - Asyn8x: configurable timing
- BCH/ECC Ability
  - 16bit/1KB BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 1K bytes data and 4 bytes meta-data
- Transmission Ability
  - Support 32K bytes data transmission at a time at most
  - Support two transfer working modes: Bypass or DMA
- Internal Memory
  - 2 built-in SRAMs, and the size is 1k bytes respectively
  - Can be accessed by other masters
  - Can be operated in Ping-Pong mode by other masters
- FIFO Mode
  - One built-in FIFO with 32 bits wide and 8 depth
  - Store command, address and data temporarily that are intend to write to the external NAND Flash

### 3.2 Block Diagram

NANDC comprises with:

- MIF: AHB Master Interface
- SIF: AHB Slave Interface
- SRIF: SRAM Interface
- TRANSC: Transfer Controller
- BCHENC: BCH Encoder
- BCHDEC: BCH Decoder
- FIF\_GEN: Flash Interface Generation

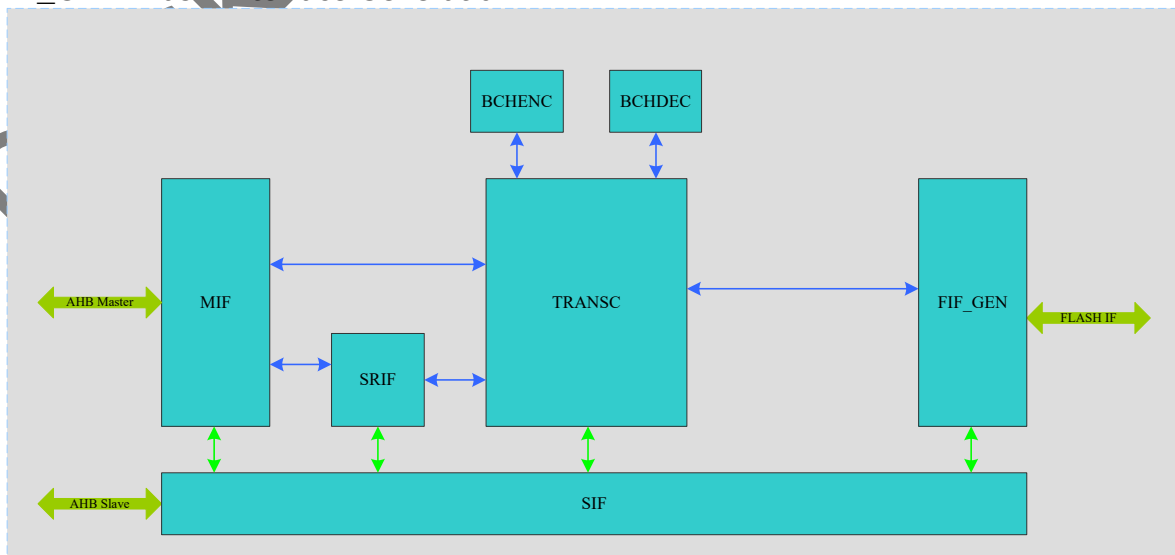


Fig.3-1 NANDC Block Diagram

### 3.3 Function Description

#### 3.3.1 AHB Interface

There is an AHB master interface in NANDC, which is selectable and configurable. It is responsible for transferring data from external memory to internal memory when NAND Flash program, or inverse when NAND Flash read.

There is an AHB slave interface in NANDC. It is responsible for accessing registers and internal memories. The addresses of these registers and memories are listed in Register Description section.

#### 3.3.1 Flash Type/Flash Interface

The NAND Flash controller supports asynchronous 8bitsNAND Flash interface. You can use it by software (configure FMCTL) to suit for devices. Also you can configure their timing parameters by software (configure FMWAIT\_ASYN) to have your desired rate.

#### 3.3.2 BCH Encoder/BCH Decoder

The BCH Encoder is responsible for encoding data to be written into NAND Flash device. The encoded length is 1056 bytes, in which the data length is 1024bytes, system information (Meta-data) is 4bytes, BCH code is 28 bytes.

The BCH Decoder is responsible for decoding data read from NAND Flash device. The decoded length is 1056 bytes, in which the data length is 1024bytes, spare length is 32 bytes.

### 3.4 Register Description

#### 3.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 3-1 NANDC Address Mapping

Base Address[12:8]	Device	Address Length	Offset Address Range
5'b00_00x(x=0, 1)	FLR	512 BYTE	0x0000 ~ 0x01ff
5'b00_01x(x=0, 1)	SPR	512 BYTE	0x0200 ~ 0x03ff
5'b00_10x(x=0, 1)	FLR1	512 BYTE	0x0400 ~ 0x05ff
5'b01_000	Flash0	256 BYTE	0x0800 ~ 0x08ff
5'b10_0xx(x=0, 1)	Sram0	1K BYTE	0x1000 ~ 0x13ff
5'b10_1xx(x=0, 1)	Sram1	1K BYTE	0x1400 ~ 0x17ff
5'b11_000	FIFO	1K BYTE	0x1800 ~ 0x1bff

#### 3.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
NANDC_FMCTL	0x0000	W	0x00000600	NAND Flash Interface Control Register
NANDC_FMWAIT_ASYN	0x0004	W	0x3F3FF7FF	NAND Flash Timing Control Register For Asynchronous Timing
NANDC_FLCTL	0x0008	W	0x00100000	Internal Transfer Control Register
NANDC_BCHCTL	0x000C	W	0x00000008	BCH Control Register
NANDC_MTRANS_CFG	0x0010	W	0x000001D0	Bus Transfer Configuration Register
NANDC_MTRANS_SADDR0	0x0014	W	0x00000000	Start Address Register For Page Data Transmission
NANDC_MTRANS_SADDR1	0x0018	W	0x00000000	Start Address Register For Spare Data Transmission
NANDC_MTRANS_STAT	0x001C	W	0x00000000	Bus Transfer Status Register

Name	Offset	Size	Reset Value	Description
<u>NANDC BCHST0</u>	0x0020	W	0x04000000	BCH Status Register For Code Word 0~1
<u>NANDC BCHST1</u>	0x0024	W	0x00000000	BCH Status Register For Code Word 2~3
<u>NANDC BCHST2</u>	0x0028	W	0x00000000	BCH Status Register For Code Word 4~5
<u>NANDC BCHST3</u>	0x002C	W	0x00000000	BCH Status Register For Code Word 6~7
<u>NANDC BCHST4</u>	0x0030	W	0x00000000	BCH Status Register For Code Word 8~9
<u>NANDC BCHST5</u>	0x0034	W	0x00000000	BCH Status Register For Code Word 10~11
<u>NANDC BCHST6</u>	0x0038	W	0x00000000	BCH Status Register For Code Word 12~13
<u>NANDC BCHST7</u>	0x003C	W	0x00000000	BCH Status Register For Code Word 14~15
<u>NANDC MTRANS_STAT2</u>	0x015C	W	0x00000000	Bus Transfer Status Register2
<u>NANDC VER</u>	0x0160	W	0x00000801	Version Register
<u>NANDC INTEN</u>	0x016C	W	0x00000000	NANDC Interrupt Enable Register
<u>NANDC INTCLR</u>	0x0170	W	0x00000000	NANDC Interrupt Clear Register
<u>NANDC INTST</u>	0x0174	W	0x00000000	NANDC Interrupt Status Register
<u>NANDC SPARE0_0</u>	0x0200	W	0xFFFFFFFF	System Information For Code Word 0
<u>NANDC SPARE1_0</u>	0x0230	W	0xFFFFFFFF	System Information For Code Word 1
<u>NANDC BCHST8</u>	0x0520	W	0x00000000	BCH Status Register For Code Word 16~17
<u>NANDC BCHST9</u>	0x0524	W	0x00000000	BCH Status Register For Code Word 18~19
<u>NANDC BCHST10</u>	0x0528	W	0x00000000	BCH Status Register For Code Word 20~21
<u>NANDC BCHST11</u>	0x052C	W	0x00000000	BCH Status Register For Code Word 22~23
<u>NANDC BCHST12</u>	0x0530	W	0x00000000	BCH Status Register For Code Word 24~25
<u>NANDC BCHST13</u>	0x0534	W	0x00000000	BCH Status Register For Code Word 26~27
<u>NANDC BCHST14</u>	0x0538	W	0x00000000	BCH Status Register For Code Word 28~29
<u>NANDC BCHST15</u>	0x053C	W	0x00000000	BCH Status Register For Code Word 30~31
<u>NANDC FLASH_DATA</u>	0x0800	W	0x00000000	Flash Data
<u>NANDC FLASH_ADDR</u>	0x0804	W	0x00000000	Flash Address

Name	Offset	Size	Reset Value	Description
NANDC_FLASH_CMD	0x0808	W	0x00000000	Command Send To Flash

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 3.4.3 Detail Registers Description

#### **NANDC\_FMCTL**

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	read_delay The number of NANDC clock cycle delays to sample the NAND Flash data after posedge of NAND Flash rdn.
23:14	RO	0x000	reserved
13	RW	0x0	tm Timing mode indication. 1'b0: Asynchronous Mode 1'b1: Reserved
12	RW	0x0	dwidth NAND Flash data bus width indication. 1'b0: 8bits, active in Asynchronous Mode 1'b1: Reserved
11	RO	0x0	reserved
10	RW	0x1	fifo_empty FIFO empty signal. 1'b0: FIFO is not empty. 1'b1: FIFO is empty
9	RO	0x1	frdy NAND Flash ready/busy indicate signal. 1'b0: NAND Flash is busy. 1'b1: NAND Flash is ready. This bit is the sample of the pin of NAND Flash R/Bn
8	RW	0x0	wp NAND Flash write protect. 1'b0: NAND Flash program/erase disabled. 1'b1: NAND Flash program/erase enabled. This bit is output to the pin of NAND Flash WPn
7:1	RO	0x00	reserved
0	RW	0x0	fcs Flash memory chip select control. 1'b1: Hold NAND Flash memory chip select activity 1'b0: NAND Flash memory chip select activity free

#### **NANDC\_FMWAIT\_ASYN**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x3f	reserved
23	RO	0x0	reserved
22:18	RW	0x0f	wait_frdy_dly The number of NANDC clock cycle delays to accept the NAND Flash ready signal.
17:12	RW	0x3f	csrw When in asynchronous mode, this field specifies the number of NANDC clock cycles from the falling edge of NAND Flash CSn to the falling edge of NAND Flash RDn or NAND Flash WRn. The min value of csw is 0.
11	RW	0x0	hard_rdy Hardware handshaking controller bit. When asserted, an external device asserts signal "NAND Flash RDY" to extend a wait-state and the rest bits in this register will be ignored.
10:5	RW	0x3f	rwpw When in asynchronous mode, this field specifies the width of NAND Flash RDn or NAND Flash WRn in NANDC clock cycles, 0x0<=rwpw<=0x3f.
4:0	RW	0x1f	rwcs When in asynchronous mode, this field specifies the number of NANDC clock cycles from the rising edge of NAND Flash RDn or NAND Flash WRn to the rising edge of NAND Flash CSn, 0x0<=rwcs<=0x1f.

**NANDC\_FLCTL**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	bypass_fifo_mode The enable signal for bypass with FIFO mode. 1'b0: Disable FIFO mode 1'b1: Enable FIFO mode
29	RO	0x0	reserved
28	RW	0x0	low_power NANDC low power control 1'b0: Normal mode 1'b1: Low power mode



Bit	Attr	Reset Value	Description
27:22	RW	0x00	<p>page_num Transmission code word number in internal DMA mode(FLCTL[3]) when bus-mode(MTRANS_CFG[2]) is master-mode. 1~32: 1~32 code word. Default: Not support. Notes: a. Only active in internal DMA mode b. Only active when bus-mode is master-mode</p>
21	RW	0x0	<p>page_size Transmission code word size in internal DMA mode. 1'b0: 1024 bytes/code word 1'b1: Reserved</p>
20	RO	0x1	<p>tr_rdy Internal DMA transmission ready indication. 1'b0: Internal DMA transmission is busy. 1'b1: Internal DMA transmission is ready. When reading NAND Flash, tr_rdy should not be set to 1 until all data transmission and correct finished. When programming NAND Flash, tr_rdy should not be set to 1 until all data transmission finished. Notes: Only active in internal DMA mode</p>
19:11	RO	0x000	reserved
10	RW	0x0	<p>cor_able Auto correct enable indication, 1 active. 1'b0: Auto correct disable 1'b1: Auto correct enable Notes: Only active in internal DMA mode.</p>
9:8	RO	0x0	reserved
7	RW	0x0	<p>flash_st_mod Mode for NANDC to start internal data transmission in internal DMA mode. 1'b0: Busy mode. Hardware should not start internal data transmission until NAND Flash is ready even flash_st is asserted. 1'b1: Ready mode. Hardware should start internal data transmission directly when flash_st is asserted. Notes: Only active in internal DMA mode.</p>

Bit	Attr	Reset Value	Description
6:5	RW	0x0	<p>tr_count Transmission code word number in internal DMA mode when bus-mode is slave-mode. 2'b00: 0 code word need transferred 2'b01: 1 code word need transferred 2'b10: 2 code word need transferred 2'b11: Not supported Notes: a. Only active in internal DMA mode. b. Only active when bus-mode is slave-mode.</p>
4	RW	0x0	<p>st_addr Start buffer address. 1'b0: Start transfer from sram0 1'b1: Start transfer from sram1 Notes: Only active in internal DMA mode</p>
3	RW	0x0	<p>bypass NANDC internal DMA bypass indication. 1'b0: Bypass the internal DMA, data are transferred to/from NAND Flash by direct path. 1'b1: Internal DMA active, data are transferred to/from NAND Flash by internal DMA.</p>
2	RW	0x0	<p>flash_st Start signal for NANDC to transfer data between NAND Flash and internal buffer in internal DMA mode. When asserted, it will be cleared automatically. 1'b0: Not start transmission 1'b1: Start transmission Notes: Only active in internal DMA mode. If flash_st_mod=1'b1, the transfer will start as well as flash_st asserts. If flash_st_mod=1'b0, the transfer will start until NAND Flash RDY is ready.</p>
1	RW	0x0	<p>flash_rdn Indicate data flow direction. 1'b0: NANDC read data from NAND Flash. 1'b1: NANDC write data to NAND Flash.</p>
0	RW	0x0	<p>flash_rst NANDC soft reset indication. When asserted, it will be cleared automatically. 1'b0: Not software reset 1'b1: Software reset Notes: Flash_rst should be executed prior to flash_st.</p>

**NANDC BCHCTL**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	bch_toddr Enable signal for storing BCH decode status into ddr in master mode. 1'b0: Disable 1'b1: Enable
27	RO	0x0	reserved
26:19	RW	0x00	bchthres BCH error number threshold. If the number of BCH error exceeds bchthres, the BCH error interrupt will generate.
18	RW	0x0	bchmode1 High bit of BCH mode selection. BchMode=bchmode1, bchmode0. 2'b00: 16bit BCH 2'b01: Reserved 2'b10: Reserved 2'b11: Reserved
17	RO	0x0	reserved
16	RW	0x0	bchpage The data size indication when BCH is active. 1'b0: 1024 bytes, all the 1024 bytes data in code word are valid data to be transferred. 1'b1: 512 bytes, higher 512bytes are valid, and lower 512bytes are invalid and stuffed with 0xff. Notes: a. Only active when data transferred in internal DMA mode. b. Only active for asynchronous NAND Flash
15:8	RW	0x00	addr BCH active range selection. Specify the address for data transmission in bypass mode where the BCH should be active.
7:5	RW	0x0	region BCH active region selection indication. 3'b000: NAND Flash memory 0 region (NAND Flash 0) 3'b010~3'b011: Reserved
4	RW	0x0	bchmode0 BCH mode selection indication. BCH mode is determined by both bchmode0 and bchmode1, detailed information is showed in BCHCTL[18].
3	RW	0x1	bchepd BCH encoder/decoder power down indication. 1'b0: BCH encoder/decoder working 1'b1: BCH encoder/decoder not working

Bit	Attr	Reset Value	Description
2	RW	0x0	mode_addrcaire BCH address care mode selection indication. 1'b0: Address care. 1'b1: Address not care. Notes: This bit is just active for data transmission in bypass mode, but not for command and address transmission. If mode_addrcaire=1'b1, the BCH addr is not effect.
1	RO	0x0	reserved
0	RW	0x0	bchrst BCH software reset indication, When asserted, it will be cleared automatically. 1'b0: Not software reset 1'b1: Software reset Notes: a. BCH Decoder should be software reset before decode begin. b. BCH software reset should be used with NANDC software reset at the same time.

**NANDC MTRANS\_CFG**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	R/W SC	0x0	ahb_rst Ahb master interface software reset, it will be cleared automatically.
14	RW	0x0	fl_pwd NAND Flash power down indication, 1 active. 1'b0: NAND Flash power on, data transferred through master interface is data that to be written into or read from NAND Flash. 1'b1: NAND Flash power down, data transferred through master interface is not data that to be written into or read from NAND Flash. NANDC is just used as DMA for external memory and internal memory.
13:9	RW	0x00	incr_num AHB Master incr num indication. incr_num=1~16. When burst=001, software should configure incr_num. Notes: Only active for master-mode

Bit	Attr	Reset Value	Description
8:6	RW	0x7	burst AHB Master burst type indication. 3'b000: Single transfer 3'b011: 4-beat burst 3'b101: 8-beat Burst 3'b111: 16-beat burst default: Not supported Notes: Only active for master-mode
5:3	RW	0x2	hsize AHB Master data size indication: 3'b000: 8 bits 3'b001: 16 bits 3'b010: 32 bits default: Not supported Notes: Only active for master-mode
2	RW	0x0	bus_mode Bus interface selection. 1'b0: Slave interface. NAND Flash data is transferred through slave interface. 1'b1: Master interface. NAND Flash data is transferred through master interface.
1	RW	0x0	ahb_wr Data transfer direction through master interface. 1'b0: Read direction (external memory -> internal memory) 1'b1: Write direction (internal memory -> external memory) Notes: a. Only active for master-mode. b. When read NAND Flash (flash_rdn=0), ahb_wr=1. When program NAND Flash (flash_rdn=1), ahb_wr=0.
0	RW	0x0	ahb_wr_st Start indication for loading data from external memory to internal memory or storing data from internal memory to external memory through master. When asserted, it will be automatically cleared only active when fl_pwd is 1. Notes: a. Only active for master-mode and fl_pwd=1. b. When fl_pwd=0, NAND Flash is active, NANDC start to transfer data through master interface if flash_st=1 c. When fl_pwd=1, NAND Flash is not active, NANDC start to transfer data through master interface if ahb_wr_st=1

**NANDC MTRANS SADDR0**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr0 Start address for page data transmission. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

**NANDC MTRANS SADDR1**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr1 Start address for spare data transmission. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

**NANDC MTRANS STAT**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	mtrans_cnt Finished counter for code word transmission through Master interface. Notes: Only active for master-mode
15:0	RW	0x0000	bus_err Bus error indication for code word 0~15. [0]: bus error for code word 0 ..... [15]: bus error for code word 15 Notes: Only active for master-mode

**NANDC BCHST0**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum1_h1 Highest bit of err_hnum1
29	RO	0x0	err_tnum1_h1 Highest bit of err_tnum1
28	RO	0x0	err_hnum0_h1 Highest bit of err_hnum0
27	RO	0x0	err_tnum0_h1 Highest bit of err_tnum0

Bit	Attr	Reset Value	Description
26	RO	0x1	bchrdy Ready indication for BCH encoder/decoder, 1 active. 1'b0: BCH encoder/decoder is busy. 1'b1: BCH encoder/decoder is ready.
25:21	RO	0x00	err_hnum1_15 Lower 5 bits of number of error bits found in first 512bytes of 1st backup code word.
20:16	RO	0x00	err_tnum1_15 Lower 5 bits of number of error bits found in 1st backup code word.
15	RO	0x0	fail1 Indication for the 1st backup code word decoded failed or not. 1'b0: Decode successfully 1'b1: Decode fail
14	RO	0x0	done1 Indication for finishing decoding the 1st backup code word. 1'b0: Not finished 1'b1: Finished
13	RW	0x0	errf1 Indication for error found in 1st backup code word. 1'b0: No error 1'b1: Error found
12:8	RW	0x00	err_hnum0_15 Lower 5 bits of number of error bits found in first 512bytes of current backup code word.
7:3	RO	0x00	err_tnum0_15 Lower 5 bits of number of error bits found in current backup code word.
2	RO	0x0	fail0 Indication for current backup code word decode fail or not. 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	done0 Indication for finishing decoding the current backup code word. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf0 Indication for error found in current backup code word. 1'b0: No error 1'b1: Error found

**NANDC BCHST1**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RO	0x0	err_hnum3_h1 Highest bit of err_hnum3
29	RO	0x0	err_tnum3_h1 Highest bit of err_tnum3
28	RO	0x0	err_hnum2_h1 Highest bit of err_hnum2
27	RO	0x0	err_tnum2_h1 Highest bit of err_tnum2
26	RO	0x0	reserved
25:21	RO	0x00	err_hnum3_l5 Lower 5 bits of number of error bits found in first 512bytes of 3th backup code word.
20:16	RO	0x00	err_tnum3_l5 Lower 5 bits of number of error bits found in 3th backup code word.
15	RW	0x0	fail3 Indication for the 3th backup code word decoded failed or not. 1'b0: Decode successfully 1'b1: Decode fail
14	RO	0x0	done3 Indication for finishing decoding the 3th backup code word. 1'b0: Not finished 1'b1: Finished
13	RO	0x0	errf3 Indication for error found in 3th backup code word. 1'b0: No error 1'b1: Error found
12:8	RO	0x00	err_hnum2_l5 Lower 5 bits of number of error bits found in first 512bytes of 2th backup code word.
7:3	RO	0x00	err_tnum2_l5 Lower 5 bits of number of error bits found in 2th backup code word.
2	RO	0x0	fail2 Indication for 2th backup code word decode failed or not. 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	done2 Indication for finishing decoding the 2th backup code word. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf2 Indication for error found in 2th backup code word. 1'b0: No error 1'b1: Error found



**NANDC\_BCHST2**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd4_cwd5 BCHST information for 4th and 5th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST3**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd6_cwd7 BCHST information for 6th and 7th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST4**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd8_cwd9 BCHST information for 8th and 9th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST5**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd10_cwd11 BCHST information for 10th and 11th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST6**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd12_cwd13 BCHST information for 12th and 13th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST7**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd14_cwd15 BCHST information for 14th and 15th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_MTRANS\_STAT2**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	bus_err2 Bus error indication for code word16~31. [0]: bus error for code word 16 ..... [15]: bus error for code word 31 Notes: Only active for master-mode

**NANDC\_VER**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000801	version Version indication for NANDC

**NANDC\_INTEN**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	reserved
6	RW	0x0	master_idle_int_en Enable for master idle interrupt. 1'b0: Interrupt disable 1'b1: Interrupt enable When master_idle_int_en is active, an interrupt is generated if posedge of master idle happen.
5:4	RO	0x0	reserved
3	RW	0x0	bchfail_int_en Enable for BCH fail interrupt. 1'b0: Interrupt disable 1'b1: Interrupt enable When bchfail_int_en is active, an interrupt is generated if BCH decode failed.
2	RW	0x0	bcherr_int_en Enable for BCH error interrupt. 1'b0: Interrupt disable 1'b1: Interrupt enable When bcherr_int_en is active, an interrupt is generated if BCH decode error bit is larger than bcthres(BCHCTL[26:19]).

Bit	Attr	Reset Value	Description
1	RW	0x0	frdy_int_en Enable for flash_rdy interrupt. 1'b0: Interrupt disable 1'b1: Interrupt enable When frdy_int_en is active, an interrupt is generated if NAND Flash R/B# changes from 0 to 1.
0	RW	0x0	dma_int_en Enable for internal DMA transfer finished interrupt. 1'b0: Interrupt disable 1'b1: Interrupt enable When dma_int_en is active, an interrupt is generated if page_num(FLCTL[27:22]) of NAND Flash data transfer in DMA mode is finished.

**NANDC\_INTCLR**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	R/W SC	0x0	master_idle_int_clr Clear for master idle interrupt. When asserted, this bit will be cleared automatically. 1'b0: Interrupt not cleared 1'b1: Interrupt cleared
5:4	RO	0x0	reserved
3	R/W SC	0x0	bchfail_int_clr Clear for BCH decode fail interrupt. When asserted, this bit will be cleared automatically. 1'b0: Interrupt cleared 1'b1: Interrupt not cleared
2	R/W SC	0x0	bcherr_int_clr Clear for BCH error interrupt. When asserted, this bit will be cleared automatically. 1'b0: Interrupt cleared 1'b1: Interrupt not cleared
1	R/W SC	0x0	frdy_int_clr Clear for flash_rdy interrupt. When asserted, this bit will be cleared automatically. 1'b0: Interrupt cleared 1'b1: Interrupt not cleared
0	R/W SC	0x0	dma_int_clr Clear for internal DMA transfer finished interrupt. When asserted, this bit will be cleared automatically. 1'b0: Interrupt cleared 1'b1: Interrupt not cleared

**NANDC\_INTST**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	master_idle_int_stat Status for master idle interrupt, high active.
5:4	RO	0x0	reserved
3	RO	0x0	bchfail_int_stat Status for BCH decode fail interrupt, high active.
2	RO	0x0	bcherr_int_stat Status for BCH error interrupt, high active.
1	RO	0x0	frdy_int_stat Status for flash_rdy interrupt, high active.
0	RO	0x0	dma_int_stat Status for internal DMA transfer finished interrupt, high active.

**NANDC\_SPARE0\_0**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 The 4th system byte of code word 0.
23:16	RW	0xff	system_2 The 3rd system byte of code word 0.
15:8	RW	0xff	system_1 The 2nd system byte of code word 0.
7:0	RW	0xff	system_0 The 1st system byte of code word 0.

**NANDC\_SPARE1\_0**

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 The 4th system byte of code word 1.
23:16	RW	0xff	system_2 The 3rd system byte of code word 1.
15:8	RW	0xff	system_1 The 2nd system byte of code word 1.
7:0	RW	0xff	system_0 The 1st system byte of code word 1.

**NANDC\_BCHST8**

Address: Operational Base + offset (0x0520)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd16_cwd17 BCHST information for 16th and 17th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST9**

Address: Operational Base + offset (0x0524)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd18_cwd19 BCHST information for 18th and 19th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST10**

Address: Operational Base + offset (0x0528)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd20_cwd21 BCHST information for 20th and 21th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST11**

Address: Operational Base + offset (0x052C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd22_cwd23 BCHST information for 22th and 23th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST12**

Address: Operational Base + offset (0x0530)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd24_cwd25 BCHST information for 24th and 25th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC\_BCHST13**

Address: Operational Base + offset (0x0534)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd26_cwd27 BCHST information for 26th and 27th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC BCHST14**

Address: Operational Base + offset (0x0538)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd28_cwd29 BCHST information for 28th and 29th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC BCHST15**

Address: Operational Base + offset (0x053C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd30_cwd31 BCHST information for 30th and 31th backup code word. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

**NANDC FLASH DATA**

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	flash_data Valid for bypass internal dma mode(FLCTL[3]=0).

**NANDC FLASH ADDR**

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flash_addr Page or block address send to NAND Flash for bypass internal dma mode.

**NANDC FLASH CMD**

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flash_cmd Contains the command write to flash for bypass internal dma mode.

**3.5 Interface Description**

Table 3-2 NANDC Interface Description

Module Pin	Direction	PIN Name	IOMUX Setting
flash_ale	O	FLASH_ALE/FSPI_D0/I2S1_LRCK_M0/GPIO1_A0_d	GRF_GPIO1A_IOMUX_L[2:0]=3'b001
flash_cle	O	FLASH_CLE/EMMC_CLKO/GPIO0_D7_d	GRF_GPIO0D_IOMUX_H[14:12]=3'b001
flash_wrn	O	FLASH_WRn/EMMC_CMD/GPIO0_D5_u	GRF_GPIO0D_IOMUX_H[6:4]=3'b001
flash_rdn	O	FLASH_RDn/FSPI_D3/I2S1_SDI_M0/GPIO1_A2_u	GRF_GPIO1A_IOMUX_L[10:8]=3'b001
flash_data[0]	I/O	FLASH_D0/EMMC_D0/GPIO0_C4_u	GRF_GPIO0C_IOMUX_H[2:0]=3'b

Module Pin	Direction	PIN Name	IOMUX Setting
			001
flash_data[1]	I/O	FLASH_D1/EMMC_D1/GPIO0_C5_u	GRF_GPIO0C_IOMUX_H[6:4]=3'b001
flash_data[2]	I/O	FLASH_D2/EMMC_D2/GPIO0_C6_u	GRF_GPIO0C_IOMUX_H[10:8]=3'b001
flash_data[3]	I/O	FLASH_D3/EMMC_D3/GPIO0_C7_u	GRF_GPIO0C_IOMUX_H[14:12]=3'b001
flash_data[4]	I/O	FLASH_D4/EMMC_D4/GPIO0_D0_u	GRF_GPIO0D_IOMUX_L[2:0]=3'b001
flash_data[5]	I/O	FLASH_D5/EMMC_D5/FSPI_CS1n/GPIO0_D1_u	GRF_GPIO0D_IOMUX_L[6:4]=3'b001
flash_data[6]	I/O	FLASH_D6/EMMC_D6/GPIO0_D2_u	GRF_GPIO0D_IOMUX_L[10:8]=3'b001
flash_data[7]	I/O	FLASH_D7/EMMC_D7/GPIO0_D3_u	GRF_GPIO0D_IOMUX_L[14:12]=3'b001
flash_rdy	I	FLASH_RDYn/FSPI_D1/I2S1_SCLK_M0/GPIO1_A1_u	GRF_GPIO1A_IOMUX_L[6:4]=3'b001
flash_csn0	O	FLASH_CS0n/FSPI_CS0n/I2S1_MCLK_M0/GPIO0_D4_u	GRF_GPIO0D_IOMUX_H[2:0]=3'b001
flash_wp	O	FLASH_WPn/EMMC_RSTn/FSPI_CLK/GPIO1_A3_d	GRF_GPIO1A_IOMUX_L[14:12]=3'b001

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different NAND Flash interface, which is shown as follows.

Table 3-3 NANDC Interface Connection

Module Pin	Direction	Flash Interface			
		Asyn8x	Asyn16x	ONFI	Toggle
flash_csni(i=0)	O	√	-	-	-
flash_ale	O	√	-	-	-
flash_cle	O	√	-	-	-
flash_wrn	O	√	-	-	-
flash_rdn	O	√	-	-	-
flash_data[7:0]	I/O	√	-	-	-
flash_rdy	I	√	-	-	-

## 3.6 Application Notes

### 3.6.1 BCHST/BCHLOC/BCHDE/SPARE Application

#### 1. BCHST

There are 16 BCHST-registers in NANDC to store 32codeword's BCH decode status(bchst) information. Every register stores 2 codeword's bchst information except BCHST0, which not only includes bchst information, but also includes one bit for *bchrdy*.

Let bchst\_cwd0~bchst\_cwd31 be the bchst information for 32codewords. In BCHST-registers, the latest codeword's bchst is stored into bchst\_cwd0, and the former is shifted into bchst\_cwd1. That is, bchst\_cwd0→ bchst\_cwd1 →.....→bchst\_cwd31. Therefore, for example, if 32codewords are decoded, then bchst\_cwd0 is the bch decode status for codeword31, and bchst\_cwd31 is the bch decode status for codeword0.

bchst\_cwd0 = {BCHST0[28], BCHST0[12:8], BCHST0[27], BCHST0[7:3], BCHST0[2:0]}

bchst\_cwd1 = {BCHST0[30], BCHST0[25:21], BCHST0[29], BCHST0[20:16], BCHST0[15:13]}

bchst\_cwd2 = {BCHST1[28], BCHST1[12:8], BCHST1[27], BCHST1[7:3], BCHST1[2:0]}

bchst\_cwd3 = {BCHST1[30], BCHST1[25:21], BCHST1[29], BCHST1[20:16], BCHST1[15:13]}

bchst\_cwd4 = {BCHST2[28], BCHST2[12:8], BCHST2[27], BCHST2[7:3], BCHST2[2:0]}

bchst\_cwd5 = {BCHST2[30], BCHST2[25:21], BCHST2[29], BCHST2[20:16], BCHST2[15:13]}

bchst\_cwd6 = {BCHST3[28], BCHST3[12:8], BCHST3[27], BCHST3[7:3], BCHST3[2:0]}

bchst\_cwd7 = {BCHST3[30], BCHST3[25:21], BCHST3[29], BCHST3[20:16], BCHST3[15:13]}

bchst\_cwd8 = {BCHST4[28], BCHST4[12:8], BCHST4[27], BCHST4[7:3], BCHST4[2:0]}

bchst\_cwd9 = {BCHST4[30], BCHST4[25:21], BCHST4[29], BCHST4[20:16], BCHST4[15:13]}

bchst\_cwd10 = {BCHST5[28], BCHST5[12:8], BCHST5[27], BCHST5[7:3], BCHST5[2:0]}

bchst\_cwd11 = {BCHST5[30], BCHST5[25:21], BCHST5[29], BCHST5[20:16],  
 BCHST5[15:13]}  
 bchst\_cwd12 = {BCHST6[28], BCHST6[12:8], BCHST6[27], BCHST6[7:3], BCHST6[2:0]}  
 bchst\_cwd13 = {BCHST6[30], BCHST6[25:21], BCHST6[29], BCHST6[20:16],  
 BCHST6[15:13]}  
 bchst\_cwd14 = {BCHST7[28], BCHST7[12:8], BCHST7[27], BCHST7[7:3], BCHST7[2:0]}  
 bchst\_cwd15 = {BCHST7[30], BCHST7[25:21], BCHST7[29], BCHST7[20:16],  
 BCHST7[15:13]}  
 bchst\_cwd16 = {BCHST8[28], BCHST8[12:8], BCHST8[27], BCHST8[7:3], BCHST8[2:0]}  
 bchst\_cwd17 = {BCHST8[30], BCHST8[25:21], BCHST8[29], BCHST8[20:16],  
 BCHST8[15:13]}  
 bchst\_cwd18 = {BCHST9[28], BCHST9[12:8], BCHST9[27], BCHST9[7:3], BCHST9[2:0]}  
 bchst\_cwd19 = {BCHST9[30], BCHST9[25:21], BCHST9[29], BCHST9[20:16],  
 BCHST9[15:13]}  
 bchst\_cwd20 = {BCHST10[28], BCHST10[12:8], BCHST10[27], BCHST10[7:3],  
 BCHST10[2:0]}  
 bchst\_cwd21 = {BCHST10[30], BCHST10[25:21], BCHST10[29], BCHST10[20:16],  
 BCHST10[15:13]}  
 bchst\_cwd22 = {BCHST11[28], BCHST11[12:8], BCHST11[27], BCHST11[7:3],  
 BCHST11[2:0]}  
 bchst\_cwd23 = {BCHST11[30], BCHST11[25:21], BCHST11[29], BCHST11[20:16],  
 BCHST11[15:13]}  
 bchst\_cwd24 = {BCHST12[28], BCHST12[12:8], BCHST12[27], BCHST12[7:3],  
 BCHST12[2:0]}  
 bchst\_cwd25 = {BCHST12[30], BCHST12[25:21], BCHST12[29], BCHST12[20:16],  
 BCHST12[15:13]}  
 bchst\_cwd26 = {BCHST13[28], BCHST13[12:8], BCHST13[27], BCHST13[7:3],  
 BCHST13[2:0]}  
 bchst\_cwd27 = {BCHST13[30], BCHST13[25:21], BCHST13[29], BCHST13[20:16],  
 BCHST13[15:13]}  
 bchst\_cwd28 = {BCHST14[28], BCHST14[12:8], BCHST14[27], BCHST14[7:3],  
 BCHST14[2:0]}  
 bchst\_cwd29 = {BCHST14[30], BCHST14[25:21], BCHST14[29], BCHST14[20:16],  
 BCHST14[15:13]}  
 bchst\_cwd30 = {BCHST15[28], BCHST15[12:8], BCHST15[27], BCHST15[7:3],  
 BCHST15[2:0]}  
 bchst\_cwd31 = {BCHST15[30], BCHST15[25:21], BCHST15[29], BCHST15[20:16],  
 BCHST15[15:13]}

## 2. SPARE

SPARE includes two register-groups, SPARE0 and SPARE1. Each group has 8 registers: SPARE0\_0~SPARE0\_7 and SPARE1\_0~SPARE1\_7. Only SPARE0\_0 and SPARE1\_0 can be accessed via software, others are used internally.

When in bch encoding, SPARE0\_0 stores system information for codeword in sram0, SPARE0\_n(n=1~7) stores encode information for codeword in sram0; SPARE1\_0 stores system information for codeword in sram1, SPARE1\_n( n=1~7) stores encode information for codeword in sram1.

When in bch decoding, SPARE0\_n(n=0~7) stores the spare data read from NAND Flash for codeword in sram0 if BCHCTL[28]=0, the bch decode status(BCHST) information which reflects the current codeword will be written into ddr instead of SPARE0\_1 if BCHCTL[28]=1; SPARE1\_n(n=0~7) stores the spare data read from NAND Flash for codeword in sram1 if BCHCTL[28]=0, the bch decode status(BCHST) information which reflects the current codeword will be written into ddr instead of SPARE1\_1 if BCHCTL[28]=1.

### 3.6.2 Bus Mode Application

MTRANS\_CFG[2] determines whether the data load/store between internal memory and external memory is through slave interface or master interface.

#### 1. Slave Mode

When MTRANS\_CFG[2]=0, slave is selected. i. e. ,NAND Flash data load/store between



internal memory and external memory is through slave interface by CPU or external DMA. In this mode, software should store page data into internal memory and spare data into SPARE registers before starting NAND Flash program operation; and should load page data from internal memory and spare data from SPARE registers after finishing NAND Flash read operation.

In this mode, MTRANS\_CFG, MTRANS\_SADDR0 and MTRANS\_SADDR1 are unused. The transfer codeword number is determined by FLCTL[6:5], and the maximum number is 2. The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transfer is finished.

## 2. Master Mode

When MTRANS\_CFG[2]=1, master is selected. i. e. ,NAND Flash data load/store between internal memory and external memory is through master interface.

In this mode, software should initialize page data and spare data into external memory, and set their addresses in MTRANS\_SADDR0 and MTRANS\_SADDR1 respectively before starting NAND Flash program operation. Similarly, software should configure MTRANS\_SADDR0 and MTRANS\_SADDR1 respectively before starting NAND Flash read operation and could read data from addresses in MTRANS\_SADDR0 and MTRANS\_SADDR1 after NANDC transfer finish.

In this mode, MTRANS\_CFG, MTRANS\_SADDR0 and MTRANS\_SADDR1 are used. The transfer codeword number is determined by FLCTL[26:22], and the maximum number is 32. The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transmission is finished.

When MTRANS\_CFG[2]=1, page data and spare data are stored in the continuous space of external memory respectively.

For page data, source address is named Saddr0, specified in MTRANS\_SADDR0. The space can be divided into many continuous units, and the unit size(named PUnit) is 1024 bytes.

For spare data, source address is named Saddr1, specified in MTRANS\_SADDR1. The space can be divided into many continuous units, and the unit size(named SUnit) is 64 bytes for 16 bits BCH mode.

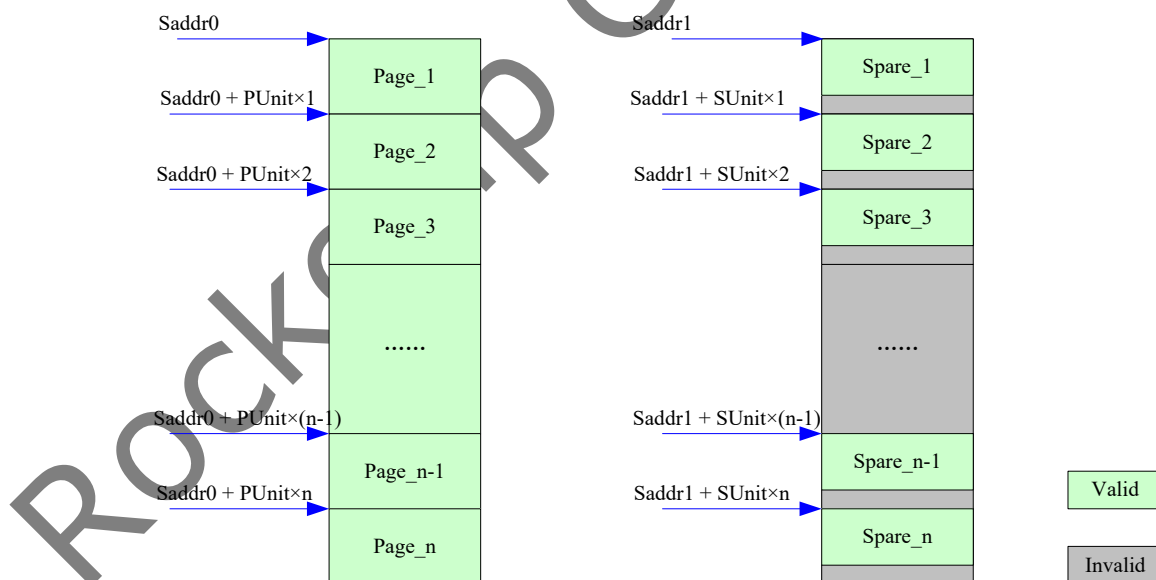


Fig.3-2 NANDC Address Assignment

The detailed format for page data and spare data in every unit is shown in following figures.

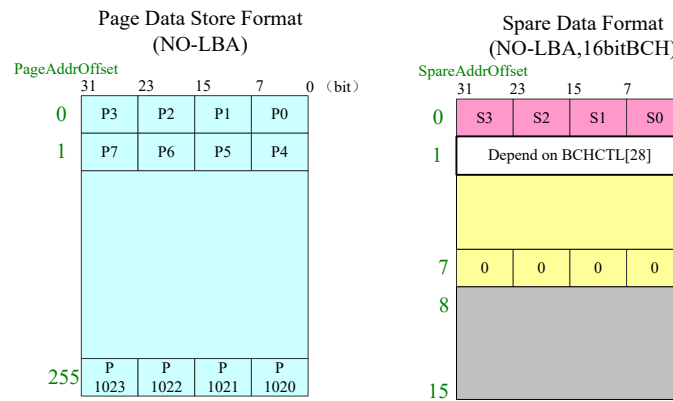


Fig.3-3 NANDC Data Format

### 3.6.3 BchPage Application

BCHCTL[16] determines whether codeword size for page data is 1024 bytes or 512 bytes when FLCTL[11] is 0.

#### 1. 1024bytes

When BCHCTL[16]=0, BchPage=0, hardware needs to write 1024 bytes page data and spare data into NAND Flash or read 1024 bytes page data and spare data from NAND Flash. All the 1024 bytes page data and spare data are encoded when writing or decoded when reading.

#### 2. 512bytes

When BCHCTL[16]=1, BchPage=1, hardware needs to write 512 bytes page data and spare data into NAND Flash or read 512 bytes page data and spare data from NAND Flash.

In this mode, the page data unit size for BCH encoder and BCH decoder still is 1024byte. So to support BCH encoder and decoder, software should configure page data as follows:

1th~512th bytes are invalid data which must be stuffed with 0xff, 513th~1024th bytes are valid page data.

### 3.6.4 PageSize/SpareSize Application

#### 1. Big Page

When FLCTL[11]=0(LbaEn=0), the NAND Flash to be operated is Raw NAND Flash. Every codeword size is 1024 bytes and FLCTL[21] should always be set to 0, and the PageStep in external memory is 1024 bytes if bus mode is master mode.

At this mode, the spare size and SpareStep in external memory are determined by BCH Mode as follows:

BCH Mode=16bitBCH: spare size=(28+4)bytes , SpareStep=64bytes

#### 2. Small Page

The NAND Flash controller will not operate in LBA mode, so small page with 512 bytes for a codeword is not supported.

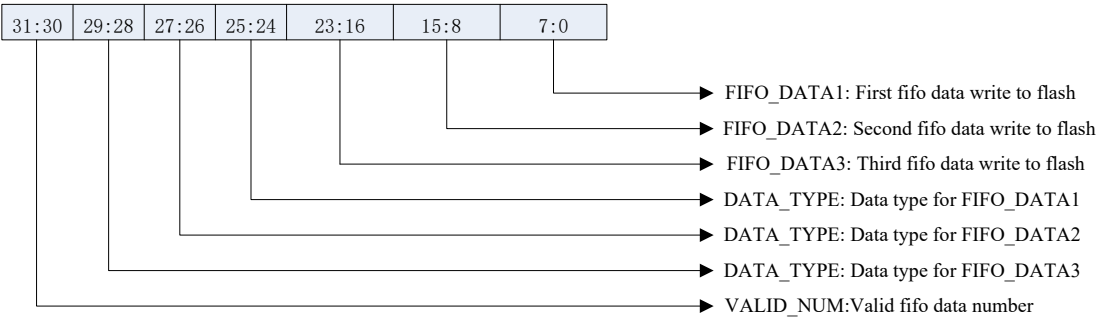
### 3.6.5 NANDC Interrupt Application

NANDC has 1 interrupt output signal and 5 interrupt sources: DMA finish interrupt source, NAND Flash ready interrupt source, bch error interrupt source, bchfail interrupt source and master idle interrupt source. When one or more of these interrupt source are enabled, NANDC interrupt is asserted if one or more interrupt source is high. Software can determine the interrupt source by reading INTST and clear interrupt by writing corresponding bit in INTCLR.

### 3.6.6 FIFO Application

FIFO in NANDC is used to store command, address and data temporarily that are intend to write to the external NAND Flash. The FIFO is 32-bit wide and 8-location deep, user can access it by configuring the NANDC to work on bypass(FLCTL[3]=1) and FIFO enable(FLCTL[30]=1) mode.

The format of data written into FIFO is as follows.



DATA\_TYPE:  
2'b00/2'b11 : flash data  
2'b10 : flash command  
2'b01 : flash address

Fig.3-4 FIFO Data Format

Command, address or data write to external NAND Flash are pushed into FIFO first and popup automatically if the FIFO is not empty. Then FIFO\_DATA1, FIFO\_DATA2 and FIFO\_DATA3 are written to NAND Flash by NANDC in order. The method to determine the end of write operation is to read register FMCTL. If FMCTL[10] is set , it means that the FIFO is empty and NAND Flash write operation is over.

## Chapter 4 Video Output Processor (VOP\_LITE)

### 4.1 Overview

Video Output Processor is a video process engine and a display interface from memory frame buffer to display device (LCD panel, MIPI, BT1120, RGB, MCU, ect). VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface.

#### 4.1.1 Features

VOP\_LITE supports the following features:

- Display interface
  - Parallel RGB LCD Interface: 24-bit(RGB888),18-bit(RGB666), 16-bit(RGB565)
  - Serial RGB LCD Interface
  - MCU LCD Interface
  - Max output resolution
    - ◆ 1920x1080 for RGB/MIPI/BT1120
- Display process
  - Background layer
    - ◆ programmable 24-bit color
  - Win0 layer
    - ◆ RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - ◆ 1/8 to 8 scaling-down and scaling-up engine(1/8 and 8 are not included)
    - ◆ Support virtual display
    - ◆ 256 level alpha blending (pre-multiplied alpha support)
    - ◆ Transparency color key
    - ◆ YCbCr2RGB (rec601-mpeg/ rec601-jpeg/rec709)
    - ◆ RGB2YCbCr(BT601/BT709)
  - Win2 layer
    - ◆ RGB888, ARGB888, RGB565
    - ◆ Support virtual display
    - ◆ 256 level alpha blending (pre-multiplied alpha support)
    - ◆ Transparency color key
    - ◆ RGB2YCbCr(BT601/BT709)
    - ◆ Support multi-region
- Others
  - Win0 layer and Win2 layer overlay exchangeable
  - Support RGB or YUV domain overlay
  - BCSH (Brightness, Contrast, Saturation, Hue adjustment)
  - BCSH: YCbCr2RGB (rec601-mpeg/ rec601-jpeg/rec709)
  - BCSH: RGB2YCbCr(BT601/BT709)
  - Support Gamma adjust for PAD
  - Support dither down allegro RGB888to666 RGB888to565 & dither down frc (configurable) RGB888to666
  - Blank and black display
  - Standby mode
  - Support NOC hurry for higher bus priority for win0 Support DMA stop mode
  - Support all layers reg\_done separately

### 4.2 Block Diagram

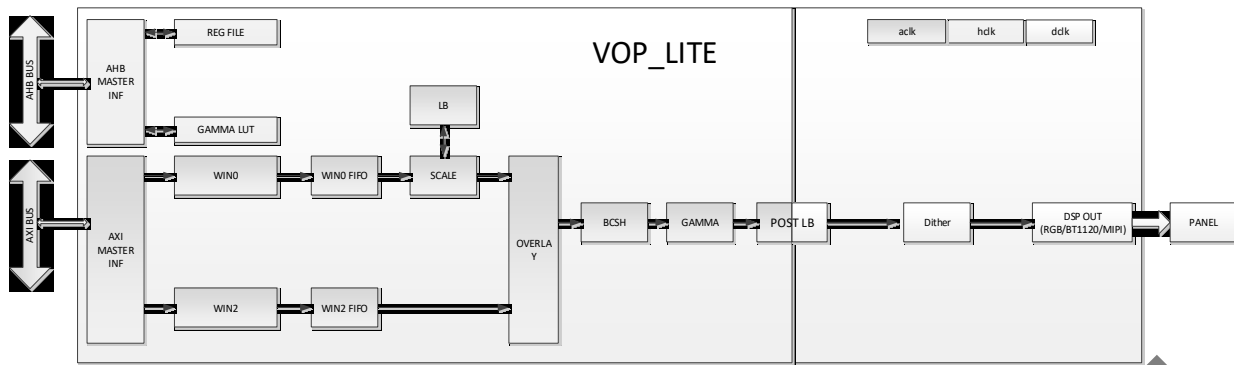


Fig.4-1 VOP Block Diagram

## 4.3 Function Description

### 4.3.1 Data Format

VOP master read the frame data from the frame buffer in the system memory. There are total 6 formats supported in two layers.

- Win0: RGB888, ARGB888, RGB565, YCbCr422\_SP, YCbCr420\_SP, YCbCr444\_SP
- Win2: RGB888, ARGB888, RGB565

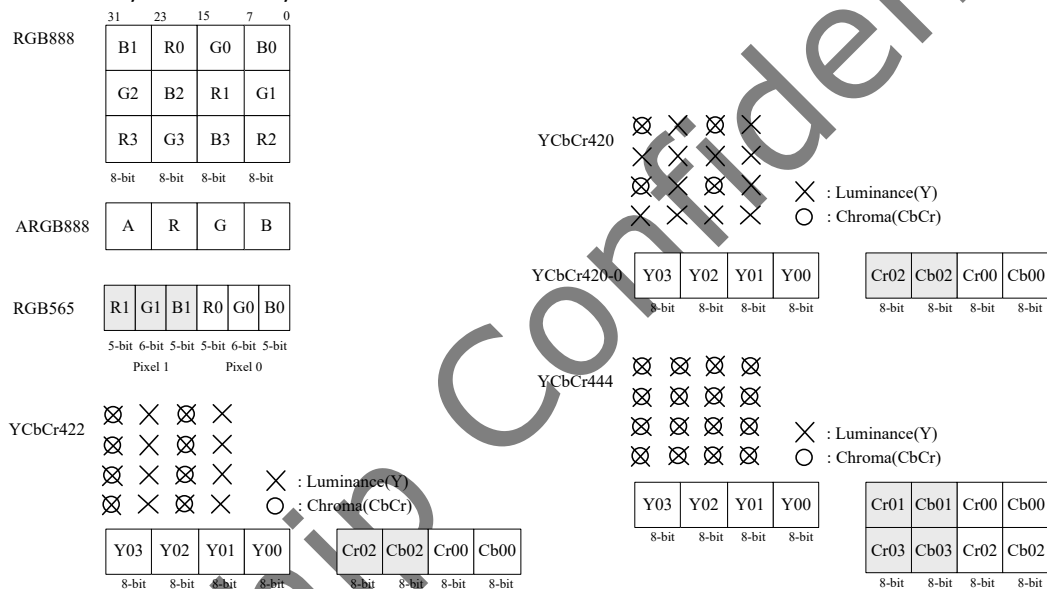


Fig.4-2 VOP Frame Buffer Data Format

### Data SWAP function

There are several swap options for different frame data formats. All the data swap types are in the following table.

Table 4-1 VOP Data Swap of Win0 and Win2

Data-swap	RB swap	Alpha swap	Y-M8 swap	CbCr swap
Win0	yes	yes	yes	yes
Win2	yes	yes	No	No

### 4.3.2 Data path

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for all the display layers. Data fetching is driven by display output requirement.

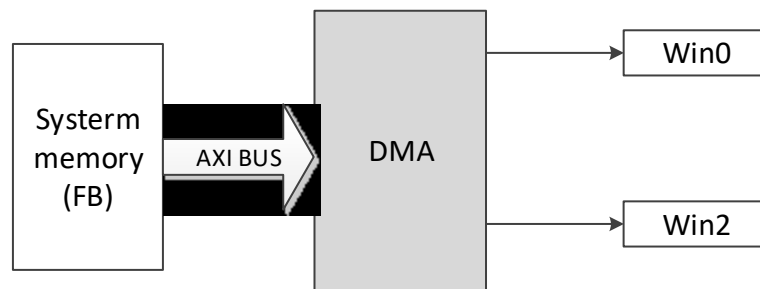


Fig.4-3 VOP Internal DMA

### 4.3.3 Virtual display

Virtual display is supported in Win0 and Win2. The active image is part of the virtual (original) image in frame buffer memory. The virtual width is indicated by setting WIN0/WIN2\_VIR\_STRIDE for different data format.

The virtual stride should be multiples of word (32-bit). That means dummy bytes in the end of virtual line if the real pixels are not 32-bit aligned.

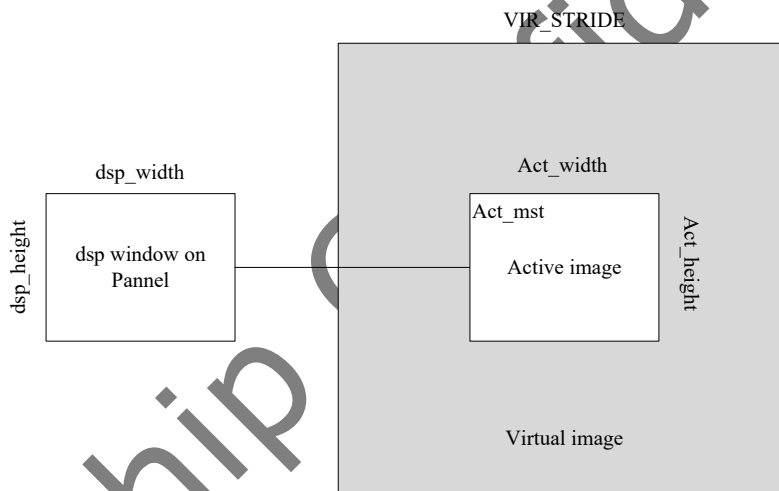


Fig.4-4 VOP Virtual Display Mode

### 4.3.4 Scaling

The scaling operation is the image resizing process of data transfer from the frame buffer memory to LCD panel or TV set.

Horizontal and vertical scaling factor should be set according the window scaling ratio.

#### 1. Scaling factor

Because the Chroma data may have different sampling rate with Luma data in the memory format of YCbCr422/YCbCr420. The scaling factor of Win0 has two couples of factor registers:

VOP\_WIN0\_SCL\_FACTOR\_Y/VOP\_WIN0\_SCL\_FACTOR\_CBR

Software calculates the scaling factor value using the following equations:

$$y\_rgb\_vertical\_factor = \left( \frac{VOP\_WIN0\_ACT\_INFO[31:16]}{VOP\_WIN0\_DSP\_INFO[31:16]} \right) \times 2^{12}$$

$$y\_rgb\_horizontal\_factor = \left( \frac{VOP\_WIN0\_ACT\_INFO[15:0]}{VOP\_WIN0\_DSP\_INFO[15:0]} \right) \times 2^{12}$$

$$yuv422\_yuv444\_Cbr\_vertical\_factor = \left( \frac{VOP\_WIN0\_ACT\_INFO[31:16]}{VOP\_WIN0\_DSP\_INFO[31:16]} \right) \times 2^{12}$$

$$yuv420\_Cbr\_vertical\_factor = \left( \frac{VOP\_WIN0\_ACT\_INFO[31:16]/2}{VOP\_WIN0\_DSP\_INFO[31:16]} \right) \times 2^{12}$$

$$yuv444\_Cbr\_horizontal\_factor = \left( \frac{VOP\_WIN0\_ACT\_INFO[15:0]}{VOP\_WIN0\_DSP\_INFO[15:0]} \right) \times 2^{12}$$

$$yuv422\_yuv420\_Cbr\_horizontal\_factor = \left( \frac{VOP\_WIN0\_ACT\_INFO[15:0]/2}{VOP\_WIN0\_DSP\_INFO[15:0]} \right) \times 2^{12}$$

## 2. Scaling start point offset

The x and y start point of the generated pixels can be adjusted, the offset value is in the range of 0 to 0.99.

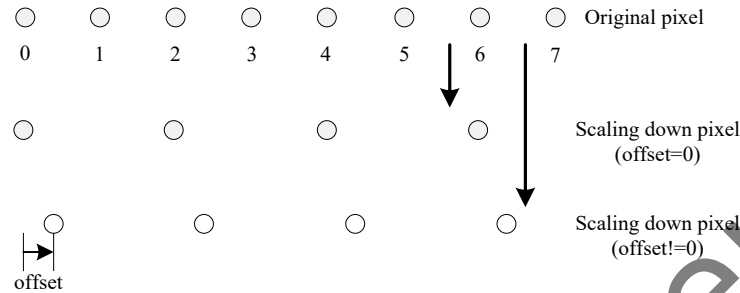


Fig.4-5 VOP Scaling Down Offset

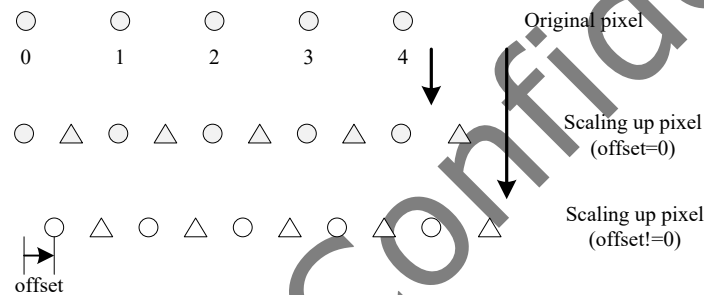


Fig.4-6 VOP Scaling Up Offset

Table 4-2 VOP Scaling Start Point Offset Registers

scaling down/up start point offset	Offset variable	Register
Win0 YRGB vertical scaling offset	Win0_YRGB_vscl_offset	Win0_SCL_OFFSET [32:24]
Win0 YRGB horizontal scaling offset	Win0_YRGB_hscl_offset	Win0_SCL_OFFSET [23:16]
Win0 Cbr vertical scaling offset	Win0_CBR_vscl_offset	Win0_SCL_OFFSET [15:8]
Win0 Cbr horizontal scaling offset	Win0_CBR_hscl_offset	Win0_SCL_OFFSET [7:0]

## 4.3.5 Overlay

### 1. Overlay display

There are totally 3 layers for overlay display: Background, Win0, Win2.

The background is a programmable solid color layer, which is always the bottom of the display screen.

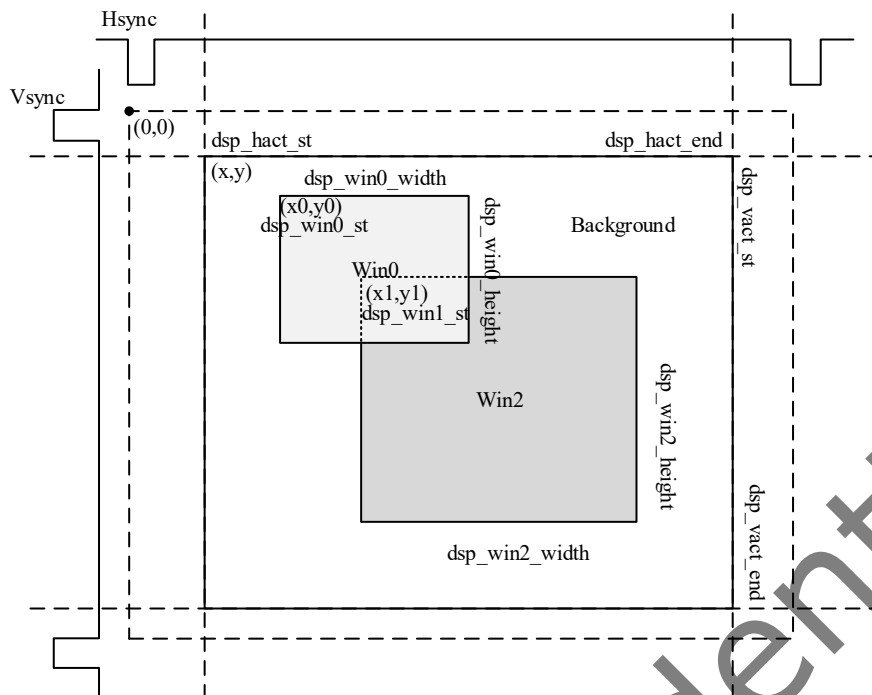


Fig.4-7 VOP Overlay Display

## 2. Transparency color key

There are specific registers (VOP\_WIN0\_COLOR\_KEY and VOP\_WIN2\_COLOR\_KEY) for Win0 and Win2 layer and to configure the color key value. The two transparency color key can be active at the same time.

The pixel color value is compared to the transparency color key before final display. The transparency color key value defines the pixel data considered as the transparent pixel. The pixel values with the source color key value are pixels not visible on the screen, and the under layer pixel values or solid background color are visible.

Transparency color key is done after the scaling module. So transparency color key can only be used in non-scaling mode.

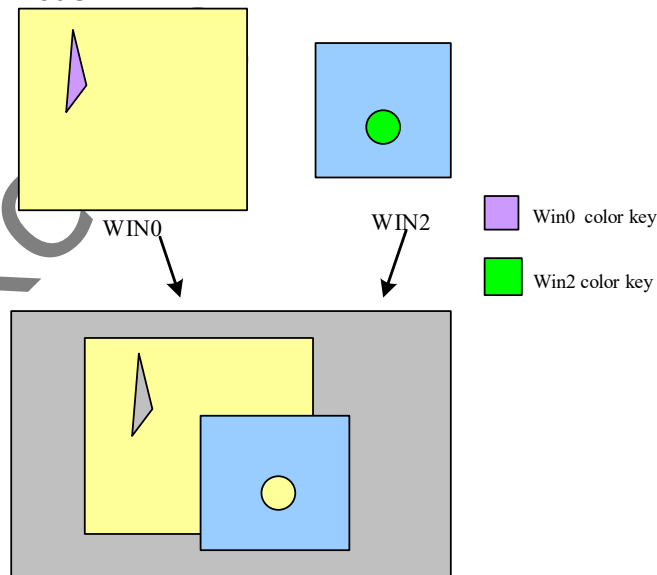


Fig.4-8 VOP Transparency Color Key

## 3. Alpha Blending

Two blending modes are supported. One is per-pixel (ARGB) mode; the other is user-specified mode. In ARGB mode, the alpha value is in the ARGB data (Win0 and Win2 normal mode only). In user-specified mode, the alpha value comes from the register (WINX\_ALPHA\_CTRL[11: 4]).

Pre-multiplied alpha is supported for per-pixel alpha in Win0 and Win2, for Pre-multiplied alpha, the SRC data has already been multiplied with alpha value.



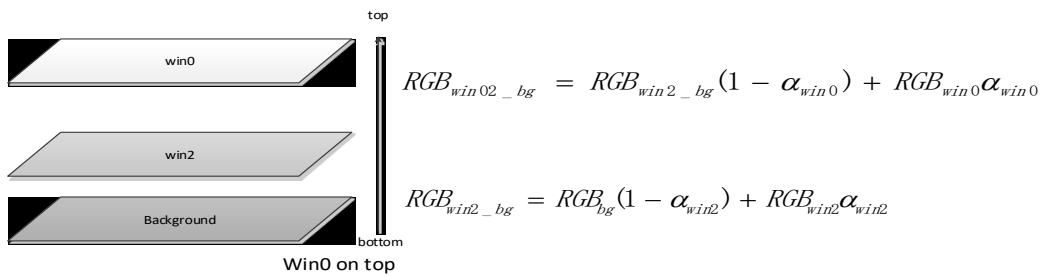


Fig.4-9 VOP Alpha blending

#### 4. RGB OVERLAY and YCbCr OVERLAY

VOP has a signal named `sw_overlay_mode` at `DSP_CTRL2[4]` to decide overlay in RGB or YUV color space.

##### RGB OVERLAY

All layers overlay in RGB color space. If win0 is YUV420/422/444, it can be converted to RGB888 by YUV2RGB use MPEG, JPEG and HDTV formula.

##### YCbCr OVERLAY

All layers overlay in YCbCr color space. When win0/1 input picture format is RGB, it can be converted to YUV444 using BT601 or BT709.

#### 4.3.6 BCSH

The BCSH block is used for brightness, contrast, saturation and hue adjustment to YCbCr format image.

The following diagram shows the BCSH adjustment processing. All the factors should be set in the VOP registers.

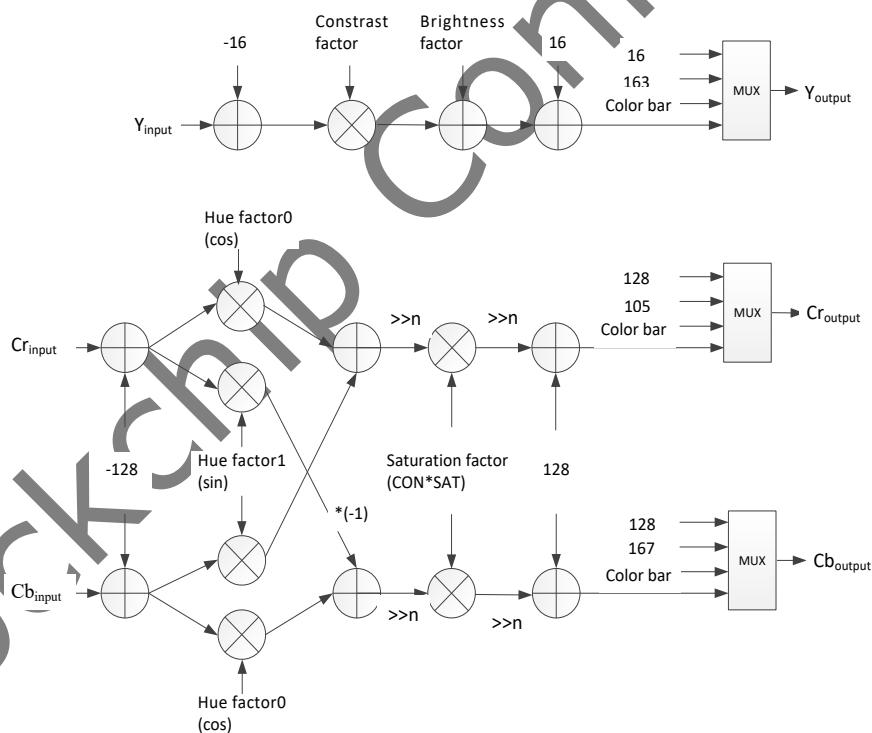


Fig.4-10 VOP BCSH Diagram

#### 4.3.7 Gamma Correction

Gamma correction is necessary because most monitors don't have a linear relationship between the voltage and the brightness, which results in your scene looking like it has too much contrast and the light falling off from the source outward, happens too quickly. The result can also be problematic if you are going into a composition program.

You can correct this by "Gamma Correction", which allows you to display the images and textures on your computer in an accurate manner.

Your screen is not linear, in that it displays the brightness unevenly. As a result, the image looks to be more high contrast than it should, you end up adding more lights or turning up

the intensity, or you don't use the lighting in a realistic way that matches well with live action scenes. It also creates problems for you if you use compositing software. It consumes 256x8bit LUT for each channel. You can write gamma correction LUT through register" DSP\_LUT\_ADDR" one by one after set dsp\_lut\_en = 0.

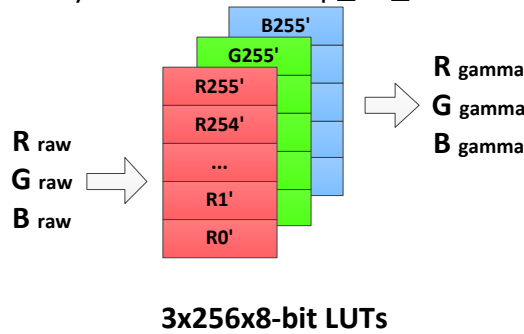


Fig.4-11 VOP Gamma LUTs

### 4.3.8 Replication and dither down

#### 1 Replication (dither up)

If the interface data bus is wider than the pixel format size, by programming the pixel components replication active/inactive, the MSB is replicated to the LSB of the interface data bus or the LSB is filled with 0s.

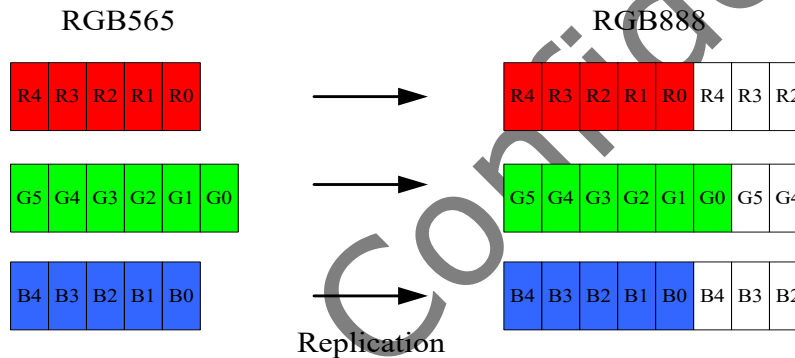


Fig.4-12 VOP Replication

Dithering is used to improve the quality of display the pixel data in a lower color depth on the LCD panel. The Dithering algorithm is based on the (x, y) pixel position, the value of removed bits and frame counter.

#### 2 Dither down

Here we support three kinds of dithering arithmetic. RGB888 to RGB666 has two ways, one is allegro, the other is FRC. RGB888 to RGB565 has only one arithmetic, which is allegro. When Dithering is not enabled, the MSBs of the pixel color components are output on the interface data bus if the interface data bus is smaller than the pixel format size.

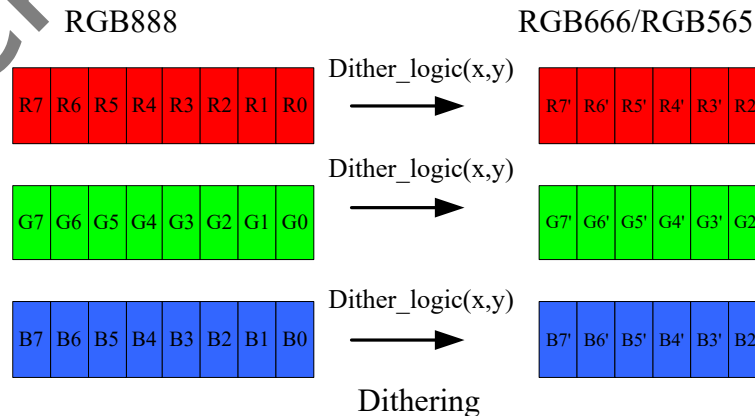


Fig.4-13 VOP dithering

The following figure is the recommended pattern picture in VOP, you can configure different value of register 0x170~0x184, to change the pattern picture(default value is recommended values below).

## 4.4 Register Description

### 4.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 4.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP LITE REG CFG DONE	0x0000	W	0x00000000	Register configure done flag
VOP LITE VERSION	0x0004	W	0x020B6441	Version for VOP
VOP LITE DSP BG	0x0008	W	0x00000000	Display control register
VOP LITE MCU	0x000C	W	0x00711C08	MCU control register
VOP LITE SYS CTRL0	0x0010	W	0x00000000	System control register
VOP LITE SYS CTRL1	0x0014	W	0x00000000	System control register
VOP LITE SYS CTRL2	0x0018	W	0x00006000	System control register
VOP LITE POST LB CTRL	0x001C	W	0x00000000	Post LB control register
VOP LITE DSP CTRL0	0x0020	W	0x01010001	Display register
VOP LITE DSP CTRL1	0x0024	W	0x00000000	Display register
VOP LITE DSP CTRL2	0x0028	W	0x09004000	Display register
VOP LITE VOP STATUS	0x002C	W	0x00000013	Some VOP module status
VOP LITE LINE FLAG	0x0030	W	0x00000000	Line flag configure register
VOP LITE INTR EN	0x0034	W	0x00000000	Interrupt enable register
VOP LITE INTR CLEAR	0x0038	W	0x00000000	Interrupt clear register
VOP LITE INTR STATUS	0x003C	W	0x301D0000	Interrupt raw status and interrupt status
VOP LITE WIN0 CTRL0	0x0050	W	0x00000000	Win0 ctrl register
VOP LITE WIN0 CTRL1	0x0054	W	0x00021220	Win0 ctrl register
VOP LITE WIN0 COLOR KEY	0x0058	W	0x00000000	Win0 color key register
VOP LITE WIN0 VIR	0x005C	W	0x01400140	Win0 virtual stride
VOP LITE WIN0 YRGB MSTR0	0x0060	W	0x00000000	Win0 YRGB memory start address 0
VOP LITE WIN0 CBR MSTR0	0x0064	W	0x00000000	Win0 Cbr memory start address 0
VOP LITE WIN0 ACT INFO	0x0068	W	0x00EF013F	Win0 active window width/height
VOP LITE WIN0 DSP INFO	0x006C	W	0x00EF013F	Win0 display width/height on panel
VOP LITE WIN0 DSP START	0x0070	W	0x000A000A	Win0 display start point on panel
VOP LITE WIN0 SCL FACTOR YRGB	0x0074	W	0x10001000	Win0 YRGB scaling factor
VOP LITE WIN0 SCL FACTOR CBR	0x0078	W	0x10001000	Win0 CBR scaling factor
VOP LITE WIN0 SCL OFFSET	0x007C	W	0x00000000	Win0 scaling start point offset
VOP LITE WIN0 ALPHA CTRL	0x0080	W	0x00000000	Blending control register
VOP LITE DSP HTOTAL HS END	0x0100	W	0x014A000A	Panel scanning horizontal width and hsync pulse end point
VOP LITE DSP HACT START END	0x0104	W	0x000A014A	Panel active horizontal scanning start point and end point
VOP LITE DSP VTOTAL VS END	0x0108	W	0x00FA000A	Panel scanning vertical height and vsync pulse end point

Name	Offset	Size	Reset Value	Description
VOP_LITE_DSP_VACT_ST_END	0x010C	W	0x000A00FA	Panel active vertical scanning start point and end point
VOP_LITE_DSP_VS_ST_END_F1	0x0110	W	0x00000000	Vertical scanning start point and vsync pulse end point of even file
VOP_LITE_DSP_VACT_ST_END_F1	0x0114	W	0x00000000	Vertical scanning active start point and end point of even filed in interlace
VOP_LITE_BCSH_CTRL	0x0160	W	0x00000000	Brightness/Contrast enhancement/Saturation/Hue contrl
VOP_LITE_BCSH_COL_BAR	0x0164	W	0x00000000	Video mode equals 2, then output color bar yuv 24bits value
VOP_LITE_BCSH_BCS	0x0168	W	0x00000000	Brightness/Contrast enhancement/Saturation
VOP_LITE_BCSH_H	0x016C	W	0x00000000	Hue
VOP_LITE_FRC_LOWER01_0	0x0170	W	0x12844821	Frc algorithm configuration register
VOP_LITE_FRC_LOWER01_1	0x0174	W	0x21488412	Frc algorithm configuration register
VOP_LITE_FRC_LOWER10_0	0x0178	W	0xA55A9696	Frc algorithm configuration register
VOP_LITE_FRC_LOWER10_1	0x017C	W	0x5AA56969	Frc algorithm configuration register
VOP_LITE_FRC_LOWER11_0	0x0180	W	0xDEB77BED	Frc algorithm configuration register
VOP_LITE_FRC_LOWER11_1	0x0184	W	0xED7BB7DE	Frc algorithm configuration register
VOP_LITE_MCU_RW_BYPASS_PORT	0x018C	W	0x00000000	MCU panel write data
VOP_LITE_WIN2_CTRL0	0x0190	W	0x00000000	Win2 ctrl register
VOP_LITE_WIN2_CTRL1	0x0194	W	0x00000800	Win2 ctrl register
VOP_LITE_WIN2_VIR0_1	0x0198	W	0x00000000	Win2 virtual stride0 and virtual stride1
VOP_LITE_WIN2_VIR2_3	0x019C	W	0x00000000	Win2 virtual stride2 and virtual stride3
VOP_LITE_WIN2_MST0	0x01A0	W	0x00000000	Win2 memory start address0
VOP_LITE_WIN2_DSP_IN_F00	0x01A4	W	0x00000000	Win2 display width0/height0 on panel
VOP_LITE_WIN2_DSP_ST_0	0x01A8	W	0x00000000	Win2 display start point0 on panel
VOP_LITE_WIN2_COLOR_KEY	0x01AC	W	0x00000000	Win2 color key register
VOP_LITE_WIN2_MST1	0x01B0	W	0x00000000	Win2 memory start address1
VOP_LITE_WIN2_DSP_IN_F01	0x01B4	W	0x00000000	Win2 display width1/height1 on panel
VOP_LITE_WIN2_DSP_ST_1	0x01B8	W	0x00000000	Win2 display start point1 on panel
VOP_LITE_WIN2_ALPHA_CTRL	0x01BC	W	0x00000000	Win2 alpha source control register
VOP_LITE_WIN2_MST2	0x01C0	W	0x00000000	Win2 memory start address2
VOP_LITE_WIN2_DSP_IN_F02	0x01C4	W	0x00000000	Win2 display width2/height2 on panel

Name	Offset	Size	Reset Value	Description
VOP LITE WIN2 DSP ST2	0x01C8	W	0x000A000A	Win2 display start point2 on panel
VOP LITE WIN2 MST3	0x01D0	W	0x00000000	Win2 memory start address3
VOP LITE WIN2 DSP IN FO3	0x01D4	W	0x00000000	Win2 display width3/height3 on panel
VOP LITE WIN2 DSP ST3	0x01D8	W	0x000A000A	Win2 display start point3 on panel
VOP LITE SCAN LINE NUM	0x01F0	W	0x000000B1	The current scan line number
VOP LITE BLANKING VALUE	0x01F4	W	0x01000000	The value of vsync blanking
VOP LITE FLAG REG FRM VALID	0x01F8	W	0x00000000	Flag register value after frame valid
VOP LITE FLAG REG	0x01FC	W	0x00000000	Flag register value before frame valid
VOP LITE GAMMA LUT A DDR	0x0A00	W	0x00F7A3E3	Note: SIZE: 24X256 used for panel GAMMA adjustment, base address: 0x0a00 -- 0x0dff
VOP LITE MMU DTE ADDR	0x0F00	W	0x00000000	MMU current page Table address
VOP LITE MMU STATUS	0x0F04	W	0x00000018	MMU status register
VOP LITE MMU COMMAND	0x0F08	W	0x00000000	MMU command register
VOP LITE MMU PAGE FAULT ADDR	0x0F0C	W	0x00000000	MMU logical address of last page fault
VOP LITE MMU ZAP ONE LINE	0x0F10	W	0x00000000	MMU Zap cache line register
VOP LITE MMU INT RAWSTAT	0x0F14	W	0x00000000	MMU raw interrupt status register
VOP LITE MMU INT CLEAR	0x0F18	W	0x00000000	MMU raw interrupt status register
VOP LITE MMU INT MASK	0x0F1C	W	0x00000000	MMU raw interrupt status register
VOP LITE MMU INT STATUS	0x0F20	W	0x00000000	MMU raw interrupt status register
VOP LITE MMU AUTO GATING	0x0F24	W	0x00000003	MMU auto gating
VOP LITE MMU CFG DONE	0x0F28	W	0x00000000	MMU configure done register

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

#### 4.4.3 Detail Register Description

##### VOP LITE REG CFG DONE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	reg_load_sys_en In the first setting of the register, the new value was saved into the mirror register. 1'b0: Disable 1'b1: Enable When all the system register configure finish(all register except win0 win2), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_win2_en In the first setting of the register, the new value was saved into the mirror register. 1'b0: Disable 1'b1: Enable When all the iep register configure finish(only 2 signals direct_path_en,direct_path_layer_sel), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3:2	RO	0x0	reserved
1	RW	0x0	reg_load_win0_en In the first setting of the register, the new value was saved into the mirror register. 1'b0: Disable 1'b1: Enable When all the win0 register configure finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	WO	0x0	reg_load_global_en In the first setting of the register, the new value was saved into the mirror register. 1'b0: Disable 1'b1: Enable When all the register configure finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

**VOP LITE VERSION**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x02	major Used for IP structure
23:16	RO	0x0b	minor Big feature change under same structure
15:0	RO	0x6441	build RTL current svn number

**VOP LITE DSP BG**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	dsp_bg_red Background Red color
15:8	RW	0x00	dsp_bg_green Background Green color

Bit	Attr	Reset Value	Description
7:0	RW	0x00	dsp_bg_blue Background Blue color

**VOP\_LITE MCU**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output select
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0: Command 1'b1: Data
28	RW	0x0	mcu_frame_st Write "1": MCU HOLD Mode Frame Start Read: MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RW	0x0	mcu_clk_sel 1'b1: MCU BYPASS sync with DCLK 1'b0: MCU BYPASS sync with HCLK
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

**VOP\_LITE SYS\_CTRL0**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved

**VOP\_LITE SYS\_CTRL1**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	sw_axi_max_outstand_num AXI max outstanding number
15:13	RO	0x0	reserved
12	RW	0x0	sw_axi_max_outstand_en AXI max outstand enable 1'b0: Disable 1'b1: Enable
11:8	RW	0x0	sw_noc_hurry_threshold NoC hurry threshold
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	sw_noc_hurry_value NoC hurry value
4	RW	0x0	sw_noc_hurry_en Hurry enable for NoC 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2:1	RW	0x0	sw_noc_qos_value NoC QoS value
0	RW	0x0	sw_noc_qos_en QoS enable for NoC 1'b0: Disable 1'b1: Enable

**VOP LITE SYS CTRL2**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	dcf_idle_en DCF means display timing hold mode. It will hold display timing signals for changing frequency. 1'b0: DCF idle disable 1'b1: DCF idle enable
14	RW	0x1	fs_addr_mask_en 1'b0: Disable 1'b1: Enable
13	RW	0x1	imd_global_regdone_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	imd_dsp_timing_imd 1'b0: Timing reg valid immediately 1'b1: Timing reg valid after frame start
11	RW	0x0	imd_edpi_frm_st Set wms_fs value for MIPI by this register.
10	RW	0x0	imd_edpi_ctrl_mode wms is a signal for MIPI controller. It works like frame start. 1'b0: wms is enable by te and wms_fs 1'b1: wms is enable by te only
9	RW	0x0	imd_edpi_te_en TE is a signal for MIPI controller. It works like frame start. 1'b0: Disable TE 1'b1: Enable TE
8	RO	0x0	reserved
7	RW	0x0	sw_io_pad_clk_sel 1'b0: Normal dclk out 1'b1: Gating dclk out
6	RW	0x0	imd_dsp_data_out_mode 1'b0: Normal output mode 1'b1: Output 24'b0
5	RO	0x0	reserved
4	RW	0x0	imd_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB Y clip: 16~235, CbCr clip: 16~239



Bit	Attr	Reset Value	Description
3	RW	0x0	imd_dsp_out_zero 1'b0: Normal output 1'b1: Output '0' means:hsync,vsync,den=1'b0,1'b0,1'b0
2	RW	0x0	imd_vop_dma_stop 1'b0: Disable 1'b1: Enable If DMA is working, the stop mode would not be active until current bus transfer is finished.
1	RW	0x0	imd_vop_standby_en Writing "1" to turn VOP into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the VOP go back to work immediately. 1'b0: Disable 1'b1: Enable Black display is recommended before setting standby mode enable.
0	RW	0x0	imd_auto_gating_en Auto gating enable 1'b0: Disable 1'b1: Enable

**VOP LITE POST LB CTRL**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	post_lb_almost_empty_threshold Post lb almost empty threshold
3:0	RW	0x0	post_lb_almost_full_threshold Post lb almost full threshold

**VOP LITE DSP CTRL0**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_bt1120_en 1'b0: RGB output 1'b1: BT1120 output
30	RW	0x0	sw_bt1120_yc_swap 1'b0: y/c no swap 1'b1: y/c swap
29	RO	0x0	reserved
28	RW	0x0	mipi_den_pol 1'b0: Positive 1'b1: Negative When this channel dclk_en = 0, this signal is used to control corresponding bit.
27	RW	0x0	mipi_vsync_pol 1'b0: Negative 1'b1: Positive When this channel dclk_en = 0, this signal is used to control corresponding bit

Bit	Attr	Reset Value	Description
26	RW	0x0	mipi_hsync_pol 1'b0: Negative 1'b1: Positive When this channel dclk_en = 0, this signal is used to control corresponding bit.
25	RO	0x0	reserved
24	RW	0x1	mipi_dclk_en 1'b0: MIPI dclk disable 1'b1: MIPI dclk enable
23:17	RO	0x00	reserved
16	RO	0x1	reserved
15:5	RO	0x000	reserved
4	RW	0x0	rgb_den_pol 1'b0: Positive 1'b1: Negative When this channel dclk_en = 0, this signal is used to control corresponding bit.
3	RW	0x0	rgb_vsync_pol 1'b0: Negative 1'b1: Positive When this channel dclk_en = 0, this signal is used to control corresponding bit.
2	RW	0x0	rgb_hsync_pol 1'b0: Negative 1'b1: Positive When this channel dclk_en = 0, this signal is used to control corresponding bit.
1	RO	0x0	reserved
0	RW	0x1	rgb_dclk_en 1'b0: RGB dclk disable 1'b1: RGB dclk enable

**VOP LITE DSP CTRL1**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved

**VOP LITE DSP CTRL2**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RO	0x2	reserved
25:24	RW	0x1	dsp_layer2_sel Layer2 select 2'b00: Select WIN0 2'b10: Select WIN2
23:22	RW	0x0	dsp_layer1_sel Layer1 select 2'b00: Select WIN0 2'b10: Select WIN2
21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	post_lb_mode 1'b0: 1920x3 1'b1: 1280x4
19:16	RW	0x0	dsp_out_mode 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] 4'b0100: Serial 2x12-bit 12'b0,G[3:0],B[7:0] + 12'b0,R[7:0],G[7:4] 4'b1000: Serial 3x8-bit RGB888 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] 4'b1100: Serial 3x8-bit RGB888 + dummy 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] + dummy Others: Reserved
15	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black (0x000000) 1'b0: Disable 1'b1: Enable
14	RW	0x1	dsp_blank_en When this bit enable, the hsync/vsync/den output is blank. means:hsync,vsync,den=1'b1,1'b1,1'b0 1'b0: Disable 1'b1: Enable
13	RO	0x0	reserved
12	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
11	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
10	RO	0x0	reserved
9	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
8	RW	0x0	dither_down 1'b0: Disable 1'b1: Enable
7	RW	0x0	dither_down_sel 1'b0: Allegro 1'b1: FRC
6	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
5	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.
4	RW	0x0	sw_overlay_mode 1'b0: Overlay in RGB domain 1'b1: Overlay in YUV domain

Bit	Attr	Reset Value	Description
3	RO	0x0	reserved
2	RW	0x0	dither_up 1'b0: Disable 1'b1: Enable
1	RW	0x0	interlace_field_pol 1'b0: Normal 1'b1: Invert
0	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable This mode is related to the TVE output, the display timing of odd field must be set correctly. (vop_dsp_vs_st_end_f1/vop_dsp_vact_end_f1)

**VOP LITE VOP STATUS**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	intr_post_lb_almost_empty_mux 1'b0: Interrupt0 1'b1: Interrupt1
12	RW	0x0	intr_post_lb_almost_full_mux 1'b0: Interrupt0 1'b1: Interrupt1
11	RO	0x0	reserved
10	RW	0x0	intr_line_flag1_mux 1'b0: Interrupt0 1'b1: Interrupt1
9	RW	0x0	intr_line_flag0_mux 1'b0: Interrupt0 1'b1: Interrupt1
8	RW	0x0	intr_dma_finish_mux 1'b0: Interrupt0 1'b1: Interrupt1
7:5	RO	0x0	reserved
4	RO	0x1	dma_stop_valid VOP DMA stop status
3	RO	0x0	reserved
2	RO	0x0	int_raw_dma_finish DMA finish raw signal 1'b1: Finish 1'b0: Not finish
1	RO	0x1	idle_mmu MMU idle status 1'b1: Idle 1'b0: Busy
0	RO	0x1	dsp_blanking_en_async 1'b1: Blanking enable 1'b0: Blanking disable

**VOP LITE LINE FLAG**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x000	dsp_line_flag1_num The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_line_flag0_num The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

**VOP LITE INTR EN**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15	RW	0x0	mmu_irq_intr_en 1'b0: Disable 1'b1: Enable
14	RO	0x0	reserved
13	RW	0x0	post_lb_almost_empty_intr_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	post_lb_almost_full_intr_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	post_empty_intr_en 1'b0: Disable 1'b1: Enable
10	RW	0x0	win2_empty_intr_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	dma_frm_fsh_intr_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	dsp_hold_valid_intr_en 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	RW	0x0	win0_empty_intr_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	bus_error_intr_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	line_flag1_intr_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	line_flag0_intr_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	addr_same_intr_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	fs1_intr_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	fs0_intr_en 1'b0: Disable 1'b1: Enable

**VOP LITE INTR CLEAR**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	mmu_irq_intr_clr 1'b0: Not clear 1'b1: Clear
14	RO	0x0	reserved
13	RW	0x0	post_lb_almost_empty_intr_clr 1'b0: Not clear 1'b1: Clear
12	RW	0x0	post_lb_almost_full_intr_clr 1'b0: Not clear 1'b1: Clear
11	RW	0x0	post_empty_intr_clr 1'b0: Not clear 1'b1: Clear
10	RW	0x0	win2_empty_intr_clr 1'b0: Not clear 1'b1: Clear
9	RW	0x0	dma_frm_fsh_intr_clr 1'b0: Not clear 1'b1: Clear
8	W1 C	0x0	dsp_hold_valid_intr_clr 1'b0: Not clear 1'b1: Clear
7	RO	0x0	reserved
6	W1 C	0x0	win0_empty_intr_clr 1'b0: Not clear 1'b1: Clear
5	W1 C	0x0	bus_error_intr_clr 1'b0: Not clear 1'b1: Clear
4	W1 C	0x0	line_flag1_intr_clr 1'b0: Not clear 1'b1: Clear
3	W1 C	0x0	line_flag0_intr_clr 1'b0: Not clear 1'b1: Clear
2	W1 C	0x0	addr_same_intr_clr 1'b0: Not clear 1'b1: Clear
1	W1 C	0x0	fs1_intr_clr 1'b0: Not clear 1'b1: Clear
0	W1 C	0x0	fs0_intr_clr 1'b0: Not clear 1'b1: Clear

**VOP LITE INTR STATUS**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_intr_raw_status MMU interrupt raw status
30	RO	0x0	reserved
29	RW	0x1	post_lb_almost_empty_intr_raw_sts Post lb almost empty interrupt raw status
28	RW	0x1	post_lb_almost_full_intr_raw Post lb almost full interrupt raw status
27	RW	0x0	post_empty_intr_raw Post lb empty interrupt raw status
26	RW	0x0	win2_empty_intr_raw_sts Win2 empty interrupt raw status
25	RO	0x0	dma_frm_fsh_intr_raw_sts DMA finish interrupt raw status
24	RO	0x0	dsp_hold_valid_intr_raw_sts Display hold interrupt raw status
23	RO	0x0	reserved
22	RO	0x0	win0_empty_intr_raw_sts Win0 empty interrupt raw status
21	RO	0x0	bus_error_intr_raw_sts Bus error interrupt raw status
20	RO	0x1	line_flag1_intr_raw_sts Line flag1 interrupt raw status
19	RO	0x1	line_flag0_intr_raw_sts Line flag0 interrupt raw status
18	RW	0x1	addr_same_intr_raw_sts Same address interrupt raw status
17	RO	0x0	fs1_intr_raw_sts New frame start interrupt raw status
16	RO	0x1	fs0_intr_raw_sts Frame start interrupt raw status
15	RO	0x0	mmu_intr_status MMU interrupt status
14	RO	0x0	reserved
13	RW	0x0	post_lb_almost_empty_intr_sts Post lb almost empty interrupt status
12	RW	0x0	post_lb_almost_full_intr Post lb almost full interrupt status
11	RW	0x0	post_empty_intr_sts Post lb empty interrupt status
10	RW	0x0	win2_empty_intr_sts Win2 empty interrupt status
9	RW	0x0	dma_frm_fsh_intr_sts DMA finish interrupt status
8	RO	0x0	dsp_hold_valid_intr_sts Display hold interrupt status
7	RO	0x0	reserved
6	RO	0x0	win0_empty_intr_sts Win0 empty interrupt status
5	RO	0x0	bus_error_intr_sts Bus error interrupt status
4	RO	0x0	line_flag1_intr_sts Line flag1 interrupt status is 1'b1 when line number matches dsp_line_flag0_num in register LINE_FLAG[27:16] if this interrupt is enabled.

Bit	Attr	Reset Value	Description
3	RO	0x0	line_flag0_intr_sts Line flag0 interrupt status is 1'b1 when line number matches dsp_line_flag0_num in register LINE_FLAG[11:0] if this interrupt is enabled.
2	RW	0x0	addr_same_intr_sts Same address interrupt status is 1'b1 when win0_mst and win2_mst are same if this interrupt is enabled.
1	RW	0x0	fs1_intr_sts New frame start interrupt status
0	RO	0x0	fs0_intr_sts Frame start interrupt status

**VOP LITE WIN0 CTRL0**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	win0_cbr_deflick 1'b0: Disable 1'b1: Enable
18	RW	0x0	win0_yrgb_deflick 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	win0_uv_swap 1'b0: CrCb 1'b1: CbCr
14	RW	0x0	win0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
13	RW	0x0	win0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	win0_rb_swap 1'b0: RGB 1'b1: BGR
11:10	RW	0x0	win0_csc_mode Color space conversion: 2'b00/11: BT601 limit range 2'b01: BT601 full range 2'b10: BT709 Reused by win0 r2y color space conversion: 2'bX0: BT601 2'bX1: BT709
9	RW	0x0	win0_no_outstanding 1'b0: Enable 1'b1: Disable
8	RW	0x0	win0_interlace_read 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved



Bit	Attr	Reset Value	Description
3:1	RW	0x0	win0_data_fmt 3'b000: ARGB888 3'b001: RGB888 3'b010: RGB565 3'b100: YCbCr420 3'b101: YCbCr422 3'b110: YCbCr444 Others: reserved
0	RW	0x0	win0_en 1'b0: Win0 layer disable 1'b1: Win0 layer enable

**VOP LITE WIN0 CTRL1**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x2	sw_win0_cbr0_rid Win0 cbr AXI read id
15:12	RW	0x1	sw_win0_yrgb0_rid Win0 yrgb AXI read id
11:8	RW	0x2	win0_cbr_axi_gather_num AXI gather number for win0_cbr
7:4	RW	0x2	win0_yrgb_axi_gather_num AXI gather number for win0_yrgb
3:2	RW	0x0	win0_dma_burst_length 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode)
1	RW	0x0	win0_cbr_axi_gather_en 1'b0: Disable 1'b1: Enable
0	WO	0x0	win0_yrgb_axi_gather_en 1'b0: Disable 1'b1: Enable

**VOP LITE WIN0 COLOR KEY**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	win0_key_en 1'b0: Disable 1'b1: Enable
23:0	RW	0x000000	win0_key_color Win0 color key

**VOP LITE WIN0 VIR**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win0_cbr_vir_stride UV420: ceil(win0_cbr_vir_stride/4) UV422: ceil(win0_cbr_vir_stride/4) UV444: ceil(win0_cbr_vir_stride/2)
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0140	win0_yrgb_vir_stride Number of words of Win0 Virtual width ARGB888: win0_yrgb_vir_stride RGB888: (win0_yrgb_vir_stride*3/4) + win0_yrgb_vir_stride%3 RGB565: ceil(win0_yrgb_vir_stride/2) YUV: ceil(win0_yrgb_vir_stride/4)

**VOP LITE WIN0 YRGB MST0**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb0_mst Win0 yrgb memory start address

**VOP LITE WIN0 CBR MST0**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbr0_mst Win0 cbr memory start address

**VOP LITE WIN0 ACT INFO**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win0_act_height win_act_height = (win0 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win0_act_width win_act_width = (win0 horizontal size -1)

**VOP LITE WIN0 DSP INFO**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x0ef	dsp_win0_height win0_dsp_height = (win0 vertical size -1)
15:11	RO	0x00	reserved
10:0	RW	0x13f	dsp_win0_width win0_dsp_width = (win0 horizontal size -1)

**VOP LITE WIN0 DSP ST**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_win0_yst Win0 y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_win0_xst Win0 x-axis start point

**VOP LITE WIN0 SCL FACTOR YRGB**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_yrgb factor = ((VOP_WIN0_ACT_INFO[31:16]) / (VOP_WIN0_DSP_INFO[31:16])) * 2 <sup>12</sup>
15:0	RW	0x1000	win0_hs_factor_yrgb factor = ((VOP_WIN0_ACT_INFO[15:0]) / (VOP_WIN0_DSP_INFO[15:0])) * 2 <sup>12</sup>

**VOP LITE WIN0\_SCL\_FACTOR\_CBR**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_cbr YCbCr420: factor = ((VOP_WIN0_ACT_INFO[31:16]/2) / (VOP_WIN0_DSP_INFO[31:16])) * 2 <sup>12</sup> YCbCr422,YCbCr444: factor = ((VOP_WIN0_ACT_INFO[31:16]) / (VOP_WIN0_DSP_INFO[31:16])) * 2 <sup>12</sup>
15:0	RW	0x1000	win0_hs_factor_cbr YCbCr422,YCbCr420: factor = ((VOP_WIN0_ACT_INFO[15:0]/2) / (VOP_WIN0_DSP_INFO[15:0])) * 2 <sup>12</sup> YCbCr444: factor = ((VOP_WIN0_ACT_INFO[15:0]) / (VOP_WIN0_DSP_INFO[15:0])) * 2 <sup>12</sup>

**VOP LITE WIN0\_SCL\_OFFSET**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_vs_offset_cbr (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win0_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win0_hs_offset_cbr (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win0_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99

**VOP LITE WIN0\_ALPHA\_CTRL**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:4	RW	0x00	win0_alpha_value Win0 global alpha value
3	RW	0x0	win0_alpha_sat_mode 1'b0: Alpha value no change 1'b1: Alpha = alpha + alpha[7]
2	RW	0x0	win0_alpha_pre_mul 1'b0: Non-premultiplied alpha 1'b1: Premultiplied alpha
1	RW	0x0	win0_alpha_mode 1'b0: Global alpha 1'b1: Per-pixel alpha
0	RW	0x0	win0_alpha_en 1'b0: Disable 1'b1: Enable

**VOP LITE DSP HTOTAL HS END**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x14a	dsp_htotal dsp_htotal
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_hs_end dsp_hs_end

**VOP LITE DSP HACT ST END**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_hact_st dsp_hact_st
15:12	RO	0x0	reserved
11:0	RW	0x14a	dsp_hact_end dsp_hact_end

**VOP LITE DSP VTOTAL VS END**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0fa	dsp_vtotal dsp_vtotal
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_vs_end dsp_vs_end

**VOP LITE DSP VACT ST END**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_vact_st dsp_vact_st
15:12	RO	0x0	reserved
11:0	RW	0x0fa	dsp_vact_end dsp_vact_end

**VOP LITE DSP VS ST END F1**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

**VOP LITE DSP VACT ST END F1**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

**VOP LITE BCSH CTRL**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	sw_bcsch_r2y_en 1'b0: Bypass 1'b1: Enable
6	RW	0x0	sw_bcsch_y2r_en 1'b0: Bypass 1'b1: Enable
5:4	RW	0x0	sw_bcsch_y2r_csc_mode Color space conversion: 2'b00/11: MPEG 2'b01: HD 2'b10: JPEG
3:2	RW	0x0	video_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
1	RW	0x0	sw_bcsch_r2y_csc_mode Color space conversion: 1'b0: BT601 1'b1: BT709
0	RW	0x0	bcsch_en 1'b0: BCSH bypass 1'b1: BCSH enable

**VOP LITE BCSH COL BAR**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	color_bar_v V component of color bar
15:8	RW	0x00	color_bar_u U component of color bar
7:0	RW	0x00	color_bar_y Y component of color bar

**VOP LITE BCSH BCS**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sat_con Saturation*Contrast*256: 0,1.992*1.992

Bit	Attr	Reset Value	Description
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: 0,1.992
7	RO	0x0	reserved
6:0	RW	0x00	brightness Brightness: -128,127

**VOP LITE BCSH H**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue cos_hue
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue sin_hue

**VOP LITE FRC LOWER01 0**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 lower01_frm1
15:0	RW	0x4821	lower01_frm0 lower01_frm0

**VOP LITE FRC LOWER01 1**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 lower01_frm3
15:0	RW	0x8412	lower01_frm2 lower01_frm2

**VOP LITE FRC LOWER10 0**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 lower10_frm1
15:0	RW	0x9696	lower10_frm0 lower10_frm0

**VOP LITE FRC LOWER10 1**

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 lower10_frm3
15:0	RW	0x6969	lower10_frm2 lower10_frm2

**VOP LITE FRC LOWER11 0**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 lower11_frm1

Bit	Attr	Reset Value	Description
15:0	RW	0x7bed	lower11_frm0 lower11_frm0

**VOP LITE FRC LOWER11 1**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 lower11_frm3
15:0	RW	0xb7de	lower11_frm2 lower11_frm2

**VOP LITE MCU RW BYPASS PORT**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mcu_write_data_bypass Write MCU bypass data in this register when MCU works in bypass mode.

**VOP LITE WIN2 CTRL0**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31	RW	0x0	win2_endian_swap3 1'b0: Big-endian 1'b1: Little-endian
30	RW	0x0	win2_alpha_swap3 1'b0: ARGB 1'b1: RGBA
29	RW	0x0	win2_rb_swap3 1'b0: RGB 1'b1: BGR
28	RW	0x0	win2_endian_swap2 1'b0: Big-endian 1'b1: Little-endian
27	RW	0x0	win2_alpha_swap2 1'b0: ARGB 1'b1: RGBA
26	RW	0x0	win2_rb_swap2 1'b0: RGB 1'b1: BGR
25	RW	0x0	win2_endian_swap1 1'b0: Big-endian 1'b1: Little-endian
24	RW	0x0	win2_alpha_swap1 1'b0: ARGB 1'b1: RGBA
23	RW	0x0	win2_rb_swap1 1'b0: RGB 1'b1: BGR
22	RW	0x0	win2_endian_swap0 1'b0: Big-endian 1'b1: Little-endian
21	RW	0x0	win2_alpha_swap0 1'b0: ARGB 1'b1: RGBA

Bit	Attr	Reset Value	Description
20	RW	0x0	win2_rb_swap0 1'b0: RGB 1'b1: BGR
19	RO	0x0	reserved
18:17	RW	0x0	win2_data_fmt3 2'b00: ARGB888 2'b01: RGB888 2'b10: RGB565
16	RW	0x0	win2_mst3_en 1'b0: Disable 1'b1: Enable
15	RO	0x0	reserved
14:13	RW	0x0	win2_data_fmt2 2'b00: ARGB888 2'b01: RGB888 2'b10: RGB565
12	RW	0x0	win2_mst2_en 1'b0: Disable 1'b1: Enable
11	RO	0x0	reserved
10:9	RW	0x0	win2_data_fmt1 2'b00: ARGB888 2'b01: RGB888 2'b10: RGB565
8	RW	0x0	win2_mst1_en 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6:5	RW	0x0	win2_data_fmt0 2'b00: ARGB888 2'b01: RGB888 2'b10: RGB565
4	RW	0x0	win2_mst0_en 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	win2_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	win2_interlace_read 1'b0: Disable 1'b1: Enable
0	RW	0x0	win2_en 1'b0: Disable 1'b1: Enable

**VOP LITE WIN2 CTRL1**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:17	RW	0x00	win2_axi_max_outstanding_num Win2 AXI max outstanding number



Bit	Attr	Reset Value	Description
16	RW	0x0	win2_axi_max_outstanding_en 1'b0: Disable 1'b1: Enable
15	RW	0x0	win2_y_mir_en 1'b0: No y_mirror 1'b1: Y_mirror
14	RW	0x0	win2_no_outstanding 1'b0: Enable 1'b1: Disable
13:12	RO	0x0	reserved
11:8	RW	0x8	win2_rid AXI read id of win2 channel
7:4	RW	0x0	win2_axi_gather_num Win2 axi gather transfer number
3:2	RW	0x0	win2_dma_burst_length 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved
1	RO	0x0	reserved
0	RW	0x0	win2_axi_gather_en 1'b0: Disable 1'b1: Enable

**VOP LITE WIN2 VIR0 1**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win2_vir_stride1 Number of words of Win2 Virtual1 width ARGB888: win2_vir_width1 RGB888: (win2_vir_width1 * 3/4) + (win2_vir_width1 % 3) RGB565: ceil(win2_vir_width1 / 2)
15:0	RW	0x0000	win2_vir_stride0 Number of words of Win2 Virtual0 width ARGB888: win2_vir_width0 RGB888: (win2_vir_width0 * 3/4) + (win2_vir_width0 % 3) RGB565: ceil(win2_vir_width0 / 2)

**VOP LITE WIN2 VIR2 3**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win2_vir_stride3 Number of words of Win2 Virtual3 width ARGB888: win2_vir_width3 RGB888: (win2_vir_width3 * 3/4) + (win2_vir_width3 % 3) RGB565: ceil(win2_vir_width3 / 2)
15:0	RW	0x0000	win2_vir_stride2 Number of words of Win2 Virtual2 width ARGB888: win2_vir_width2 RGB888: (win2_vir_width2 * 3/4) + (win2_vir_width2 % 3) RGB565: ceil(win2_vir_width2 / 2)

**VOP LITE WIN2 MST0**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst0 Must be aligned to 8 byte address

**VOP LITE WIN2 DSP INFO0**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win2_dsp_height0 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x000	win2_dsp_width0 win2_dsp_width = size -1

**VOP LITE WIN2 DSP ST0**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win2_dsp_yst0 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x0000	win2_dsp_xst0 Win2 horizontal start point(x) of the Panel scanning

**VOP LITE WIN2 COLOR KEY**

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	win2_key_en 1'b0: Disable 1'b1: Enable
23:0	RW	0x000000	win2_key_color Win2 key color

**VOP LITE WIN2 MST1**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst1 Must be aligned to 8 byte address

**VOP LITE WIN2 DSP INFO1**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win2_dsp_height1 win2_dsp_height1 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x000	win2_dsp_width1 win2_dsp_width1 = size -1

**VOP LITE WIN2 DSP ST1**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	win2_dsp_yst1 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x0000	win2_dsp_xst1 Win2 horizontal start point(x) of the Panel scanning

**VOP LITE WIN2 ALPHA CTRL**

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:4	RW	0x00	win2_alpha_value Win2 global alpha value
3	RW	0x0	win2_alpha_sat_mode 1'b0: Alpha value no change 1'b1: Alpha=Alpha + Alpha[7]
2	RW	0x0	win2_alpha_pre_mul 1'b0: Non-premultiplied alpha 1'b1: Premultiplied alpha
1	RW	0x0	win2_alpha_mode 1'b0: Global alpha 1'b1: Per-pixel alpha
0	RW	0x0	win2_alpha_en 1'b0: Disable 1'b1: Enable

**VOP LITE WIN2 MST2**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst2 Must be aligned to 8byte address

**VOP LITE WIN2 DSP INFO2**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win2_dsp_height2 win2_dsp_height2 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x000	win2_dsp_width2 win2_dsp_width2 = size -1

**VOP LITE WIN2 DSP ST2**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst2 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst2 Win2 horizontal start point(x) of the Panel scanning

**VOP LITE WIN2 MST3**

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst3 Must be aligned to 8byte address

**VOP LITE WIN2 DSP INFO3**

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win2_dsp_height3 win2_dsp_height3 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x000	win2_dsp_width3 win2_dsp_width3 = size -1

**VOP LITE WIN2 DSP ST3**

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst3 Win2 vertical start point(y) of the panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst3 Win2 horizontal start point(x) of the panel scanning

**VOP LITE SCAN LINE NUM**

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x0b1	scan_line_num The current scan line number

**VOP LITE BLANKING VALUE**

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x1	blanking_value_config_en If this bit enable, blank value can be set by sw_blanking_value. 1'b0: Disable 1'b1: Enable
23:0	WO	0x000000	sw_blanking_value Set blank value when VOP is in blank mode. Change default blank value by this register.

**VOP LITE FLAG REG FRM VALID**

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag_reg_frm_valid This register is the value of FLAG_REG(0x1fc).

**VOP LITE FLAG REG**

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	flag_reg The flag register is just for software flow. This does not affect the normal operation of VOP.

**VOP LITE GAMMA LUT ADDR**

Address: Operational Base + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0xf7a3e3	gamma_lut_addr GAMMA LUT address

**VOP LITE MMU DTE ADDR**

Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU DTE address

**VOP LITE MMU STATUS**

Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault
4	RW	0x1	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0 = Read 1'b1 = Write
3	RW	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command
0	RW	0x0	PAGING_ENABLED Paging is enabled 1'b0: Disabled 1'b1: Enabled

**VOP LITE MMU COMMAND**

Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

**VOP LITE MMU PAGE FAULT ADDR**

Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PAGE_FAULT_ADDR Address of last page fault

**VOP LITE MMU ZAP ONE LINE**

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_ZAP_ONE_LINE Address to be invalidated from the page table cache

**VOP LITE MMU INT RAWSTAT**

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

**VOP LITE MMU INT CLEAR**

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

**VOP LITE MMU INT MASK**

Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

**VOP LITE MMU INT STATUS**

Address: Operational Base + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

**VOP LITE MMU AUTO GATING**

Address: Operational Base + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x1	sw_mmu_cfg_mode When it is 1'b0, the MMU reg config will valid after frame start.

Bit	Attr	Reset Value	Description
0	RW	0x1	mmu_auto_gating When it is 1'b1, the MMU will auto gating itself. 1'b0: Disabled auto gating 1'b1: Enabled auto gating

**VOP LITE MMU CFG DONE**

Address: Operational Base + offset (0x0F28)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	reg_load_mmu_en In the first setting of the register, the new value was saved into the mirror register. 1'b0: Disabled 1'b1: Enabled When all the MMU register configure finish, writing this register to enable the copyright of the mirror register to real register.

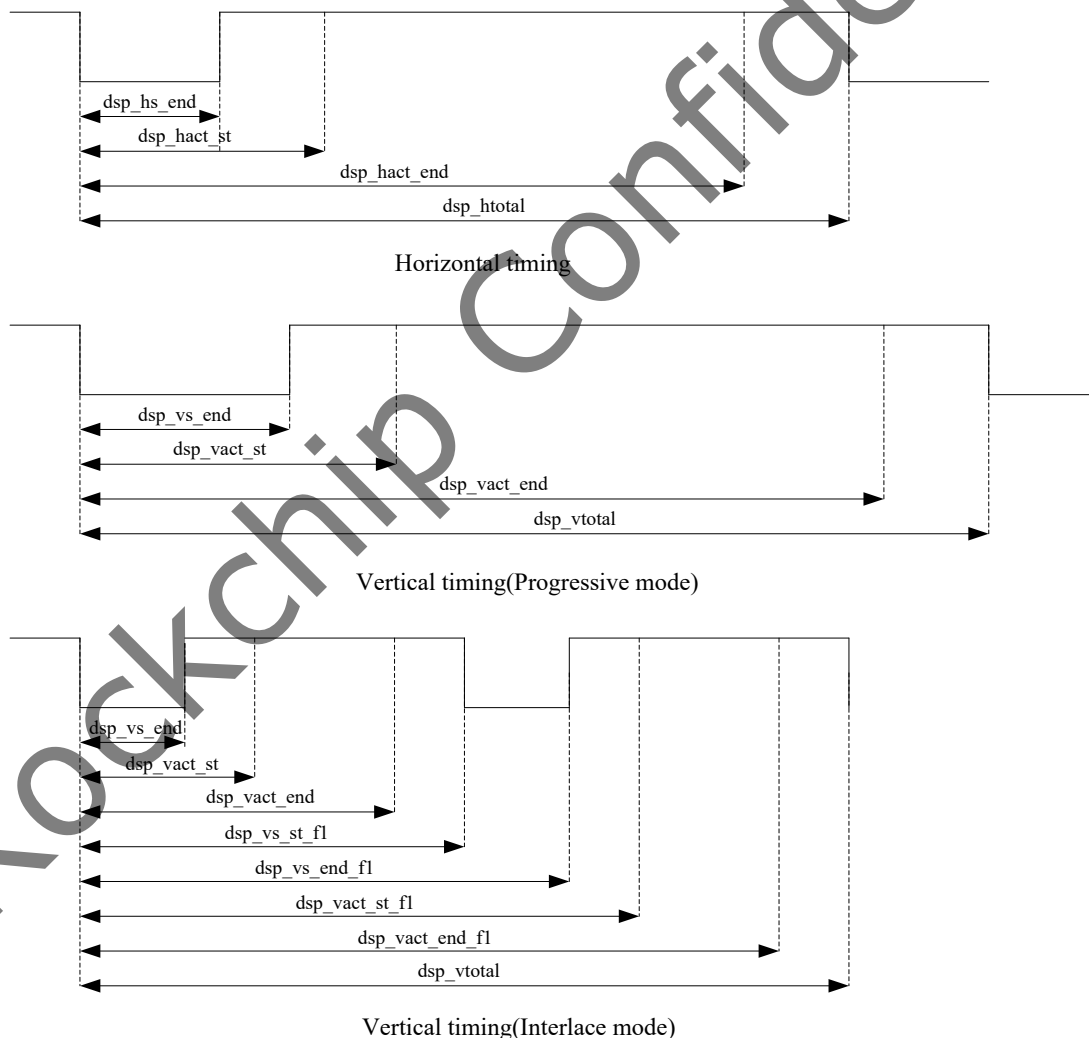
**4.5 Timing Diagram**

Fig.4-14 VOP RGB interface timing setting

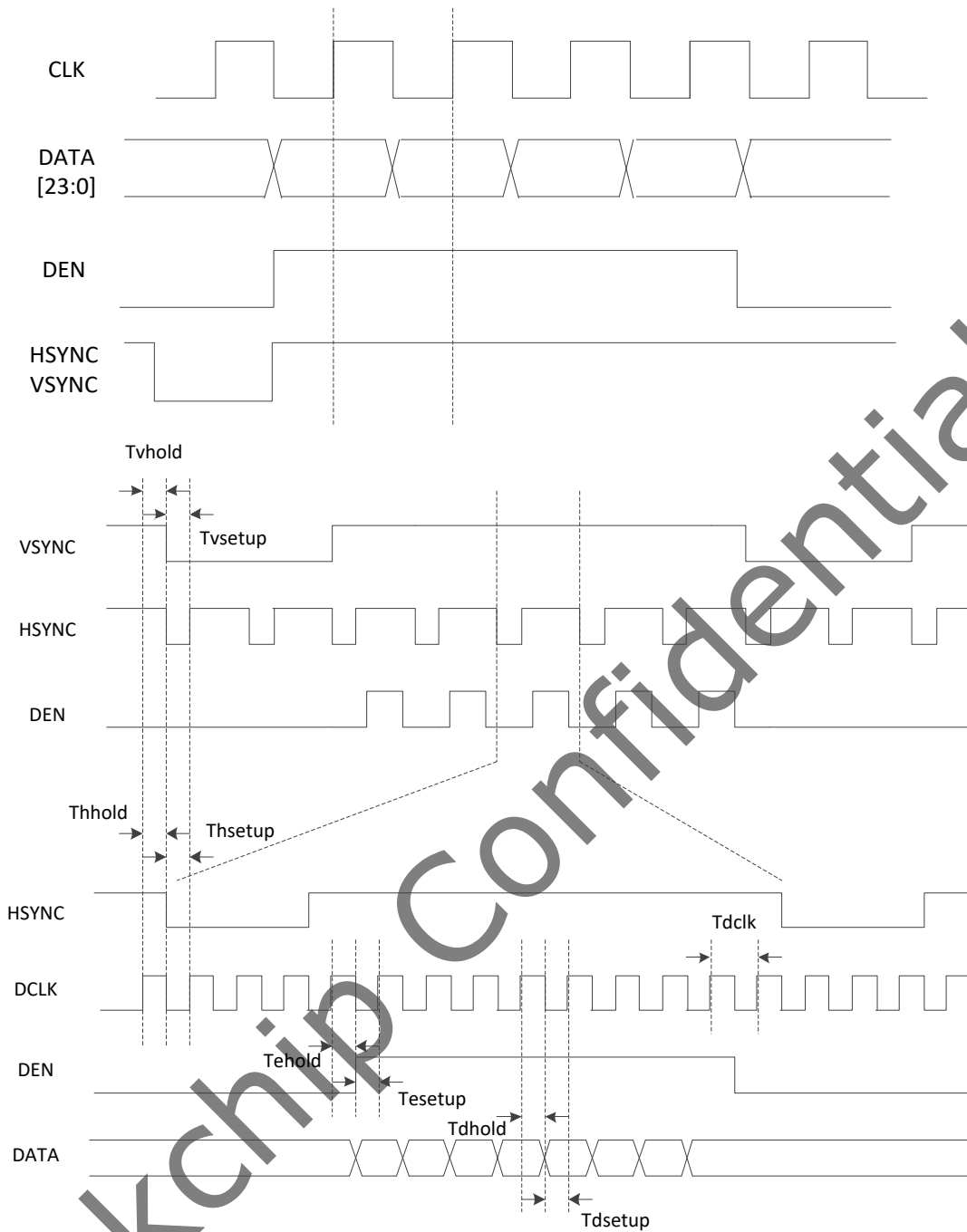


Fig.4-15 VOP RGB interface timing(SDR)

## 4.6 Interface Description

### 4.6.1 VOP Outputs

Table 4-3 VOP Control Pins Definition

Module Pin	Dir	Pin Name	IOMUX Setting
vop_data0	O	LCDC_D0/RGMII_TXD3_M1/CIF_D0_M1/UART4_RTSN_M1/GPIO2_A4_d	GRF_GPIO2A_IOMUX_H[3:0]=0x1
vop_data1	O	LCDC_D1/RGMII_CRS_M1/CIF_D1_M1/UART4_CTSN_M1/I2C5_SCL_M0/GPIO2_A5_d	GRF_GPIO2A_IOMUX_H[7:4]=0x1
vop_data2	O	LCDC_D2/RGMII_COL_M1/CIF_D2_M1/PWM5_M1/UART4_TX_M1/GPIO2_A6_d	GRF_GPIO2A_IOMUX_H[11:8]=0x1
vop_data3	O	LCDC_D3/I2S2_SDO_M1/UART4_RX_M1/PWM4_M1/SPI0_CS0n_	GRF_GPIO2A_IOMUX_H[15:12]=0x1



Module Pin	Dir	Pin Name	IOMUX Setting
		M2/GPIO2_A7_d	
vop_data4	O	LCDC_D4/I2S2_SDI_M1/UART5_TX_M1/PWM3_IR_M1/SPI0_M0SI_M2/GPIO2_B0_d	GRF_GPIO2B_IOMUX_L[3:0]=0x1
vop_data5	O	LCDC_D5/I2S2_SCLK_M1/UART5_RX_M1/PWM2_M1/SPI0_MISO_M2/GPIO2_B1_d	GRF_GPIO2B_IOMUX_L[7:4]=0x1
vop_data6	O	LCDC_D6/I2S2_LRCK_M1/UART5_RTSN_M1/PWM1_M1/SPI0_CLK_M2/GPIO2_B2_d	GRF_GPIO2B_IOMUX_L[11:8]=0x1
vop_data7	O	LCDC_D7/I2S2_MCLK_M1/CIF_D3_M1/UART5_CTSN_M1/SPI0_CS1n_M2/PWM0_M1/I2C5_SDA_M0/GPIO2_B3_d	GRF_GPIO2B_IOMUX_L[15:12]=0x1
vop_data8	O	LCDC_D8/RGMII_RXDV_M1/CIF_D4_M1/GPIO2_B4_d	GRF_GPIO2B_IOMUX_H[3:0]=0x1
vop_data9	O	LCDC_D9/RGMII_RXD0_M1/CIF_D5_M1/GPIO2_B5_d	GRF_GPIO2B_IOMUX_H[7:4]=0x1
vop_data10	O	LCDC_D10/RGMII_RXD1_M1/CIF_D6_M1/GPIO2_B6_d	GRF_GPIO2B_IOMUX_H[11:8]=0x1
vop_data11	O	LCDC_D11/RGMII_CLK_M1/CIF_D7_M1/GPIO2_B7_d	GRF_GPIO2B_IOMUX_H[15:12]=0x1
vop_data12	O	LCDC_D12/RGMII_RXER_M1/CIF_D8_M1/GPIO2_C0_d	GRF_GPIO2C_IOMUX_L[3:0]=0x1
vop_data13	O	LCDC_D13/RGMII_MDIO_M1/CIF_D9_M1/GPIO2_C1_d	GRF_GPIO2C_IOMUX_L[7:4]=0x1
vop_data14	O	LCDC_D14/RGMII_MDC_M1/CIF_D10_M1/GPIO2_C2_d	GRF_GPIO2C_IOMUX_L[11:8]=0x1
vop_data15	O	LCDC_D15/RGMII_TXD0_M1/CIF_D11_M1/GPIO2_C3_d	GRF_GPIO2C_IOMUX_L[15:12]=0x1
vop_data16	O	LCDC_D16/RGMII_TXD1_M1/CIF_D12_M1/GPIO2_C4_d	GRF_GPIO2C_IOMUX_H[3:0]=0x1
vop_data17	O	LCDC_D17/CLK_OUT_ETHERNET_M1/CIF_D13_M1/GPIO2_C5_d	GRF_GPIO2C_IOMUX_H[7:4]=0x1
vop_data18	O	LCDC_D18/RGMII_TXEN_M1/CIF_D14_M1/GPIO2_C6_d	GRF_GPIO2C_IOMUX_H[11:8]=0x1
vop_data19	O	LCDC_D19/RGMII_RXD2_M1/CIF_D15_M1/I2S1_MCLK_M2/GPIO2_C7_d	GRF_GPIO2C_IOMUX_H[15:12]=0x1
vop_data20	O	LCDC_D20/RGMII_RXD3_M1/CIF_VSYNC_M1/I2S1_SDO_M2/GPIO2_D0_d	GRF_GPIO2D_IOMUX_L[3:0]=0x1
vop_data21	O	LCDC_D21/RGMII_TXD2_M1/CIF_CLKOUT_M1/I2S1_SCLK_M2/GPIO2_D1_d	GRF_GPIO2D_IOMUX_L[7:4]=0x1
vop_data22	O	LCDC_D22/RGMII_TXCLK_M1/CIF_CLKIN_M1/I2S1_LRCK_M2/GPIO2_D2_d	GRF_GPIO2D_IOMUX_L[11:8]=0x1
vop_data23	O	LCDC_D23/RGMII_RXCLK_M1/CIF_HSYNC_M1/I2S1_SDI_M2/GPIO2_D3_d	GRF_GPIO2D_IOMUX_L[15:12]=0x1
vop_den	O	LCDC_DEN/PWM6_M1/SPI1_CS0n_M2/I2C3_SCL_M1/GPIO2_D4_d	GRF_GPIO2D_IOMUX_H[3:0]=0x1

Module Pin	Dir	Pin Name	IOMUX Setting
vop_hsync	O	LCDC_HSYNC/PWM10_M1/ SPI1_CLK_M2 /I2C3_SDA_M1/GPIO2_D5_d	GRF_GPIO2D_IOMUX_H[7:4] =0x1
vop_vsync	O	LCDC_VSYNC/UART3_RTSN_M2 /PWM9_M1/SPI1_MOSI_M2/GPI O2_D6_d	GRF_GPIO2D_IOMUX_H[11: 8]=0x1
vop_clk	O	LCDC_CLK/UART3_CTSN_M2/P WM8_M1/SPI1_MISO_M2/GPIO 2_D7_d	GRF_GPIO2D_IOMUX_H[15: 12]=0x1

Notes: I=input, O=output, I/O=input/output, bidirectional

VOP supports RGB, MIPI, BT1120, MCU output. BT1120 and MCU reuse the RGB interface. VOP is suitable for different display mode by different usage, which is shown as follows.

Table 4-4 VOP Display Mode

Display mode	RGB Parallel 24-bit	RGB Parallel 18-bit	RGB Parallel 16-bit
DCLK	DCLK	DCLK	DCLK
VSNC	VSNC	VSNC	VSNC
HSNC	HSNC	HSNC	HSNC
DEN	DEN	DEN	DEN
DATA	DATA[23:0]	DATA[17:0]	DATA[15:0]

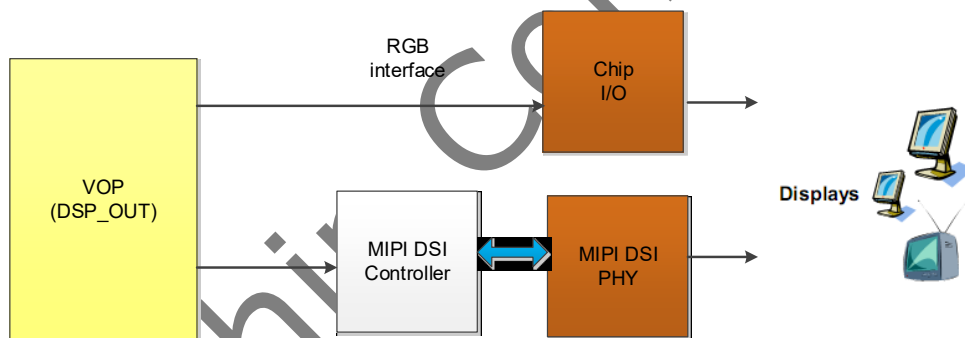


Fig.4-16 VOP Display output for peripherals

## 4.7 Application Notes

### 4.7.1 DMA transfer mode

There are three DMA transfer modes for loading win0 or win2 frame data determined by following parameters(X=0,1):

dma\_burst\_length

winX\_no\_outstanding

winX\_gather\_en

winX\_gather\_thres

### 4.7.2 auto outstanding transfer mode(random transfer)

When winX\_no\_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the empty level of internal memory, dma\_burst\_length, data format and active image width.

### 4.7.3 configured outstanding transfer mode(fixed transfer)

When winX\_gather\_en is 1, fixed-number of bursts transfer command should be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by winX\_gather\_thres. Since the internal memory size is limited, there is some restriction for the winX\_gather\_thres as follows.

Table 4-5 Gather configuration for all format

Gather Threshold	dma_burst_length = 2'b00(burst16)	dma_burst_length = 2'b01(burst8)	dma_burst_length = 2'b10(burst4)
YCbCr420 YCbCr422 YCbCr444	0	0,1,2	0,1,2,3
ARGB888 RGB888 RGB565	0,1,2,3	0,1,2,3	0,1,2,3

### 4.7.4 GAMMA LUT

When dsp\_lut\_en is 0, the DSP LUT data should be refreshed by software. i.e, writing dsp lut data to the internal memory with the start address DSP\_LUT\_MST. The memory size is 256x24, i.e, lower 24bits valid, and the writing data number is determined by software.

### 4.7.5 DMA control (QoS/Hurry/Outstanding)

If you want to get higher priority for VOP to access external memory when the frame data is urgent, a QoS and hurry request can be generated and sent out basing on the configured values:

sw\_noc\_qos\_en: SYS\_CTRL1[0]

sw\_noc\_qos\_value: SYS\_CTRL1[2:1]

sw\_noc\_hurry\_en: SYS\_CTRL1[4]

sw\_noc\_hurry\_value: SYS\_CTRL1[6:5]

sw\_noc\_hurry\_threshold: SYS\_CTRL1[11:8]

sw\_axi\_max\_outstand\_en: SYS\_CTRL1[12]

sw\_axi\_max\_outstand\_num: SYS\_CTRL1[20:16]

QoS request for higher bus priority for win2

NOC hurry for higher bus priority for VIO when win0 needs higher priority.

Max Outstanding number is configurable.

### 4.7.6 Interrupt

VOP interrupt is comprised of 14 interrupt sources:

- frame start0 interrupt
- frame start1 interrupt
- address same interrupt
- line flag0 interrupt
- line flag1 interrupt
- bus error interrupt
- Win0 empty interrupt
- Win2 empty interrupt
- Display hold interrupt
- DMA finish interrupt
- Post empty interrupt
- Post lb almost full interrupt
- Post lb almost empty interrupt
- MMU interrupt

Every interrupt has independent interrupt enable signal(VOP\_INT\_EN), interrupt clear signal(VOP\_INT\_CLR) and interrupt raw status signal (VOP\_INT\_STATUS).

There is only one interrupt combined with all this interrupt signals to CPU, and it high active. DMA finish interrupt is used for changing DDR frequency. This interrupt will be asserted when DMA finish getting all the Pixel DATA every frame. This interrupt is asserted at the end of the frame.

Address same interrupt will be asserted at this kind of scenario that all the memory start address configured in VOP register are same compared with the former frame. This interrupt

is asserted at the beginning of frame start.

The difference between frame start0 interrupt and frame start1 interrupt is that frame start0 interrupt will be asserted every frame, while the frame start1 interrupt will be masked when all the memory start address is same.

#### 4.7.7 RGB display mode

RGB display mode is used for RGB panel display. It is a continuous frames display mode.

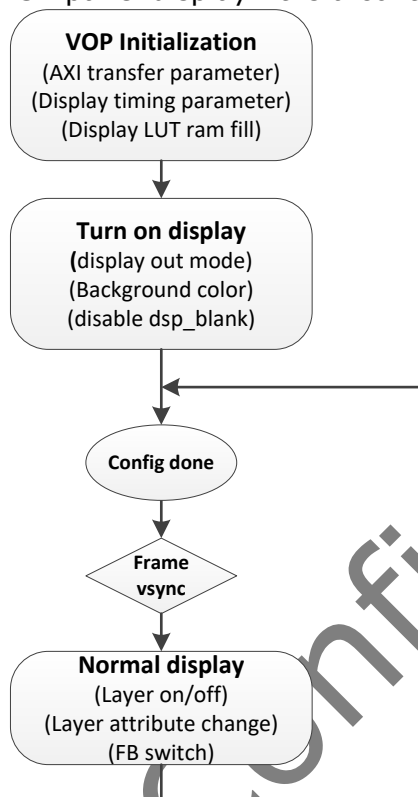


Fig.4-17 VOP RGB Mode Programming Flow

##### 1.VOP initialization

VOP initialization should be done before turning display on.

First, AXI bus parameter (VOP\_SYS\_CTRL1) should be set for DMA transfer.

Second, display panel/interface timing should be set for display output. The registers are:

VOP\_DSP\_HTOTAL\_HS\_END/ VOP\_DSP\_HACT\_ST\_END/ VOP\_DSP\_VTOTAL\_HS\_END/  
VOP\_DSP\_VACT\_ST\_END/ VOP\_DSP\_VS\_ST\_END\_F1/ VOP\_DSP\_VACT\_ST\_END\_F1

##### 2.Background display

Before normal display, the background display could be turn on.

First, set display output mode (VOP\_DSP\_CTRL0/1) according to display device.

Second, disable dsp\_blank mode, which would not be enable until frame synchronization.

Finally, writing '1' to "VOP\_REG\_CFG\_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

##### 3.Normal display

In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.

First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until frame synchronization.

Finally, write 1 to "VOP\_REG\_CFG\_DONE" register then all the frame-sync registers will be enabled at the beginning of next frame.

#### 4.7.8 Immediately control register

There are two type registers in VOP, one is effective immediately, the other is effective by frame sync. Effective immediately registers list as follows, other registers are all effective by frame sync.

Table 4-6 effective immediately register table

register address	description
0x0008	background
0x0018	All display and control signal registers
0x170~0x184	Frc configuration bits

#### 4.7.9 Output Polarity Control

There are two channel outputs (RGB MIPI, some may not support because SOC do not have the related interface), every channel has its own xxx\_dclk\_en, xxx\_hsync\_pol, xxx\_vsync\_pol, xxx\_den\_pol. BT1120 and MCU reuse the RGB interface.

The xxx\_dclk\_en should be set to 1 when output select the xxx channel, and the other channel's xxx\_dclk\_en should be set to 0 to gate the output clk and data.

When using RGB panel, the dclk should be tied to "0" or "1" in some scenarios.

In this case, you should enable sw\_io\_pad\_clk\_sel, to tie dclk to "0".

For RGB and BT1120 interface, set LCDC dclk invert by GRF registers. Configure GRF\_IOFUNC\_SEL3[2] = 0x1.

#### 4.7.10 Some special control

- The blanking value of VSYNC could be configured through register BLANKING\_VALUE.
- The current scan line number could be read through reg\_addr 0x1f0.
- There is a FLAG\_REG which is readable and writable. This FLAG\_REG does not for configuration function. Our software staff may use it in the future. After writing a meaningful 32bit value to FLAG\_REG, we can read it before frame valid through reading 0x1fc value, and can get the same value after frame valid reading 0x1f8 value.

#### 4.7.11 RGB PATH

TTL typical configuration is as follows:

```
Word32(GRF_BASE + GRF_GPIO2A_IOMUX_H) = 0xffff1111;
Word32(GRF_BASE + GRF_GPIO2B_IOMUX_L) = 0xffff1111;
Word32(GRF_BASE + GRF_GPIO2B_IOMUX_H) = 0xffff1111;
Word32(GRF_BASE + GRF_GPIO2C_IOMUX_L) = 0xffff1111;
Word32(GRF_BASE + GRF_GPIO2C_IOMUX_H) = 0xffff1111;
Word32(GRF_BASE + GRF_GPIO2D_IOMUX_L) = 0xffff1111;
Word32(GRF_BASE + GRF_GPIO2D_IOMUX_H) = 0xffff1111;
```

#### 4.7.12 GRF LCDC BYPASS

Set GRF\_IOFUNC\_SEL3[0] = 0x1.

The block diagram of LCDC bypass is as follows:

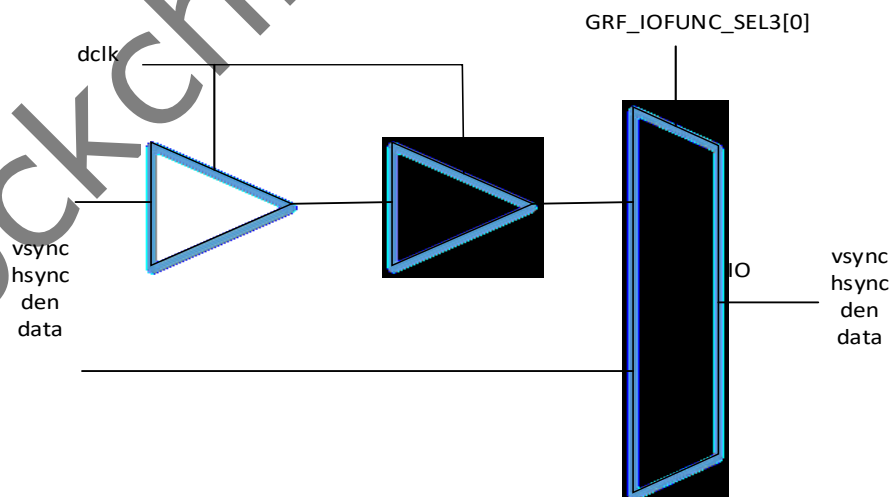


Fig.4-18 LCDC bypass block diagram

#### 4.7.13 MCU INTERFACE PATH

Configure GRF LCDC bypass before using MCU interface.

The MCU interface configuration is as follows:

- No bypass mode
- 1) Set dsp\_out\_mode(0x0028[19:16]) according to interface width.
  - 2) Set mcu\_type, mcu\_bypass and mcu timing value in 0x0004 register.

mcu\_type = 1'b1;

mcu\_bypass = 1'b0;

3) If mcu\_hold\_mode set 1'b1, configure one mcu\_frame\_st can send one frame data. If mcu\_hold\_mode set 1'b0, it will not hold.

- Bypass mode

1) Set dsp\_out\_mode(0x0028[19:16]) according to interface width.

2) Set mcu\_type, mcu\_bypass and mcu timing value in 0x0004 register.

mcu\_type = 1'b1;

mcu\_bypass = 1'b1;

mcu\_clk\_sel = 1'b0; MCU bypass sync with HCLK.

3) Write 0x018c register to send MCU command.

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## Chapter 5 Neural Process Unit (NPU)

### 5.1 Overview

NPU is the process unit which is dedicated to neural network. It is designed to accelerate the neural network arithmetic in field of AI (artificial intelligence) such as machine vision and natural language processing. The variety of applications for AI is expanding, and currently provides functionality in a variety of areas, including face tracking as well as gesture and body tracking, image classification, video surveillance, automatic speech recognition (ASR) and advanced driver assistance systems (ADAS).

NPU supports the following features:

- Host interface
  - 32bit AHB interface used for configuration only support single
  - 128bit AXI interface used to fetch data from memory
- Neural Network
  - Support integer 8, integer 16 convolution operation
  - Support Liner, Fully Connected, Fully Convolution
  - Unlimited network size (bound by system resource)
  - Supported DeepLearning Frameworks: TensorFlow, Pytorch, Caffe, ONNX, MxNet
  - Inference Engine : OpenVX, Android NN backend
  - Support network sparse coefficient decompression
  - Support Max, average pooling
  - Max pooling support 2x2, 3x3, stride  $\leq \min(\text{input width}, \text{input height})$
  - Local average pooling size  $\leq 11 \times 11$
  - Support unpooling
  - Support batch normalize, l2 normalize, l2 normalize scale, local response normalize
  - Support permute, reshape, concat, depth to space, space to depth, flatten, reorg, squeeze and split
  - Convolution size  $N \times N$ ,  $N \leq 11 \times \text{stride}$ , stride  $\leq \min(\text{input width}, \text{input height})$
  - Support dilate convolution,  $N \leq 11 \times \text{stride}$ , stride  $\leq \min(\text{input width}, \text{input height})$ , dilation  $< 1024$
  - Support de-convolution,  $N \leq 11 \times \text{stride}$ , stride  $\leq \min(\text{input width}, \text{input height})$
  - Support Elementwise addition, div, floor, max, mul, scale, sub
  - Support elu, leaky\_relu, prelu, relu, relu1, relu6, sigmoid, softmax, tanh
  - Support LSTM, RNN
  - Support channel shuffle
  - Support dequantize, dropout.

### 5.2 Block Diagram

NPU comprises with:

- HIF: Host Interface
- PM : Power Management
- NN Engine : Neural Network Engine
- VPU : Vector Procession Unit

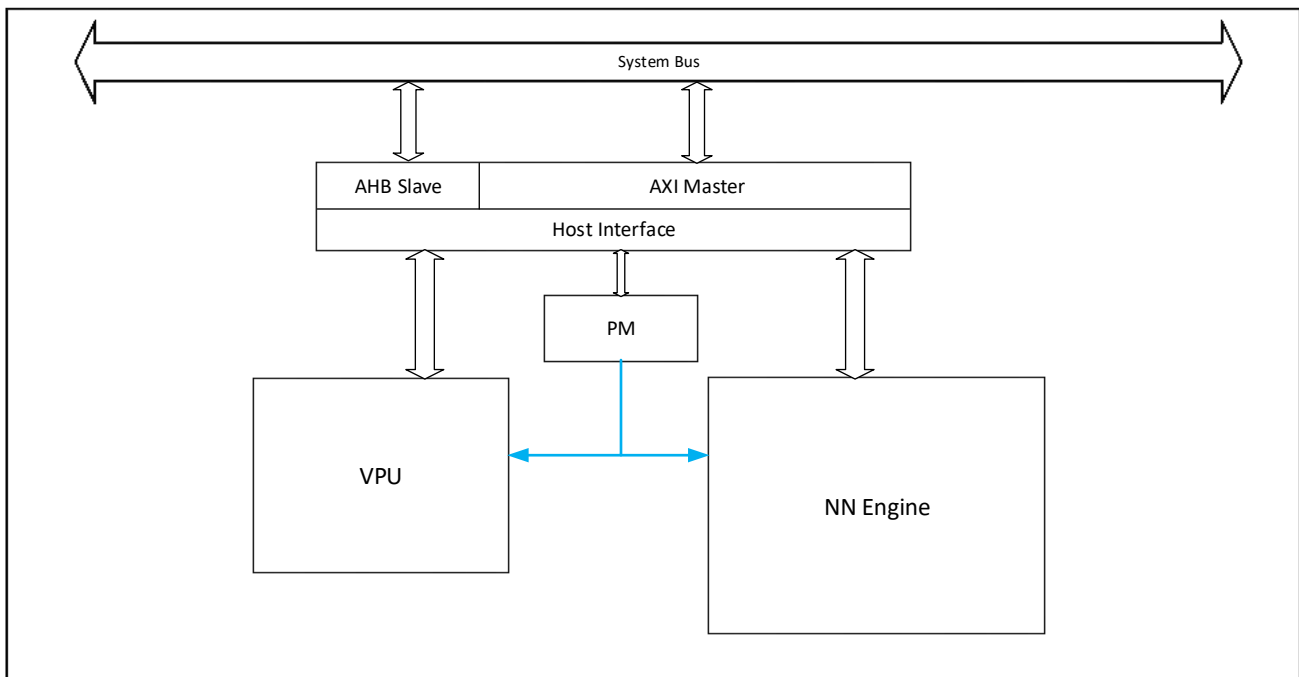


Fig. 5-1 NPU Block Diagram

## 5.3 Function Description

### 5.3.1 Host Interface

Allows the NPU to communicate with external memory and the CPU through the AXI or AHB bus. In this block data crosses clock domain boundaries. It includes a Front End (FE) to insert high level primitives and commands into the calculation pipeline. There is an AHB slave and AXI master in Host interface unit. The AXI master interface is used to fetch data from memory that is attached to the Soc AXI interconnect. The AHB slave interface is used to access the graphics registers for configuration, debug and test.

### 5.3.2 Power Management

Power management in NPU is used to provide top level controls for clock, reset and power management. AHB clock, AXI clock, clock for VPU and NN Engine are all asynchronization, and clock pins are connected to Power Management. The reset of all models are also controlled by Power Management. Global clock gating can be controlled by Power Management to reduce power.

### 5.3.3 Neural Network Engine

As the unit name, NN Engine is the main process unit for Neural Network arithmetic. This unit Provides parallel convolution MAC for recognition functions and int8, int16 are supported. Active functions and pooling such as leaky\_relu, relu, relu1, relu6, sigmoid, tanh are also processed in NN Engine. So NN Engine is mainly serve for convolution neural network and fully connected network.

### 5.3.4 Vector Processing Unit

Vector Processing Unit can be the supplement for NN Engine. The programmable SIMD processor unit is included which perform as a Compute Unit for OpenCL. VPU provides advanced image processing functions. For example, in one cycle, VPU can perform one MUL/ADD instruction or a dot product of two 16-component values. Most element wise operations and matrix operations are processed in VPU.

## 5.4 Register Description

### 5.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
<u>npu AQ HI CLOCK CONT</u> <u>ROL</u>	0x0000	W	0x00000100	Host interface control register



Name	Offset	Size	Reset Value	Description
<u>npu AQ HI IDLE</u>	0x0004	W	0x001C0009	Idle status register
<u>npu AQ AXI STATUS</u>	0x000C	W	0x00000000	Axi status register
<u>npu AQ INT ACKNOWLEDGE</u>	0x0010	W	0x00000000	Interrupt acknowledge register
<u>npu AQ INTR ENBL</u>	0x0014	W	0x00000000	Interrupt enable register
<u>npu GC TOTAL CYCLES</u>	0x0078	W	0x00000000	Total cycles
<u>npu GC REG HI CHIP PATCH REV</u>	0x0098	W	0x00000000	Patch revision level
<u>npu GC PRODUCT ID</u>	0x00A8	W	0x50080001	Product id
<u>npu GC ECOID</u>	0x00E8	W	0x00000000	ECO Id
<u>npu GC MODULE POWER CONT</u>	0x0100	W	0x00140020	Control register for module level power controls
<u>npu AQ MEMORY DEBUG</u>	0x0414	W	0x00000000	Limits the total number of outstanding read requests
<u>npu AQ REG TIMING CONTROL</u>	0x042C	W	0x00030000	Sleep and power down controls for memory
<u>npu GC MMU AHB CONTROL</u>	0x0388	W	0x00000000	Control register that enables the MMU (only time shot)
<u>npu GC MMU TABLE ADDRESS LOW</u>	0x038C	W	0x00000000	MMU Table Array Base Low 32bit address
<u>npu GC MMU TABLE ARRAY SIZE</u>	0x0394	W	0x0000FFFF	MMU Table Array Size
<u>npu GC MMU NON SECURE ADDR</u>	0x0398	W	0x00000000	A 64-byte address that will acts as a 'safe' zone
<u>npu GC MMU SECURE ADDRESS</u>	0x039C	W	0x00000000	A 64-byte address that will acts as a 'safe' zone
<u>npu GC CMD BUFFER AHB CTRL</u>	0x03A4	W	0x00000000	Command buffer control
<u>npu GC HI AHB CONTROL</u>	0x03A8	W	0x00000000	Debug and soft reset control
<u>npu GC AXI AHB CONFIG</u>	0x03AC	W	0x00222200	AXI control
<u>npu AQ CMD BUFFER ADDRESS</u>	0x0654	W	0x00000000	Base address for the command buffer
<u>npu AQ FE DEBUG CURRENT CMD ADR</u>	0x0664	W	0x00000000	This is the command decoder address

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

## 5.4.2 Detail Registers Description

### npu AQ HI CLOCK CONTROL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:20	RW	0x0	multi_pipe_reg_select Determines which HI/MC to use while reading registers.
19	RW	0x0	isolate_gpu Not applicable.
18:17	RO	0x0	reserved
16	RO	0x0	idle3_d 3D pipe is idle. 1'b0: 3D pipe is busy 1'b1: 3D pipe is idle
15:14	RO	0x0	reserved
13	RW	0x0	disable_ram_power_optimization Disables ram power optimization. 1'b0: Enables ram power optimization 1'b1: Disables ram power optimization
12:11	RO	0x0	reserved
10	RW	0x0	disable_ram_clock_gating Disables clock gating for rams. 1'b0: Enable ram clock gating 1'b1: Disable ram clock gating
9	RW	0x0	fscale_cmd_load Core clock frequency scale value 'enable. When writing a 1 to this bit, it updates the frequency scale factor with the value FSCALE_VAL[6:0]. The bit must be set back to 0 after that. If this bit is set and FSCALE_VAL=0 (an invalid combination), the HREADYOUT output signal will get stuck to 0.
8:2	RW	0x40	fscale_val Core clock frequency scale value.
1	RW	0x0	clk2d_dis Software clock disable signal. For this core both bits CLK3D_DIS and CLK2D_DIS should be controlled by software. The AXI interface clock is the only block not stalled at this point. 1'b0: Enable software clock 1'b1: Disable software clock
0	RW	0x0	clk3d_dis Disable 3D clock. Software core clock disable signal for 3d modules (clk_3d). When set to 1, this clock is frozen. 1'b0: Enable clk_3d 1'b1: Disable clk_3d

**npu AQ HI IDLE**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	axi_lp AXI is in low power mode. 1'b1: Axi is in low power mode.

Bit	Attr	Reset Value	Description
30:21	RO	0x000	reserved
20	RO	0x1	idle_vsc Vip Scaler is idle.
19	RO	0x1	idle_tb TP is idle.
18	RO	0x1	idle_nn NN is idle.
17:4	RO	0x0000	reserved
3	RO	0x1	idle_sh SH is idle. Shader Module. 1'b1: Sh is idle.
2:1	RO	0x0	reserved
0	RO	0x1	idle_fe FE is idle. 'Fetch Engine, Front End'. 1'b1: Fe is idle.

**npu AQ AXI STATUS**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	det_rd_err Detect read error.
8	RO	0x0	det_wr_err Detect write error.
7:4	RO	0x0	rd_err_id Read Error ID.
3:0	RO	0x0	wr_err_id Write Error ID.

**npu AQ INT ACKNOWLEDGE**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RC	0x00000000	intr_enbl_vec Each bit represents a corresponding event being triggered. Reading from this register clears the outstanding interrupt. For each interrupt event, 0=Clear, 1=Interrupt Active Bit 31 is AXI_BUS_ERROR interrupt.

**npu AQ INTR ENBL**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intr_enbl_vec 1'b0: Disable interrupt 1'b1: Enable interrupt

**npu GC TOTAL CYCLES**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cycles Total cycles. This register is a free running counter It can be reset by writing 0 to it.

**npu GC REG HI CHIP PATH REV**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	path_rev Patch revision level for the chip. This register has no set reset value. It varies with the implementation. READ ONLY.

**npu GC PRODUCT ID**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x50080001	id Shows Product ID. Reset values varies with the implementation. READ ONLY.

**npu GC ECOID**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	id Shows the ID for the chip ECO.

**npu GC MODULE POWER CONT**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0014	turn_off_counter Counter value for clock gating the module if the module is idle for this amount of clock cycles.
15:8	RO	0x00	reserved
7:4	RW	0x2	turn_on_counter Number of clock cycles to wait after turning on the clock.
3	RO	0x0	reserved
2	RW	0x0	disable_starve_module_clock_gating Disables module level clock gating for starve/idle condition. 1'b0: Enable 1'b1: Disable
1	RW	0x0	disable_stall_module_clock_gating Disables module level clock gating for stall condition. 1'b0: Enable 1'b1: Disable

Bit	Attr	Reset Value	Description
0	RW	0x0	enable_module_clock_gating Enables module level clock gating. 1'b0: Disable 1'b1: Enable

**npu\_AQ\_MEMORY\_DEBUG**

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	max_outstanding_reads Limits the total number of outstanding read requests.

**npu\_AQ\_REG\_TIMING\_CONTROL**

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	light_sleep Bit to allow SOC to manage light sleep for embedded memories.
21	RW	0x0	deep_sleep Deep sleep. Bit to allow SOC to manage deep sleep for embedded memories.
20	RW	0x0	power_down Power down memory.
19:18	RW	0x0	fast_wtc WTC for fast rams.
17:16	RW	0x3	fast_rtc RTC for fast rams.
15:8	RW	0x00	for_rf2p For 2 port RAM.
7:0	RW	0x00	for_rf1p For 1 port RAM.

**npu\_GC\_MMU\_AHB\_CONTROL**

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	mmu Enable the MMU. For security reasons, once the MMU is enabled it cannot be disabled anymore. 1'b0: Disable 1'b1: Enable

**npu\_GC\_MMU\_TABLE\_ADDR\_LOW**

Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address 32 bit Address for MMU Table Array Base Low 32bit.

**npu GC MMU TABLE ARRAY SIZE**

Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	size 16 bit MMU Table Array Size.

**npu GC MMU NON SECURE ADDR**

Address: Operational Base + offset (0x0398)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address A 64-byte address that will acts as a 'safe' zone. Any address that would cause an exception is routed to this safe zone. Reads will happened and writes will go to this address, but with a write-enable of 0. This register can only be programmed once after a reset, any attempt to write to this register after the initial write-after-reset will be ignored. This is in Non-Secure memory.

**npu GC MMU SECURE ADDR**

Address: Operational Base + offset (0x039C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address A 64-byte address that will acts as a 'safe' zone. Any address that would cause an exception is routed to this safe zone. Reads will happened and writes will go to this address, but with a write-enable of 0. This register can only be programmed once after a reset. Any attempt to write to this register after the initial write-after-reset will be ignored. This is in Secure memory.

**npu GC CMD BUFFER AHB CTRL**

Address: Operational Base + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	enable Enable the command parser. 1'b0: Enable 1'b1: Disable
15:0	WO	0x0000	prefetch Number of 64-bit words to fetch from the command buffer.

**npu GC HI AHB CONTROL**

Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	debug_mode Enable debug mode if disabled debug registers return 0xffffffff.
0	RW	0x0	soft_reset 1'b0: Disable 1'b1: Enable

**npu GC AXI AHB CONFIG**

Address: Operational Base + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x2	axcache_override_shared Configure AxCACHE value for shareable request.
19:18	RW	0x0	axidomain_non_shared Configure AxDOMAIN value for non-shareable request.
17:16	RW	0x2	axdomain_shared Configure AxDOMAIN value for shareable request.
15:12	RW	0x2	archche Set ARACHE[3:0] value.
11:8	RW	0x2	awchche Set AWCACHE[3:0] value.
7:0	RO	0x00	reserved

**npu AQ CMD BUFFER ADDR**

Address: Operational Base + offset (0x0654)

Bit	Attr	Reset Value	Description
31	WO	0x0	type 1'b0: System 1'b1: Virtual system
30:0	WO	0x00000000	address Base address for the command buffer. The address must be 64-bit aligned and it is always physical. To check the value of the current fetch address use AQ_FE_DEBUG_CUR_CMD_ADR.

**npu AQ FE DEBUG CUR CMD ADR**

Address: Operational Base + offset (0x0664)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	cur_cmd_adr This is the command decoder address. It has no reset value. READ ONLY.
2:0	RO	0x0	reserved

**5.5 Application Notes**

## 5.5.1 Clock and Reset

### 5.5.1.1 Clock Domains

The NPU module uses multiple clock domains, There are three independent clock domains.

- Core clock, which is the clock for NN engine and VPU. In this module shader clock (clksh) and clk\_3d are all indicated to core clk.
- AHB clock, which is the clock for AHB interface.
- AXI clock, which is the clock for AXI interface.

Communication between the different domains in NPU occurs mostly by way of asynchronous FIFOs. All clocks are asynchronous to each other. There is no communication between AHB and AXI clock domains.

Clock frequency can be controlled by CRU, please refer to the relevant sections.

Automatic localized clock gating is employed throughout the design in order to minimize the dynamic power consumption. Almost all of the flip-flops are clock gated in the design. Block level clock gating is implemented in a majority of the blocks. If a block and the interface to the block are both idle, then the clock of that block will be gated automatically. This feature can be disabled by software, please refer to GC\_MODULE\_POWER\_CONTRPLS.

### 5.5.1.2 NPU Reset

Correspond to the clock domain, there are three reset signals. Resetrn\_pin, the reset signal for NN Engine and VPU, which is synchronized to the core clock domain. HRESETn is the AHB interface reset pin and which is synchronized to the AHB clock domain. ARESETn is the AXI interface reset pin and which is synchronized to the AXI clock domain.

All the three signals must be asserted for a minimum of 32 core clock cycles, using the slowest of the three clocks. Then three signals must be release at the same time. For the correct reset, when the reset pin release, all three clocks must be slow down to 120M or below. Our suggestion is that configure CRU to the slowest clock frequency before reset, then after de-assertion, wait for 128 cycles of the slowest clock before recover to working frequency.

After the entire 32 cycle assertion and 128 cycle wait, AHB can be started.

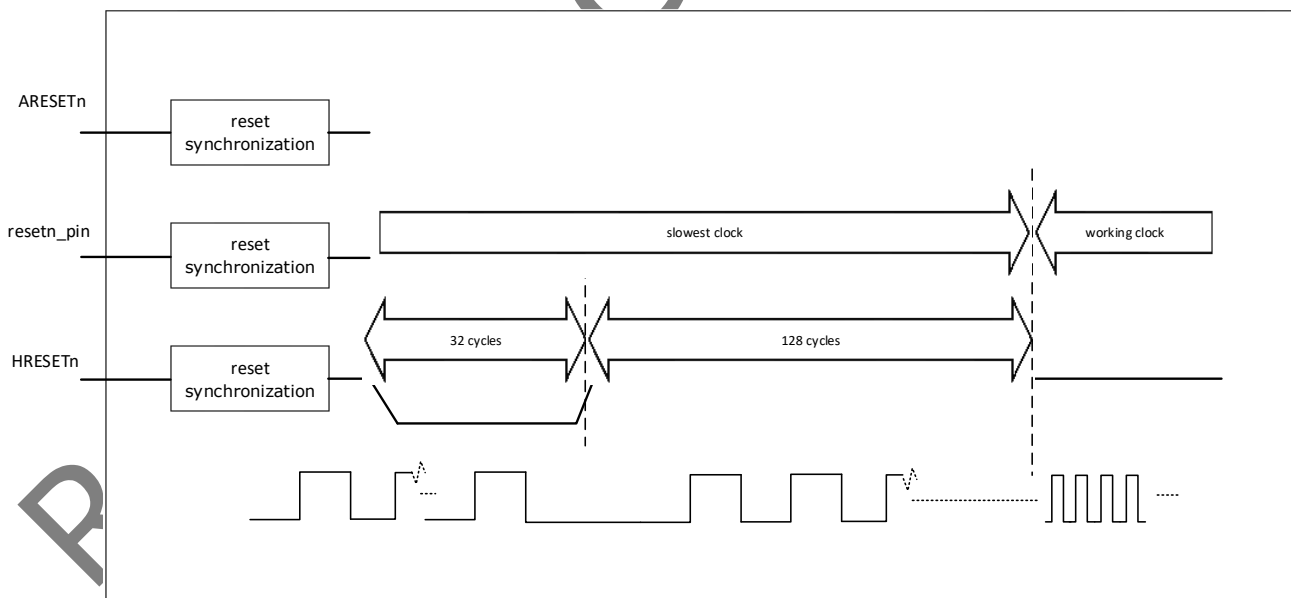


Fig. 5-2 NPU Reset Diagram

### 5.5.2 NPU Interrupt Application

NPU has 1 interrupt output signal and it remains asserted until the host processor clears the interrupt by reading the interrupt acknowledge register (AQ\_INTR\_ACKNOWLEDGE). Each bit of AQ\_INTR\_ACKNOWLEDGE represents one of the 32 possible events that the NPU can signal to the host processor. By setting the bits of the interrupt enable register (AQ\_INTR\_ENBL) the programmer can control which of those events will generate an interrupt. The bits of these registers have no predefined meaning, except for bit 31 which is used for AXI\_BUS\_ERROR.



### 5.5.3 NPU Debugging Support

For lab debugging, it is desirable to read register GRF\_SOC\_STATUS0.npu\_debug\_out to know the status of NPU. The debug idle status signals from the various functional blocks are very useful when the NPU is hung or in an unrecoverable state, as they provide visibility into the idle states of the blocks.

The single is 8 bits wide and it shows here.

Table 5-1 NPU Debug Signal

Bit location	Description
7:4	reserved
3	1'b0: VPU is busy 1'b1: VPU is idle
2	reserved
1	1'b0: NPU is busy 1'b1: All NPU is idle
0	1'b0: Front End block is busy 1'b1: Front End block is idle

## Chapter 6 MIPI DSI D-PHY

### 6.1 Overview

The MIPI D-PHY integrates a MIPI® V1.2 compatible PHY that supports up to 2.0Gbps high speed data receiver, plus a MIPI® low-power low speed transceiver that supports data transfer in the bi-directional mode. The IP supports the full specifications described in V1.2 of the D-PHY spec. The D-PHY is built in with a standard digital interface to talk to any third party Host controller. The architecture supports connection of multiple data lanes in parallel – up to 4 data lanes can be connected to increase the total through-put, customizable to user determined configurations. The I/O and ESD are also built-in as one in a rectangular footprint for any configuration (one lane to 4 lanes or more). It is optimized for high speed applications with robust timing and small silicon area. The D-PHY supports the electrical portion of MIPI D-PHY V1.0 standard, covering all transmission modes (ULP/LP/HS). The MIPI D-PHY cost-effectively adds MIPI D-PHY V1.2 capability to any SOC used in communication and consumer electronics field.

- The MIPI D-PHY supports the following features:
- Mixed-signal D-PHY mixed-signal hard-macro- HS/LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.2 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™
- MIPI® protocols
- 1.0Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4.0Gbps transfer rate
- MIPI-HS, MIPI-LP modes supported
- Skew-calibration supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: less than 22mA/Lane in HS TX/RX mode
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

### 6.2 Block Diagram

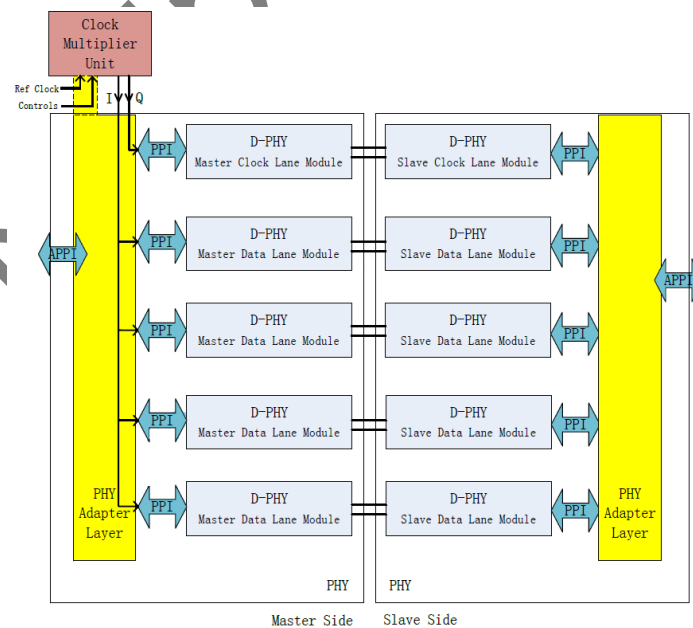


Fig. 6-1 MIPI DSI D-PHY Detailed Block Diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure 1 shows the DPHY architecture.

### 6.3 Function Description

### 6.3.1 System Connection

The MIPI DPHY supports DSI mode as shown in following figure:



Fig. 6-2 MIPI DSI D-PHY VOP Connection

### 6.3.2 MIPI Mode

In MIPI mode, there are some functions of DPHY controlled by grf registers. These register bit and function is show in following table:

Table 6-1 Function of GRF Bits in MIPI Mode

register bit	function
dsi_phy_lane0_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
dsi_phy_lane1_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
dsi_phy_lane2_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
dsi_phy_lane3_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
dsi_phy_lane0_turndisable	Disable Turn-around. This signal is used to prevent a (bi-directional) Lane from going into transmit mode – even if it observes a turn-around request on the Lane interconnect.
dsi_phy_forcerxmode	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.

### 6.3.3 Program PLL in MIPI Mode

The PLL output frequency can be calculated using a simple formula:

$$\text{PLL\_Output\_Frequency} = (\text{FREF}/\text{PREDIV} * \text{FBDIV})/\text{POSTDIV}$$

PLL\_Output\_Frequency: It is equal to DDR\_Clock\_Frequency \* 2.

FREF: 24 MHz.

PREDIV: PLL input reference clock divider which can be configured by the register of prediv.

FBDIV: Integer value programmed into feedback divider which can be configured by the register of fbdiv.

POSTDIV: PLL post-divider 2 can be configured by the registers of reg\_postdiv. If reg\_postdiv is set to 1, the POSTDIV value is 2, otherwise, the value is 1.

Additional Programming Considerations:

1. The divided reference frequency (FREF/PREDIV) should be less than 40MHz.
2. The all possible settings of feedback divider are 12, 13, 14, 16~511.

## 6.4 Register Description

### 6.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 6.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DPHY PHY CTRL LANE ENABLE	0x0000	W	0x00000000	Lane enable
DPHY PHY CTRL PWR CTRL	0x0004	W	0x00000000	Power control
DPHY PHY CTRL PREDIV	0x000C	W	0x00000000	PLL PREDIV
DPHY PHY CTRL FBDIV	0x0010	W	0x00000000	Integer value programmed into feedback divider
DPHY PHY CLK LANE SKEW PHASE	0x0014	W	0x00000000	Clock lane skew phase
DPHY DAT LANE23 SKEW PHASE	0x0018	W	0x00000000	Data2/3 lane skew phase
DPHY DAT LANE01 SKEW PHASE	0x001C	W	0x00000000	Data0/1 lane skew phase
DPHY PLL post divider	0x0020	W	0x00000000	PLL post divider
DPHY CLK LANE VOD	0x002C	W	0x00000000	Clock lane Vod
DPHY DATA SAMPLE PHASES	0x0044	W	0x00000000	Data sample phases
DPHY PRE EMPHSIZE EN	0x0060	W	0x00000000	
DPHY DIGITAL CTRL	0x0080	W	0x00000000	digital control
DPHY INVERT CLK	0x0084	W	0x00000000	Inverting clock
DPHY PHY CLK LANE SWAP	0x0100	W	0x00000000	Clock lane differential signals swap
DPHY PHY CLK LANE TLPX	0x0114	W	0x00000000	Clock lane TLPX
DPHY PHY CLK LANE HS TXTHSPREPREARE	0x0118	W	0x00000000	Clock lane HSTXTHSPREPREARE
DPHY PHY CLK LANE HS TXTZERO	0x011C	W	0x00000000	Clock lane THSZERO
DPHY PHY CLK LANE HS TXTTRAIL	0x0120	W	0x00000000	Clock lane THSTRAIL
DPHY PHY CLK LANE HS TXTEXTIT	0x0124	W	0x00000000	Clock lane THSEXIT
DPHY PHY CLK LANE TCLKPOST	0x0128	W	0x00000000	Clock lane TCLKPOST
DPHY PHY CLK LANE LPDT	0x0130	W	0x00000000	Clock lane LPDT control
DPHY PHY CLK LANE TWAKUP	0x0134	W	0x00000000	Clock lane HS Twakup
DPHY PHY CLK LANE TP RE	0x0138	W	0x00000000	Clock lane TP RE
DPHY PHY CLK LANE TT AGO	0x0140	W	0x00000000	Clock lane TT AGO
DPHY PHY CLK LANE TT ASURE	0x0144	W	0x00000000	Clock lane TT ASURE
DPHY PHY CLK LANE TT AWAIT	0x0148	W	0x00000000	Clock lane TT AWAIT
DPHY PHY DATA0 LANE SWAP	0x0180	W	0x00000000	Data0 lane differential signals swap

Name	Offset	Size	Reset Value	Description
<u>DPHY PHY DATA0 LANE TLPX</u>	0x0194	W	0x00000000	Data0 lane TLPX
<u>DPHY PHY DATA0 LANE HSTXTHSPREPARE</u>	0x0198	W	0x00000000	Data0 lane HSTXTHSPREPARE
<u>DPHY PHY DATA0 LANE HSTXTZERO</u>	0x019C	W	0x00000000	Data0 lane THSZERO
<u>DPHY PHY DATA0 LANE HSTXTTRAIL</u>	0x01A0	W	0x00000000	Data0 lane THSTRAIL
<u>DPHY PHY DATA0 LANE HSTXTEXIT</u>	0x01A4	W	0x00000000	Data0 lane THSEXIT
<u>DPHY PHY DATA0 LANE TDATA0POST</u>	0x01A8	W	0x00000000	Data0 lane TCLKPOST
<u>DPHY PHY DATA0 LANE LPDT</u>	0x01B0	W	0x00000000	Data0 lane LPDT control
<u>DPHY PHY DATA0 LANE TWAKUP</u>	0x01B4	W	0x00000000	Data0 lane HS Twakup
<u>DPHY PHY DATA0 LANE TPRE</u>	0x01B8	W	0x00000000	Data0 lane TPRE
<u>DPHY PHY DATA0 LANE TTAGO</u>	0x01C0	W	0x00000000	Data0 lane TTAGO
<u>DPHY PHY DATA0 LANE TTASURE</u>	0x01C4	W	0x00000000	Data0 lane TTASURE
<u>DPHY PHY DATA0 LANE TTAWAIT</u>	0x01C8	W	0x00000000	Data0 lane TTAWAIT
<u>DPHY PHY DATA1 LANE SWAP</u>	0x0200	W	0x00000000	Data1 lane differential signals swap
<u>DPHY PHY DATA1 LANE TLPX</u>	0x0214	W	0x00000000	Data1 lane TLPX
<u>DPHY PHY DATA1 LANE HSTXTHSPREPARE</u>	0x0218	W	0x00000000	Data1 lane HSTXTHSPREPARE
<u>DPHY PHY DATA1 LANE HSTXTZERO</u>	0x021C	W	0x00000000	Data1 lane THSZERO
<u>DPHY PHY DATA1 LANE HSTXTTRAIL</u>	0x0220	W	0x00000000	Data1 lane THSTRAIL
<u>DPHY PHY DATA1 LANE HSTXTEXIT</u>	0x0224	W	0x00000000	Data1 lane THSEXIT
<u>DPHY PHY DATA1 LANE TDATA1POST</u>	0x0228	W	0x00000000	Data1 lane TCLKPOST
<u>DPHY PHY DATA1 LANE LPDT</u>	0x0230	W	0x00000000	Data1 lane LPDT control
<u>DPHY PHY DATA1 LANE TWAKUP</u>	0x0234	W	0x00000000	Data1 lane HS Twakup
<u>DPHY PHY DATA1 LANE TPRE</u>	0x0238	W	0x00000000	Data1 lane TPRE
<u>DPHY PHY DATA1 LANE TTAGO</u>	0x0240	W	0x00000000	Data1 lane TTAGO
<u>DPHY PHY DATA1 LANE TTASURE</u>	0x0244	W	0x00000000	Data1 lane TTASURE
<u>DPHY PHY DATA1 LANE TTAWAIT</u>	0x0248	W	0x00000000	Data1 lane TTAWAIT
<u>DPHY PHY DATA2 LANE SWAP</u>	0x0280	W	0x00000000	Data2 lane differential signals swap

Name	Offset	Size	Reset Value	Description
DPHY PHY DATA2 LANE TLPX	0x0294	W	0x00000000	Data2 lane TLPX
DPHY PHY DATA2 LANE HSTXTHSPREPARE	0x0298	W	0x00000000	Data2 lane HSTXTHSPREPARE
DPHY PHY DATA2 LANE HSTXTZERO	0x029C	W	0x00000000	Data2 lane THSZERO
DPHY PHY DATA2 LANE HSTXTTRAIL	0x02A0	W	0x00000000	Data2 lane THSTRAIL
DPHY PHY DATA2 LANE HSTXTEXIT	0x02A4	W	0x00000000	Data2 lane THSEXIT
DPHY PHY DATA2 LANE TDATA2POST	0x02A8	W	0x00000000	Data2 lane TCLKPOST
DPHY PHY DATA2 LANE LPDT	0x02B0	W	0x00000000	Data2 lane LPDT control
DPHY PHY DATA2 LANE TWAKUP	0x02B4	W	0x00000000	Data2 lane HS Twakup
DPHY PHY DATA2 LANE TPRES	0x02B8	W	0x00000000	Data2 lane TPRES
DPHY PHY DATA2 LANE TTAGO	0x02C0	W	0x00000000	Data2 lane TTAGO
DPHY PHY DATA2 LANE TTASURE	0x02C4	W	0x00000000	Data2 lane TTASURE
DPHY PHY DATA2 LANE TTAWAIT	0x02C8	W	0x00000000	Data2 lane TTAWAIT
DPHY PHY DATA3 LANE SWAP	0x0300	W	0x00000000	Data3 lane differential signals swap
DPHY PHY DATA3 LANE TLPX	0x0314	W	0x00000000	Data3 lane TLPX
DPHY PHY DATA3 LANE HSTXTHSPREPARE	0x0318	W	0x00000000	Data3 lane HSTXTHSPREPARE
DPHY PHY DATA3 LANE HSTXTZERO	0x031C	W	0x00000000	Data3 lane THSZERO
DPHY PHY DATA3 LANE HSTXTTRAIL	0x0320	W	0x00000000	Data3 lane THSTRAIL
DPHY PHY DATA3 LANE HSTXTEXIT	0x0324	W	0x00000000	Data3 lane THSEXIT
DPHY PHY DATA3 LANE TDATA3POST	0x0328	W	0x00000000	Data3 lane TCLKPOST
DPHY PHY DATA3 LANE LPDT	0x0330	W	0x00000000	Data3 lane LPDT control
DPHY PHY DATA3 LANE TWAKUP	0x0334	W	0x00000000	Data3 lane HS Twakup
DPHY PHY DATA3 LANE TPRES	0x0338	W	0x00000000	Data3 lane TPRES
DPHY PHY DATA3 LANE TTAGO	0x0340	W	0x00000000	Data3 lane TTAGO
DPHY PHY DATA3 LANE TTASURE	0x0344	W	0x00000000	Data3 lane TTASURE
DPHY PHY DATA3 LANE TTAWAIT	0x0348	W	0x00000000	Data3 lane TTAWAIT

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 6.4.3 Detail Registers Description

#### DPHY PHY CTRL LANE ENABLE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	Bandgap power down enable 1'b0:Power on 1'b1:Power down
6	RW	0x0	Lane_en_4 Lane 4 enable.
5	RW	0x0	Lane_en_3 Lane 3 enable.
4	RW	0x0	Lane_en_2 Lane 2 enable.
3	RW	0x0	Lane_en_1 Lane 1 enable.
2	RW	0x0	lane_en_0 Lane 0 enable.
1:0	RW	0x0	power_work 2'b0x:Power work enable. 2'b10:Power work disable. 2'b11:Reserved.

#### **DPHY PHY CTRL PWR CTRL**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	syncrst Analog reset
1	RW	0x0	ido_pd LDO power down
0	RW	0x0	pll_pd PLL power down

#### **DPHY PHY CTRL PREDIV**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5	RW	0x0	reg_fbdiv[8] integer valude programmed into feedback divider.
4:0	RW	0x00	reg_prediv PLL input reference clock divider.

#### **DPHY PHY CTRL FBDIV**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x00000000	reserved
7:0	RW	0x00	reg_fbdiv[7:0] PLL input reference clock divider.

#### **DPHY PHY CLK LANE SKEW PHASE**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	clk_lane_skew_phase clock lane skew phase set: 3'b000:phase0 3'b001:phase1 3'b010:phase2 3'b011:phase3 3'b100:phase4 3'b101:phase5 3'b110:phase6 3'b111:phase7

**DPHY DAT LANE23 SKEW PHASE**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ido_output_bit1 Ldo output set bit1 for HS Vcom. 2'b00:Ido output is set as 400mv. 2'b01:Ido output is set as 400mv. 2'b10:Ido output is set as 430mv. 2'b11:Ido output is set as 460mv.
6:4	RW	0x0	dat_lane3_skew_phase data lane3 skew phase set: 3'b000:phase0 3'b001:phase1 3'b010:phase2 3'b011:phase3 3'b100:phase4 3'b101:phase5 3'b110:phase6 3'b111:phase7
3	RW	0x0	ido_output_bit0 Ldo output set bit0 for HS Vcom. 2'b00:Ido output is set as 400mv. 2'b01:Ido output is set as 400mv. 2'b10:Ido output is set as 430mv. 2'b11:Ido output is set as 460mv.
2:0	RW	0x0	dat_lane2_skew_phase data lane2 skew phase set: 3'b000:phase0 3'b001:phase1 3'b010:phase2 3'b011:phase3 3'b100:phase4 3'b101:phase5 3'b110:phase6 3'b111:phase7

**DPHY DAT LANE01 SKEW PHASE**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved



Bit	Attr	Reset Value	Description
7	RW	0x0	pre_emphasis_bit1 pre-emphasis range set bit1 2'b00:min-range 2'b01:mid_range 2'b11:max-range
6:4	RW	0x0	dat_lane1_skew_phase data lane1 skew phase set: 3'b000:phase0 3'b001:phase1 3'b010:phase2 3'b011:phase3 3'b100:phase4 3'b101:phase5 3'b110:phase6 3'b111:phase7
3	RW	0x0	pre_emphasis_bit0 pre-emphasis range set bit0 2'b00:min-range 2'b01:mid_range 2'b11:max-range
2:0	RW	0x0	dat_lane0_skew_phase data lane0 skew phase set: 3'b000:phase0 3'b001:phase1 3'b010:phase2 3'b011:phase3 3'b100:phase4 3'b101:phase5 3'b110:phase6 3'b111:phase7

**DPHY PLL post divider**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	PLL_post_divider The PLL post-divider 2 can be enable.
4	RO	0x0	reserved
3:0	RW	0x0	data_lanes_vod data lanes Vod range set: 4'b0000:min-range 4'b0011:mid-range 4'b0111:bigger-range 4'b1111:max-range

**DPHY CLK LANE VOD**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	clk_lane_vod clock lanes Vod range set: 4'b0000:min-range 4'b0011:mid-range 4'b0111:bigger-range 4'b1111:max-range

**DPHY DATA SAMPLE PHASES**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	data_sample_phases Data sample phases set: 2'b00:data sample phase 0 2'b01:data sample phase 1 2'b10:data sample phase 2 2'b11:data sample phase 3
5:0	RO	0x00	reserved

**DPHY PRE EMPHSIZE EN**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	pre_emphsize_clk_en 1'b0 : disable 1'b1 : enable
6	RW	0x0	pre_emphsize_lane0_en 1'b0 : disable 1'b1 : enable
5	RW	0x0	pre_emphsize_lane1_en 1'b0 : disable 1'b1 : enable
4	RW	0x0	pre_emphsize_lane2_en 1'b0 : disable 1'b1 : enable
3	RW	0x0	pre_emphsize_lane3_en 1'b0 : disable 1'b1 : enable
2:0	RO	0x0	reserved

**DPHY DIGITAL CTRL**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	reg_dig_resetrn 1'b0:reset 1'b1:normal

**DPHY INVERT CLK**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	invert_txclkesc 1'b0:disable 1'b1:enable
0	RW	0x0	invert_txbyteclkhs 1'b0:disable 1'b1:enable

**DPHY PHY CLK LANE SWAP**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	clk_lane_swap Differential signals swap enable. 1'b0:disable 1'b1:enable
3:0	RO	0x0	reserved

**DPHY\_PHY\_CLK\_LANE\_TLPX**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	thstlpx The value of counter for HS tlpX Time $\text{tpin\_txbyteclkhs} * (2 + \text{value})$

**DPHY\_PHY\_CLK\_LANE\_HSTXTHSPREPRE**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	thszero_bit7 The value of counter for HS Ths-zero:HSTXTHZERO[6].
6:0	RW	0x00	thsprepare The value of counter for HS Ths-prepare. For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI).For clock lane, s_hstxthsprpr[6:0] = 7'b0000011. For data lane, s_hstxthsprpr[6:0] = 7'b0000011. Frequency(1/UI) value(HEX) 80-110MHz 7f 110-150 MHz 7f 150-200 MHz 7f 200-250 MHz 7f 250-300 MHz 7f 300-400 MHz 7e 400-500 MHz 70 500-600 MHz 60 600-700 MHz 40 700-800 MHz 02 800-1000 MHz 08 1000-1200Mhz 03 1200-1400Mhz 03 1400-1600Mhz 42 1600-1800Mhz 47 1800-2000Mhz 64

**DPHY\_PHY\_CLK\_LANE\_HSTXTZERO**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	<p>thszero</p> <p>For clock lane, Ths-prepare+Ths-zero (<math>\geq 300\text{ns}</math>). For data lane, Ths-prepare+Ths-zero (<math>\geq 145\text{ ns} + 10*UI</math>) = <math>T_{pin\_txbyteclkhs}*(5+value)</math>. For clock lane, <math>s\_hstxthszero[5:0] = 6'b100000</math>.</p> <p>Frequency(1/UI) Value(HEX)</p> <p>80 -110 MHz 16</p> <p>110-150 MHz 16</p> <p>150-200 MHz 17</p> <p>200-250 MHz 17</p> <p>250-300 MHz 18</p> <p>300-400 MHz 19</p> <p>400-500 MHz 1B</p> <p>500-600 MHz 1D</p> <p>600-700 MHz 1E</p> <p>700-800 MHz 1F</p> <p>800-1000 MHz 20</p> <p>1000-1200Mhz 32</p> <p>1200-1400Mhz 32</p> <p>1400-1600Mhz 36</p> <p>1600-1800Mhz 7a</p> <p>1800-2000Mhz 7a</p>

**DPHY\_PHY\_CLK\_LANE\_HSTXTTRAIL**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	<p>thstrail</p> <p>The value of counter for HS Ths-trail. For clock lane, Ths-trail (<math>\geq 60\text{ns}</math>). For data lane, Ths-trail (<math>\geq \max(8UI, 60\text{ns}+4UI)</math>). For clock lane, <math>s\_hstxthstrail[6:0] = 7'b0000111</math>. For data lane, <math>s\_hstxthstrail[6:0] = 7'b0000111</math>. Frequency(1/UI) Value(HEX)</p> <p>80 -110 MHz 02</p> <p>110-150 MHz 02</p> <p>150-200 MHz 02</p> <p>200-250 MHz 04</p> <p>250-300 MHz 04</p> <p>300-400 MHz 04</p> <p>400-500 MHz 08</p> <p>500-600 MHz 10</p> <p>600-700 MHz 30</p> <p>700-800 MHz 30</p> <p>800-1000 MHz 30</p> <p>1000-1200Mhz 0f</p> <p>1200-1400Mhz 0f</p> <p>1400-1600Mhz 0f</p> <p>1600-1800Mhz 0f</p> <p>1800-2000Mhz 0b</p>

**DPHY\_PHY\_CLK\_LANE\_HSTXTEXT**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	thsexit The value of counter for HS ths-exit. Ths-exit = $Tpin\_txbyteclkhs \times value$

**DPHY PHY CLK LANE TCLKPOST**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thspost The value of counter for HS tclk-post. Tclk-post = $Tpin\_txbyteclkhs \times value$ .

**DPHY PHY CLK LANE LPDT**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	lpdt_synchronization LPDT TX PPI signals internal synchronization enable. 1'b0:disable 1'b1:enable
1:0	RW	0x0	thstwakup_bit89 The value[9:8] of counter for HS Twakup.

**DPHY PHY CLK LANE TWAKUP**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0x00	thstwakup The value[7:0] of counter for HS Twakup. Twakup for ulpm, Twakup = $Tpin\_sys\_clk \times value[9:0]$ .

**DPHY PHY CLK LANE TPRES**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3:0	RW	0x0	thstpre The value of counter for HS Tpre. Tpre = $Ttxbyteclkhs \times value$ .

**DPHY PHY CLK LANE TTAGO**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x0	thspost_high_2bits The value of counter tor HS Tpost high 2bits
5:0	RW	0x00	thsttago

**DPHY PHY CLK LANE TTASURE**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	thstexit_high_1bit The value of counter for HS Ths-exit high 1bit.
5:0	RW	0x00	thsttasure The value of counter for HS ttasure.

**DPHY PHY CLK LANE TTAWAIT**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	thsttawait The value of counter for HS tta-wait.Tta-wait for turnaround.Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHY PHY DATA0 LANE SWAP**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	data0_lane_swap Differential signals swap enable. 1'b0:disable 1'b1:enable
3:0	RO	0x0	reserved

**DPHY PHY DATA0 LANE TLPX**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	hs_tlp The value of counter for HS tlp Time $\text{Time} \geq \text{tlpx} \times \text{tpin\_txbyteclkhs} * (2 + \text{value})$

**DPHY PHY DATA0 LANE HSTXTHSPREPARE**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	thszero_bit7 The value of counter for HS Ths-zero:HSTXTHZERO[6].

Bit	Attr	Reset Value	Description
6:0	RW	0x00	<p>thsprepare</p> <p>The value of counter for HS Ths-prepare. For clock lane, Ths-prepar(38ns~95ns)</p> <p>For data lane, Ths-prepare(40ns+4UI~85ns+6UI).For clock lane,s_hstxthsprpr[6:0] = 7'b0000011.For data lane, s_hstxthsprpr[6:0] = 7'b0000011.Frequency(1/UI) value(HEX)</p> <p>80-110MHz 7f</p> <p>110-150 MHz 7f</p> <p>150-200 MHz 7f</p> <p>200-250 MHz 7f</p> <p>250-300 MHz 7f</p> <p>300-400 MHz 7e</p> <p>400-500 MHz 70</p> <p>500-600 MHz 60</p> <p>600-700 MHz 40</p> <p>700-800 MHz 02</p> <p>800-1000 MHz 08</p> <p>1000-1200Mhz 03</p> <p>1200-1400Mhz 03</p> <p>1400-1600Mhz 42</p> <p>1600-1800Mhz 47</p> <p>1800-2000Mhz 64</p>

**DPHY PHY DATA0 LANE HSTXTZERO**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	<p>thszero</p> <p>For clock lane, Ths-prepare+Ths-zero (<math>\geq 300</math>ns). For data lane, Ths-prepare+Ths-zero (<math>\geq 145</math> ns + <math>10 \times \text{UI}</math>) = <math>T_{pin\_txbyteclkhs} \times (5 + \text{value})</math>. For clock lane, s_hstxthszero[5:0] = 6'b100000.</p> <p>Frequency(1/UI) Value(HEX)</p> <p>80 -110 MHz 16</p> <p>110-150 MHz 16</p> <p>150-200 MHz 17</p> <p>200-250 MHz 17</p> <p>250-300 MHz 18</p> <p>300-400 MHz 19</p> <p>400-500 MHz 1B</p> <p>500-600 MHz 1D</p> <p>600-700 MHz 1E</p> <p>700-800 MHz 1F</p> <p>800-1000 MHz 20</p> <p>1000-1200Mhz 32</p> <p>1200-1400Mhz 32</p> <p>1400-1600Mhz 36</p> <p>1600-1800Mhz 7a</p> <p>1800-2000Mhz 7a</p>

**DPHY PHY DATA0 LANE HSTXTTRAIL**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	thstrail The value of counter for HS Ths-trail. For clock lane, Ths-trail ( $\geq 60\text{ns}$ ). For data lane, Ths-trail ( $\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$ ). For clock lane, s_hstxthstrail[6:0] = 7'b0000111. For data lane, s_hstxthstrail[6:0] = 7'b0000111. Frequency(1/UI) Value(HEX) 80 -110 MHz 02 110-150 MHz 02 150-200 MHz 02 200-250 MHz 04 250-300 MHz 04 300-400 MHz 04 400-500 MHz 08 500-600 MHz 10 600-700 MHz 30 700-800 MHz 30 800-1000 MHz 30 1000-1200Mhz 0f 1200-1400Mhz 0f 1400-1600Mhz 0f 1600-1800Mhz 0f 1800-2000Mhz 0b

**DPHY PHY DATA0 LANE HSTXTEXTIT**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	thsexit The value of counter for HS ths-exit. Ths-exit = Tpin_txbyteclkhs*value

**DPHY PHY DATA0 LANE TDATA0POST**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thspost The value of counter for HS tclk-post. Tclk-post = Tpin_txbyteclkhs*value.

**DPHY PHY DATA0 LANE LPDT**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	lpdt_synchronization LPDT TX PPI signals internal synchronization enable. 1'b0:disable 1'b1:enable
1:0	RW	0x0	thstwakeup_bit89 The value[9:8] of counter for HS Twakeup.

**DPHY PHY DATA0 LANE TWAKUP**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved



Bit	Attr	Reset Value	Description
7:0	RW	0x00	thstwakup The value[7:0] of counter for HS Twakup. Twakup for ulpm, Twakup = Tpin_sys_clk*value[9:0].

**DPHY PHY DATA0 LANE TPRE**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thstpre The value of counter for HS Tpre. Tpre = Ttxbyteclkhs*value.

**DPHY PHY DATA0 LANE TTAGO**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x0	thspost_high_2bits The value of counter for HS Tpost high 2bits
5:0	RW	0x00	thsttago

**DPHY PHY DATA0 LANE TTASURE**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	thstexit_high_1bit The value of counter for HS Ths-exit high 1bit.
5:0	RW	0x00	thsttasure The value of counter for HS ttasure.

**DPHY PHY DATA0 LANE TTAWAIT**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	thsttawait The value of counter for HS tta-wait. Tta-wait for turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHY PHY DATA1 LANE SWAP**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	data1_lane_swap Differential signals swap enable. 1'b0:disable 1'b1:enable
3:0	RO	0x0	reserved

**DPHY PHY DATA1 LANE TLPX**

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	hs_tlp The value of counter for HS tlp Time $\text{hs\_tlp} \times \text{hs\_tclk} = \text{tpin\_txbyteclkhs} * (2 + \text{value})$

**DPHY PHY DATA1 LANE HSTXTHSPREPRE**

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	thszero_bit The value of counter for HS Ths-zero: HSTXTHZERO[6].
6:0	RW	0x00	thsprepare The value of counter for HS Ths-prepare. For clock lane, Ths-prepar(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI). For clock lane, s_hstxthsprpr[6:0] = 7'b0000011. For data lane, s_hstxthsprpr[6:0] = 7'b0000011. Frequency(1/UI) value(HEX) 80-110MHz 7f 110-150 MHz 7f 150-200 MHz 7f 200-250 MHz 7f 250-300 MHz 7f 300-400 MHz 7e 400-500 MHz 70 500-600 MHz 60 600-700 MHz 40 700-800 MHz 02 800-1000 MHz 08 1000-1200Mhz 03 1200-1400Mhz 03 1400-1600Mhz 42 1600-1800Mhz 47 1800-2000Mhz 64

**DPHY PHY DATA1 LANE HSTXTZERO**

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	<p>thszero</p> <p>For clock lane, Ths-prepare+Ths-zero (<math>\geq 300\text{ns}</math>). For data lane, Ths-prepare+Ths-zero (<math>\geq 145\text{ ns} + 10*UI</math>) = <math>T_{pin\_txbyteclkhs}*(5+value)</math>. For clock lane, <math>s\_hstxthszero[5:0] = 6'b100000</math>.</p> <p>Frequency(1/UI) Value(HEX)</p> <p>80 -110 MHz 16</p> <p>110-150 MHz 16</p> <p>150-200 MHz 17</p> <p>200-250 MHz 17</p> <p>250-300 MHz 18</p> <p>300-400 MHz 19</p> <p>400-500 MHz 1B</p> <p>500-600 MHz 1D</p> <p>600-700 MHz 1E</p> <p>700-800 MHz 1F</p> <p>800-1000 MHz 20</p> <p>1000-1200Mhz 32</p> <p>1200-1400Mhz 32</p> <p>1400-1600Mhz 36</p> <p>1600-1800Mhz 7a</p> <p>1800-2000Mhz 7a</p>

**DPHY PHY DATA1 LANE HSTXTTRAIL**

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	<p>thstrail</p> <p>The value of counter for HS Ths-trail. For clock lane, Ths-trail (<math>\geq 60\text{ns}</math>). For data lane, Ths-trail (<math>\geq \max(8UI, 60\text{ns}+4UI)</math>). For clock lane, <math>s\_hstxthstrail[6:0] = 7'b0000111</math>. For data lane, <math>s\_hstxthstrail[6:0] = 7'b0000111</math>. Frequency(1/UI) Value(HEX)</p> <p>80 -110 MHz 02</p> <p>110-150 MHz 02</p> <p>150-200 MHz 02</p> <p>200-250 MHz 04</p> <p>250-300 MHz 04</p> <p>300-400 MHz 04</p> <p>400-500 MHz 08</p> <p>500-600 MHz 10</p> <p>600-700 MHz 30</p> <p>700-800 MHz 30</p> <p>800-1000 MHz 30</p> <p>1000-1200Mhz 0f</p> <p>1200-1400Mhz 0f</p> <p>1400-1600Mhz 0f</p> <p>1600-1800Mhz 0f</p> <p>1800-2000Mhz 0b</p>

**DPHY PHY DATA1 LANE HSTXTEXIT**

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	thsexit The value of counter for HS ths-exit. Ths-exit = Tpin_txbyteclkhs*value

**DPHY PHY DATA1 LANE TDATA1POST**

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thspost The value of counter for HS tclk-post. Tclk-post = Tpin_txbyteclkhs*value.

**DPHY PHY DATA1 LANE LPDT**

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	lpdt_synchronization LPDT TX PPI signals internal synchronization enable. 1'b0:disable 1'b1:enable
1:0	RW	0x0	thstwakup_bit89 The value[9:8] of counter for HS Twakup.

**DPHY PHY DATA1 LANE TWAKUP**

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0x00	thstwakup The value[7:0] of counter for HS Twakup. Twakup for ulpm, Twakup = Tpin_sys_clk*value[9:0].

**DPHY PHY DATA1 LANE TPRES**

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3:0	RW	0x0	thstpre The value of counter for HS Tpre. Tpre = Ttxbyteclkhs*value.

**DPHY PHY DATA1 LANE TTAGO**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x0	thspost_high_2bits The value of counter for HS Tpost high 2bits
5:0	RW	0x00	thsttago

**DPHY PHY DATA1 LANE TTASURE**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	thstexit_high_1bit The value of counter for HS Ths-exit high 1bit.
5:0	RW	0x00	thsttasure The value of counter for HS ttasure.

**DPHY PHY DATA1 LANE TTAWAIT**

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	thsttawait The value of counter for HS tta-wait.Tta-wait for turnaround.Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHY PHY DATA2 LANE SWAP**

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	data2_lane_swap Differential signals swap enable. 1'b0:disable 1'b1:enable
3:0	RO	0x0	reserved

**DPHY PHY DATA2 LANE TLPX**

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	hs_tlp The value of counter for HS tlp Time $\text{Time} \geq \text{tlpx} \times \text{tpin\_txbyteclkhs} * (2 + \text{value})$

**DPHY PHY DATA2 LANE HSTXTHSPREPARE**

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	thszero_bit7 The value of counter for HS Ths-zero:HSTXTHZERO[6].

Bit	Attr	Reset Value	Description
6:0	RW	0x00	<p>thsprepare</p> <p>The value of counter for HS Ths-prepare. For clock lane, Ths-prepar(38ns~95ns)</p> <p>For data lane, Ths-prepare(40ns+4UI~85ns+6UI).For clock lane,s_hstxthsprpr[6:0] = 7'b0000011.For data lane, s_hstxthsprpr[6:0] = 7'b0000011.Frequency(1/UI) value(HEX)</p> <p>80-110MHz 7f</p> <p>110-150 MHz 7f</p> <p>150-200 MHz 7f</p> <p>200-250 MHz 7f</p> <p>250-300 MHz 7f</p> <p>300-400 MHz 7e</p> <p>400-500 MHz 70</p> <p>500-600 MHz 60</p> <p>600-700 MHz 40</p> <p>700-800 MHz 02</p> <p>800-1000 MHz 08</p> <p>1000-1200Mhz 03</p> <p>1200-1400Mhz 03</p> <p>1400-1600Mhz 42</p> <p>1600-1800Mhz 47</p> <p>1800-2000Mhz 64</p>

**DPHY PHY DATA2 LANE HSTXTZERO**

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	<p>thszero</p> <p>For clock lane, Ths-prepare+Ths-zero (&gt;=300ns). For data lane, Ths-prepare+Ths-zero (&gt;= 145 ns + 10*UI) = Tpin_txbyteclkhs*(5+value). For clock lane, s_hstxthszero[5:0] = 6'b100000.</p> <p>Frequency(1/UI) Value(HEX)</p> <p>80 -110 MHz 16</p> <p>110-150 MHz 16</p> <p>150-200 MHz 17</p> <p>200-250 MHz 17</p> <p>250-300 MHz 18</p> <p>300-400 MHz 19</p> <p>400-500 MHz 1B</p> <p>500-600 MHz 1D</p> <p>600-700 MHz 1E</p> <p>700-800 MHz 1F</p> <p>800-1000 MHz 20</p> <p>1000-1200Mhz 32</p> <p>1200-1400Mhz 32</p> <p>1400-1600Mhz 36</p> <p>1600-1800Mhz 7a</p> <p>1800-2000Mhz 7a</p>

**DPHY PHY DATA2 LANE HSTXTTRAIL**

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	thstrail The value of counter for HS Ths-trail. For clock lane, Ths-trail ( $\geq 60\text{ns}$ ). For data lane, Ths-trail ( $\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$ ). For clock lane, s_hstxthstrail[6:0] = 7'b0000111. For data lane, s_hstxthstrail[6:0] = 7'b0000111. Frequency(1/UI) Value(HEX) 80 -110 MHz 02 110-150 MHz 02 150-200 MHz 02 200-250 MHz 04 250-300 MHz 04 300-400 MHz 04 400-500 MHz 08 500-600 MHz 10 600-700 MHz 30 700-800 MHz 30 800-1000 MHz 30 1000-1200Mhz 0f 1200-1400Mhz 0f 1400-1600Mhz 0f 1600-1800Mhz 0f 1800-2000Mhz 0b

**DPHY PHY DATA2 LANE HSTXTEXTIT**

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	thsexit The value of counter for HS ths-exit. Ths-exit = Tpin_txbyteclkhs*value

**DPHY PHY DATA2 LANE TDATA2POST**

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thspost The value of counter for HS tclk-post. Tclk-post = Tpin_txbyteclkhs*value.

**DPHY PHY DATA2 LANE LPDT**

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	lpdt_synchronization LPDT TX PPI signals internal synchronization enable. 1'b0:disable 1'b1:enable
1:0	RW	0x0	thstwakeup_bit89 The value[9:8] of counter for HS Twakeup.

**DPHY PHY DATA2 LANE TWAKUP**

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	thstwakup The value[7:0] of counter for HS Twakup. Twakup for ulpm, Twakup = Tpin_sys_clk*value[9:0].

**DPHY PHY DATA2 LANE TPRE**

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thstpre The value of counter for HS Tpre. Tpre = Ttxbyteclkhs*value.

**DPHY PHY DATA2 LANE TTAGO**

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x0	thspost_high_2bits The value of counter for HS Tpost high 2bits
5:0	RW	0x00	thsttago

**DPHY PHY DATA2 LANE TTASURE**

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	thstexit_high_1bit The value of counter for HS Ths-exit high 1bit.
5:0	RW	0x00	thsttasure The value of counter for HS ttasure.

**DPHY PHY DATA2 LANE TTAWAIT**

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	thsttawait The value of counter for HS tta-wait. Tta-wait for turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHY PHY DATA3 LANE SWAP**

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	data3_lane_swap Differential signals swap enable. 1'b0:disable 1'b1:enable
3:0	RO	0x0	reserved

**DPHY PHY DATA3 LANE TLPX**



Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	hs_tlp The value of counter for HS tlp Time $\text{hs\_tlp} = \text{tpin\_txbyteclkhs} * (2 + \text{value})$

### **DPHY PHY DATA3 LANE HSTXTHSPREPRE**

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	thszero_bit The value of counter for HS Ths-zero: HSTXTHZERO[6].
6:0	RW	0x00	thsprepare The value of counter for HS Ths-prepare. For clock lane, Ths-prepar(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI). For clock lane, s_hstxthsprpr[6:0] = 7'b0000011. For data lane, s_hstxthsprpr[6:0] = 7'b0000011. Frequency(1/UI) value(HEX) 80-110MHz 7f 110-150 MHz 7f 150-200 MHz 7f 200-250 MHz 7f 250-300 MHz 7f 300-400 MHz 7e 400-500 MHz 70 500-600 MHz 60 600-700 MHz 40 700-800 MHz 02 800-1000 MHz 08 1000-1200Mhz 03 1200-1400Mhz 03 1400-1600Mhz 42 1600-1800Mhz 47 1800-2000Mhz 64

### **DPHY PHY DATA3 LANE HSTXTZERO**

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	thszero For clock lane, Ths-prepare+Ths-zero ( $\geq 300\text{ns}$ ). For data lane, Ths-prepare+Ths-zero ( $\geq 145\text{ ns} + 10 \cdot \text{UI}$ ) = $T_{\text{pin\_txbyteclkhs}} \cdot (5 + \text{value})$ . For clock lane, $s\_hstxtszero[5:0] = 6'b100000$ . Frequency(1/UI) Value(HEX) 80 -110 MHz 16 110-150 MHz 16 150-200 MHz 17 200-250 MHz 17 250-300 MHz 18 300-400 MHz 19 400-500 MHz 1B 500-600 MHz 1D 600-700 MHz 1E 700-800 MHz 1F 800-1000 MHz 20 1000-1200MHz 32 1200-1400Mhz 32 1400-1600Mhz 36 1600-1800Mhz 7a 1800-2000Mhz 7a

**DPHY PHY DATA3 LANE HSTXTTRAIL**

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	thstrail The value of counter for HS Ths-trail. For clock lane, Ths-trail ( $\geq 60\text{ns}$ ). For data lane, Ths-trail ( $\geq \max(8\text{UI}, 60\text{ns} + 4\text{UI})$ ). For clock lane, $s\_hstxthstrail[6:0] = 7'b0000111$ . For data lane, $s\_hstxthstrail[6:0] = 7'b0000111$ . Frequency(1/UI) Value(HEX) 80 -110 MHz 02 110-150 MHz 02 150-200 MHz 02 200-250 MHz 04 250-300 MHz 04 300-400 MHz 04 400-500 MHz 08 500-600 MHz 10 600-700 MHz 30 700-800 MHz 30 800-1000 MHz 30 1000-1200Mhz 0f 1200-1400Mhz 0f 1400-1600Mhz 0f 1600-1800Mhz 0f 1800-2000Mhz 0b

**DPHY PHY DATA3 LANE HSTXTEXT**

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	thsexit The value of counter for HS ths-exit. Ths-exit = Tpin_txbyteclkhs*value

**DPHY PHY DATA3 LANE TDATA3POST**

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	thspost The value of counter for HS tclk-post. Tclk-post = Tpin_txbyteclkhs*value.

**DPHY PHY DATA3 LANE LPDT**

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	lpdt_synchronization LPDT TX PPI signals internal synchronization enable. 1'b0:disable 1'b1:enable
1:0	RW	0x0	thstwakup_bit89 The value[9:8] of counter for HS Twakup.

**DPHY PHY DATA3 LANE TWAKUP**

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:0	RW	0x00	thstwakup The value[7:0] of counter for HS Twakup. Twakup for ulpm, Twakup = Tpin_sys_clk*value[9:0].

**DPHY PHY DATA3 LANE TPRES**

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3:0	RW	0x0	thstpre The value of counter for HS Tpre. Tpre = Ttxbyteclkhs*value.

**DPHY PHY DATA3 LANE TTAGO**

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x0	thspost_high_2bits The value of counter tor HS Tpost high 2bits
5:0	RW	0x00	thsttago

**DPHY PHY DATA3 LANE TTASURE**

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	thstexit_high_1bit The value of counter for HS Ths-exit high 1bit.
5:0	RW	0x00	thsttasure The value of counter for HS ttasure.

**DPHY PHY DATA3 LANE TTAWAIT**

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	thsttawait The value of counter for HS tta-wait. Tta-wait for turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**6.5 Application Notes****6.5.1 Common Configuration (Default in MIPI Mode)**

Step1: Enable reference clock.

Step2: Wait a period after reference clock have been enabled.

Step3: Send 0xe4 to register MIPI\_DSI\_DPHY\_CTRL\_PWRCTL. Enable PLL and LDO.

Step4: Send 0x7d to register MIPI\_DSI\_DPHY\_CTRL\_LANE\_ENABLE. Enable all lanes on analog part.

Step5: Send 0xe0 to register MIPI\_DSI\_DPHY\_CTRL\_PWRCTL. Reset analog.

Step6: Wait a period after analog has been reset.

Step7: Send 0x1e to register MIPI\_DSI\_DPHY\_CTRL\_DIG\_RST. Reset digital.

Step8: Send 0x1f to register MIPI\_DSI\_DPHY\_CTRL\_DIG\_RST. Reset digital.

Step9: Wait a period until pll locked. Run in MIPI mode.

**6.5.2 Low Power Mode (For DSI Only)**

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

**● Low Power in Steps:**

Step1: Send 0x01 to register MIPI\_DSI\_DPHY\_CTRL\_LANE\_ENABLE. Disable all lanes on analog part.

Step2: Send 0xe3 to register MIPI\_DSI\_DPHY\_CTRL\_PWRCTL. Disable PLL and LDO.

Step3: Wait a period before reference clock have been disabled.

Step4: Disable reference clock.

**● Low Power out Steps:**

Step1: Enable reference clock.

Step2: Wait a period after reference clock have been enabled.

Step3: Send 0xe4 to register MIPI\_DSI\_DPHY\_CTRL\_PWRCTL. Enable PLL and LDO.

Step4: Send 0x7d to register MIPI\_DSI\_DPHY\_CTRL\_LANE\_ENABLE. Enable all lanes on analog part.

Step5: Send 0xe0 to register MIPI\_DSI\_DPHY\_CTRL\_PWRCTL. Reset analog.

Step6: Wait a period after analog has been reset.

Step7: Send 0x1e to register MIPI\_DSI\_DPHY\_CTRL\_DIG\_RST. Reset digital.

Step8: Send 0x1f to register MIPI\_DSI\_DPHY\_CTRL\_DIG\_RST. Reset digital.

Step9: Wait a period before normal transmission.

## Chapter 7 MIPI DSI HOST Controller

### 7.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI HOST Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI HOST Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI DSI HOST Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI DSI HOST Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
  - 16 bits per pixel, configurations 1,2,and 3
  - 18 bits per pixel, configurations 1 and 2
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
  - Up to 2047 vertical active lines
  - Up to 63 vertical back porch lines
  - Up to 63 vertical front porch lines
  - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTP)
- Ultra-Low-Power mode
- Fault recovery schemes

### 7.2 Block Diagram

The following diagram shows the MIPI DSI HOST Controller architecture.

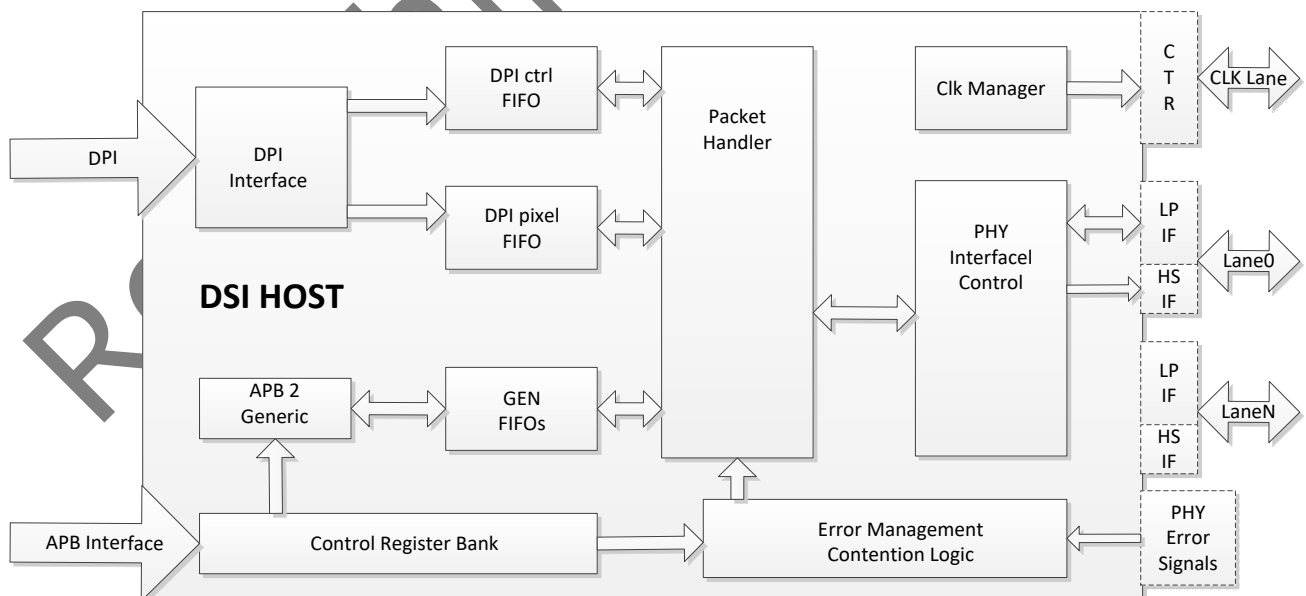


Fig. 7-1 MIPI DSI HOST Controller Architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video

packets, then in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI DSI HOST Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.

The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.

The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.

The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOs: Command FIFO, Write payload FIFO, Read payload FIFO.

The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

## 7.3 Function Description

### 7.3.1 DPI Interface Function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands]. To transfer additional commands (for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpixdata bus. The following table shows the interface pixel color coding.

Table 7-1 Color Table

Signal Line	16-bit			18-bit		24bit
Config	Config1	Config2	Config3	Config1	Config2	Config1
Dpdata23	Not used	Not used	Not used	Not used	Not used	R7
Dpdata22	Not used	Not used	Not used	Not used	Not used	R6
Dpdata21	Not used	Not used	R4	Not used	R5	R5
Dpdata20	Not used	R4	R3	Not used	R4	R4
Dpdata19	Not used	R3	R2	Not used	R3	R3
Dpdata18	Not used	R2	R1	Not used	R2	R2
Dpdata17	Not used	R1	R0	R5	R1	R1
Dpdata16	Not used	R0	Not used	R4	R0	R0
Dpdata15	R4	Not used	Not used	R3	Not used	G7
Dpdata14	G3	Not used	Not used	G2	Not used	G6
Dpdata13	G2	G5	G5	G1	G5	G5
Dpdata12	G1	G4	G4	G0	G4	G4
Dpdata11	G0	G3	G3	G5	G3	G3
Dpdata10	G5	G2	G2	G4	G2	G2
Dpdata9	G4	G1	G1	G3	G1	G1
Dpdata8	G3	G0	G0	G2	G0	G0
Dpdata7	G2	Not used	Not used	G1	Not used	B7

Signal Line	16-bit			18-bit		24bit
Config	Config1	Config2	Config3	Config1	Config2	Config1
Dpdata6	G1	Not used	Not used	G0	Not used	B6
Dpdata5	G0	Not used	B4	B5	B5	B5
Dpdata4	B4	B4	B3	B4	B4	B4
Dpdata3	B3	B3	B2	B3	B3	B3
Dpdata2	B2	B2	B1	B2	B2	B2
Dpdata1	B1	B1	B0	B1	B1	B1
Dpdata0	B0	B0	Not used	B0	B0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows: Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI DSI HOST Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.

If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

### 7.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI DSI HOST Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN\_PLD\_DATA register has two distinct functions based on the operation.

Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN\_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN\_PLD\_DATA register.

The valid packets available to be transmitted through the Generic interface are as follows:

- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Generic Write Short Packet 0 Parameter
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameter
- DCS Write Short Packet 1 Parameter
- DCS Write Short Packet 0 Parameter
- DCS Write Long Packet

A set of bits in the CMD\_PKT\_STATUS register report the status of the FIFOs associated with APB interface support.

Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these modes are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.

The transfer of packets through the APB bus is based on the following conditions:

The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.

The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bit rate achievable by the APB interface.

The DSI link bit rate when using solely APB is equal to (APB clock frequency) \* 16 Mbps. The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.

To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI DSI HOST Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.

The memory write commands require maximum throughput from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN\_PLD\_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least significant byte position of the APB data bus. After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be organized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams. In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

### 7.3.3 Transmission of Commands in Video Mode

The MIPI DSI HOST Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

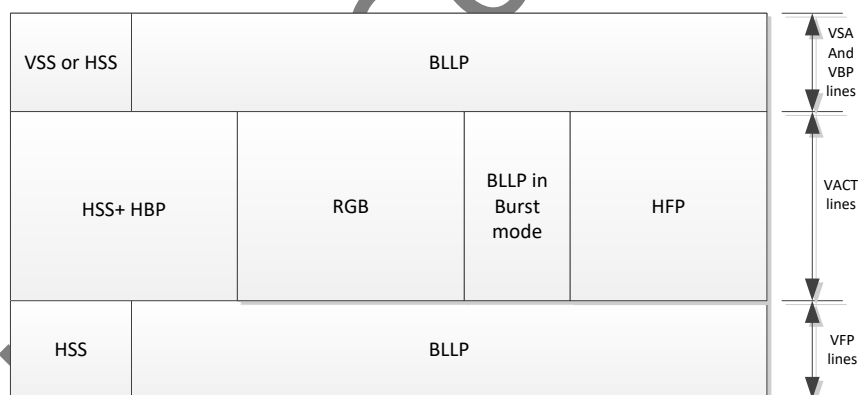


Fig. 7-2 Command Transmission Periods Within The Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Vertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.

The MIPI DSI HOST Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) \* (number of lines - 1) shorter than tL.

The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down



Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the `lpcmden` bit of the `VID_MODE_CFG` register is 1, these commands are sent in LP mode. In LP mode, the `outvact_lpcmd_time` field of the `LP_CMD_TIM` register is used to determine if these commands can be transmitted. It is assumed that `outvact_lpcmd_time` is greater than or equal to 4 bytes (number of bytes in a short packet), because the DSI HOST does not transmit these commands on the last line.

If the `frame_BTA_ack` field is set in the `VID_MODE_CFG` register, a BTA is generated by DSI HOST after the last line of a frame. This may coincide with a write command or a read command. In either case, the `edpihalt` signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).

If the `lpcmden` bit of the `VID_MODE_CFG` register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch (VFP) regions.

The `outvact_lpcmd_time` field of the `LP_CMD_TIM` register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP

$$\text{Outvact\_lpcmd\_time} = (\text{tL} - (\text{Time to transmit HSS and HSE frames} + \text{tHSA} + \text{Time to enter and leave LP mode} + \text{Time to send the D-PHY LPDT command})) / \text{escape clock period} / 8 / 2$$

Where, `tL`=Line time, and `tHSA`=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses).

In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.

The `outvact_lpcmd_time` field can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field.

This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.

Consider an example with 12.6  $\mu\text{s}$  per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:

- Sync pulses are not being transmitted
- Two lane byte clock ticks are required to transmit a short packet

$$\text{phy\_lp2hs\_time} = 16$$

$$\text{phy\_lp2p\_time} = 20$$

In this example, a 11-byte command can be transmitted as follows:

$$\text{outvact\_lpcmd\_time} = 11 \text{ bytes}$$

The `invact_lpcmd_time` field of the `LP_CMD_TIM` register indicates the time available (in bytes) to transmit a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:

$$\text{Invact\_lpcmd\_time} = ((\text{tHFP} - \text{Time to enter and leave low-power mode} + \text{Blanking period before the HFP when in Burst mode} - \text{Time to send the D-PHY LPDT command}) / \text{escape clock period}) / 8.$$
 Where,

$$\text{tHFP} = \text{line\_time} - \text{tHSA} - \text{tHBP} - \text{tHACT}$$

$$\text{tHACT} = \text{vid\_pkt\_size} * \text{bits\_per\_pixel} * \text{lane\_byte\_clock\_period} / \text{num\_lanes}$$

The `invact_lpcmd_time` field can be compared directly with the size of the command to be transmitted to determine if there is time to transmit the command.

Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The `tL` in this case is 12.6  $\mu\text{s}$ . With a lane byte clock of 100 MHz, 1260 clock ticks are available to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6  $\mu\text{s}$ ) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3  $\mu\text{s}$  is available for HFP and the escape clock is 15 MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.

A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore,

in this example, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:  
The controller is not in Burst mode:

$$phy\_lp2hs\_time = 16$$

In this example invact\_lpcmd\_time is calculated as follows:

$$Invact\_lpcmd\_time = (2.3\mu s - (16 \times 10\text{ ns}) - (20 \times 10\text{ ns}) - (8 \times 66\text{ ns})) / 66\text{ ns} / 8 = 2\text{ bytes}$$

The outvact\_lpcmd\_time and invact\_lpcmd\_time fields allow a simple comparison to determine if a command can be transmitted in any of the BLLP periods.

Following figure illustrates the meaning of invact\_lpcmd\_time and outvact\_lpcmd\_time, matching them with the shaded areas and the VACT region.

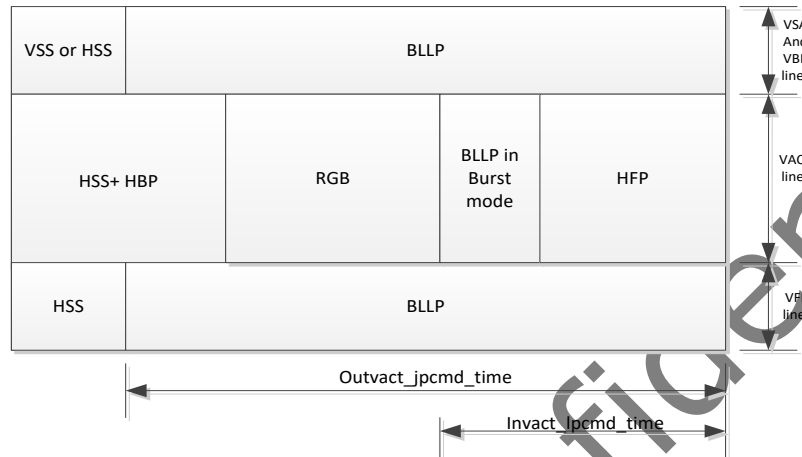


Fig. 7-3 Location In The Image Area

If the lpcmden bit of the VID\_MODE\_CFG register is 0, the commands are sent in high\_speed in Video Mode. In this case, the DSI HOST automatically determines the area where each command can be sent and no programming or calculation is required. On read command Transmission, the max\_rd\_time field of the PHY\_TMR\_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.

The maximum time required to perform a read command in Lane byte clock cycles (max\_rd\_time) = Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.

The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral; not the escape clock of the host. The max\_rd\_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.

In high-speed mode (lpcmden=0), max\_rd\_time is calculated as follows:

$$\text{max\_rd\_time} = \text{phy\_hs2lp\_time} + \text{Time to return the read data packet from the peripheral device} + \text{phy\_hs2hs\_time}$$

In low-power mode (lpcmden = 1), max\_rd\_time is calculated as follows:

$$\text{max\_rd\_time} = \text{phy\_hs2lp\_time} + \text{LPDT command time} + \text{Read command time in LP mode} + \text{Time to return the data read from the peripheral device} + \text{phy\_lp2hs\_time}$$

Where,

$$\text{LPDT command time} = (8 \times \text{Host escape clock period}) / \text{Lane byte clock period}$$

$$\text{Read command time in LP mode} = (32 \times \text{host escape clock period}) / \text{lane byte clock period}$$

It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max\_rd\_time \* Lane byte clock period is less than outvact\_lpcmd\_time \* 8 \* Escape clock period of the host.

Otherwise, the read commands are serviced on the last line of a frame and the edpiahalt signal may be asserted. If it is necessary to read a large number of parameters (>16), increase the max\_rd\_time while the read command is being executed. When the read has completed, decrease the max\_rd\_time to a lower value.

## 7.4 Register Description

### 7.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 7.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
<u>MIPS_DSI_VERSION</u>	0x0000	W	0x3133302A	Version of DSI host controller only read, Value after Reset : 0x3133_302A
<u>MIPS_DSI_PWR_UP</u>	0x0004	W	0x00000000	Core power-up
<u>MIPS_DSI_CLKMGR_CFG</u>	0x0008	W	0x00000000	Configuration of the internal clock dividers
<u>MIPS_DSI_DPI_VCID</u>	0x000C	W	0x00000000	DPI virtual channel id
<u>MIPS_DSI_DPI_COLOR_CODING</u>	0x0010	W	0x00000000	DPI color coding
<u>MIPS_DSI_DPI_CFG_POL</u>	0x0014	W	0x00000000	DPI polarity configuration
<u>MIPS_DSI_DPI_LP_CMD_TIM</u>	0x0018	W	0x00000000	Low-power command timing configuration
<u>MIPS_DSI_DBI_VCID</u>	0x001C	W	0x00000000	DBI virtual channel id
<u>MIPS_DSI_DBI_CFG</u>	0x0020	W	0x00000000	DBI interface configuration
<u>MIPS_DSI_DBI_PARTITIONING_EN</u>	0x0024	W	0x00000000	DBI partitioning enable
<u>MIPS_DSI_DBI_CMD_SIZE</u>	0x0028	W	0x00000000	DBI command size configuration
<u>MIPS_DSI_PCKHDL_CFG</u>	0x002C	W	0x00000000	Packet handler virtual channel id
<u>MIPS_DSI_GEN_VCID</u>	0x0030	W	0x00000000	This register configures the virtual channel id of the read responses to store and return to the Generic interface
<u>MIPS_DSI_MODE_CFG</u>	0x0034	W	0x00000001	This register configures the mode of operation - Video mode or Command mode
<u>MIPS_DSI_VID_MODE_CFG</u>	0x0038	W	0x00000000	This register configures several aspects of the Video mode operation such as the transmission mode, switching to low-power in the middle of a frame, enabling acknowledge, and whether to send the commands in low-power.
<u>MIPS_DSI_VID_PKT_SIZE</u>	0x003C	W	0x00000000	This register configures the video packet size
<u>MIPS_DSI_VID_NUM_CHUNKS</u>	0x0040	W	0x00000000	This register configures the number of chunks to use. The data in each chunk has the size provided by VID_PKT_SIZE
<u>MIPS_DSI_VID_NULL_SIZE</u>	0x0044	W	0x00000000	This register configures the size of null packets
<u>MIPS_DSI_VID_HSA_TIME</u>	0x0048	W	0x00000000	This register configures the video Horizontal Synchronism Active (HSA) time.
<u>MIPS_DSI_VID_HBP_TIME</u>	0x004C	W	0x00000000	This register configures the video Horizontal Back Porch (HBP) time.
<u>MIPS_DSI_VID_HLINE_TIME</u>	0x0050	W	0x00000000	This register configures the overall time for each video line.

Name	Offset	Size	Reset Value	Description
<u>MIPS DSI VID VSA LINE S</u>	0x0054	W	0x00000000	This register configures the Vertical Synchronism Active (VSA) period.
<u>MIPS DSI VID VBP LINE S</u>	0x0058	W	0x00000000	This register configures the Vertical Back Porch (VBP) period.
<u>MIPS DSI VID VFP LINE S</u>	0x005C	W	0x00000000	This register configures the Vertical Front Porch (VFP) period.
<u>MIPS DSI VID VACTIVE LINES</u>	0x0060	W	0x00000000	This register configures the vertical resolution of the video
<u>MIPS DSI EDPI CMD SI ZE</u>	0x0064	W	0x00000000	This register configures the size of the eDPI packets.
<u>MIPS DSI CMD MODE C FG</u>	0x0068	W	0x00000000	This register configures several aspects of the command mode operation, tearing effect, acknowledge for each packet, and the speed mode to transmit each data type related to commands.
<u>MIPS DSI GEN HDR</u>	0x006C	W	0x00000000	This register sets the header for new packets sent using the Generic interface.
<u>MIPS DSI GEN PLD DAT A</u>	0x0070	W	0x00000000	This register sets the payload for the packets sent using the Generic interface and, when read, returns the contents of the read responses from the peripheral.
<u>MIPS DSI CMD PKT STA TUS</u>	0x0074	W	0x00001515	This register contains information about the status of the FIFOs related to the DBI and the Generic interfaces.
<u>MIPS DSI TO CNT CFG</u>	0x0078	W	0x00000000	This register configures the counters that trigger the timeout errors. These are used to warn the system about a failure, through an interrupt, and restart the core in case of unexpected situations that cause deadlock conditions.
<u>MIPS DSI HS RD TO CN I</u>	0x007C	W	0x00000000	This register configures the Peripheral Response timeout after high-speed read operations
<u>MIPS DSI LP RD TO CN I</u>	0x0080	W	0x00000000	This register configures the Peripheral Response timeout after the low-power read operations.
<u>MIPS DSI HS WR TO C NT</u>	0x0084	W	0x00000000	This register configures the Peripheral Response timeout after the high-speed write operations.
<u>MIPS DSI LP WR TO CN I</u>	0x0088	W	0x00000000	This register configures the Peripheral Response timeout after the low-power write operations
<u>MIPS DSI BTA TO CNT</u>	0x008C	W	0x00000000	Register0012 Description
<u>MIPS DSI LPCLK CTRL</u>	0x0094	W	0x00000000	Register0014 Description

Name	Offset	Size	Reset Value	Description
<u>MIPS_DSI_PHY_TMR_LPC_LK_CFG</u>	0x0098	W	0x00000000	This register sets the time that the mipi_dsi_host assumes in calculations for the clock lane to switch between high-speed and low-power
<u>MIPS_DSI_PHY_TMR_CFG</u>	0x009C	W	0x00000000	This register sets the time that the mipi_dsi_host assumes in calculations for the data lanes to switch between high-speed and low-power.
<u>MIPS_DSI_PHY_RSTZ</u>	0x00A0	W	0x00000000	This register controls the resets and the PLL of the D-PHY.
<u>MIPS_DSI_PHY_IF_CFG</u>	0x00A4	W	0x00000000	This register configures the number of active lanes and the minimum time to remain in the Stop state.
<u>MIPS_DSI_PHY_ULPS_CTL</u>	0x00A8	W	0x00000000	Register0000 Description
<u>MIPS_DSI_PHY_TX_TRIGGERS</u>	0x00AC	W	0x00000000	This register configures the signals that activate the triggers in the D-PHY.
<u>MIPS_DSI_PHY_STATUS</u>	0x00B0	W	0x00001528	Register0002 Description
<u>MIPS_DSI_PHY_TST_CTL0</u>	0x00B4	W	0x00000001	This register controls the clock and the clear signals of the D-PHY vendor specific interface.
<u>MIPS_DSI_PHY_TST_CTL1</u>	0x00B8	W	0x00000000	This register controls the data and the enable pins of the D-PHY vendor specific interface
<u>MIPS_DSI_INT_ST0</u>	0x00BC	W	0x00000000	Register0001 Description
<u>MIPS_DSI_INT_ST1</u>	0x00C0	W	0x00000000	This register contains the status of the interrupt sources related to timeouts, ECC, CRC, packet size, EoTp, Generic, and DBI interfaces.
<u>MIPS_DSI_INT_MSK0</u>	0x00C4	W	0x00000000	Register0003 Description
<u>MIPS_DSI_INT_MSK1</u>	0x00C8	W	0x00000000	This register configures the masks for the sources of the interrupts that affect the INT_ST1 register.
<u>MIPS_DSI_INT_FORCE0</u>	0x00D8	W	0x00000000	This register force interrupts that affects the INT_ST0 register.
<u>MIPS_DSI_INT_FORCE1</u>	0x00DC	W	0x00000000	Register0000 Description
<u>MIPS_DSI_VID_SHADOW_CTRL</u>	0x0100	W	0x00000000	Register0001 Description
<u>MIPS_DSI_DPI_VCID_ACT</u>	0x010C	W	0x00000000	This register configures the virtual channel id for the DPI traffic.
<u>MIPS_DSI_DPI_COLOR_CODING_ACT</u>	0x0110	W	0x00000000	This register configures DPI color coding.
<u>MIPS_DSI_DPI_LP_CMD_TIM_ACT</u>	0x0118	W	0x00000000	Register0000 Description

Name	Offset	Size	Reset Value	Description
<u>MIPS_DSI_VID_MODE_CFG_ACT</u>	0x0138	W	0x00000000	This register configures several aspects of Video mode operation, the transmission mode, switching to low-power in the middle of a frame, enabling acknowledge and whether to send commands in low-power.
<u>MIPS_DSI_VID_PKT_SIZE_ACT</u>	0x013C	W	0x00000000	This register configures the video packet size.
<u>MIPS_DSI_VID_NUM_CHUNKS_ACT</u>	0x0140	W	0x00000000	This register configures the number of chunks to use. The data in each chunk has the size provided by VID_PKT_SIZE.
<u>MIPS_DSI_VID_NULL_SIZE_ACT</u>	0x0144	W	0x00000000	This register configures the size of null packets.
<u>MIPS_DSI_VID_HSA_TIME_ACT</u>	0x0148	W	0x00000000	This register configures the video HSA time.
<u>MIPS_DSI_VID_HBP_TIME_ACT</u>	0x014C	W	0x00000000	This register configures the video HBP time.
<u>MIPS_DSI_VID_HLINE_TIME_ACT</u>	0x0150	W	0x00000000	This register configures the overall time for each video line.
<u>MIPS_DSI_VID_VSA_LINES_ACT</u>	0x0154	W	0x00000000	This register configures the VSA period.
<u>MIPS_DSI_VID_VBP_LINES_ACT</u>	0x0158	W	0x00000000	This register configures the VBP period.
<u>MIPS_DSI_VID_VFP_LINES_ACT</u>	0x015C	W	0x00000000	This register configures the VFP period.
<u>MIPS_DSI_VID_VACTIVE_LINES_ACT</u>	0x0160	W	0x00000000	This register configures the vertical resolution of video.

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 7.4.3 Detail Registers Description

#### **MIPS\_DSI\_VERSION**

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x3133302a	VERSION This field indicates the version of the mipi_dsi_host.

#### **MIPS\_DSI\_PWR\_UP**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shutdownz This bit configures the core either to power up or to reset. shutdownz is the soft reset register. Its default value is 0. After the core configuration, to enable the mipi_dsi_host, set this register to 1. 1'b0: Reset 1'b1: Power-up

#### **MIPS\_DSI\_CLKMGR\_CFG**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	to_clk_division This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.
7:0	RW	0x00	tx_esc_clk_division This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation. 7'h0,7'h1:stop the TX_ESC clock generation.

**MIPS DSI DPI VCID**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets.

**MIPS DSI DPI COLOR CODING**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	loosely18_en 1'b0: disable loosely packed variant to 18-bit configurations. 1'b1: enable loosely packed variant to 18-bit configurations.
7:4	RO	0x0	reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4'b0000:16-bit configuration 1 4'b0001:16-bit configuration 2 4'b0010:16-bit configuration 3 4'b0011:18-bit configuration 1 4'b0100:18-bit configuration 2 4'b0101:24-bit 4'b0110:20-bit YCbCr 4:2:2 loosely packed 4'b0111:24-bit YCbCr 4:2:2 4'b1000:16-bit YCbCr 4:2:2 4'b1001:30-bit 4'b1010:36-bit 4'b1011-1111:12-bit TCbCr 4:2:0 Note: If the eDPI interface is chosen and currently works in the Command mode (cmd_video_mode = 1), then 0110-1111: 24-bit

**MIPS DSI DPI CFG POL**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4	RW	0x0	colorm_active_low 1'b0:disable the color mode pin as active low. 1'b1:enable the color mode pin as active low.
3	RW	0x0	shutd_active_low 1'b0:disable the shutdown pin as active low. 1'b1:enable the shutdown pin as active low.

Bit	Attr	Reset Value	Description
2	RW	0x0	hsync_active_low 1'b0:disable the horizontal synchronism pin as active low. 1'b1:enable the horizontal synchronism pin as active low.
1	RW	0x0	vsync_active_low 1'b0:disable the vertical synchronism pin as active low. 1'b1:enable the vertical synchronism pin as active low.
0	RW	0x0	Dataen_active_low 1'b0:disable the data enable pin as active low. 1'b1:enable the data enable pin as active low.

**MIPS DSI DPI LP CMD TIM**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	outvact_Ipcmd_time This field is used for the transmission of commands in low-power mode It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions.
15:8	RO	0x00	reserved
7:0	RW	0x00	invact_Ipcmd_time This field is used for the transmission of commands in low-power mode . It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region.

**MIPS DSI DBI VCID**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	dbi_vcid This field configures the virtual channel id that is indexed to the DCS packets from DBI.

**MIPS DSI DBI CFG**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	lut_size_conf This field configures the size used to transport the write Lut commands as follows: 2'b00: 16-bit color display 2'b01: 18-bit color display 2'b10: 24-bit color display 2'b11: 16-bit color display
15:12	RO	0x0	reserved



Bit	Attr	Reset Value	Description
11:8	RW	0x0	out_dbi_conf This field configures the DBI output pixel data as follows: 4'b0000: 8-bit 8 bpp 4'b0001: 8-bit 12 bpp 4'b0010: 8-bit 16 bpp 4'b0011: 8-bit 18 bpp 4'b0100: 8-bit 24 bpp 4'b0101: 9-bit 18 bpp 4'b0110: 16-bit 8 bpp 4'b0111: 16-bit 12 bpp 4'b1000: 16-bit 16 bpp 4'b1001: 16-bit 18 bpp, option 1 4'b1010: 16-bit 18 bpp, option 2 4'b1011: 16-bit 24 bpp, option 1 4'b1100: 16-bit 24 bpp, option 2
7:4	RO	0x0	reserved
3:0	RW	0x0	in_dbi_conf This field configures the DBI input pixel data as follows: 4'b0000: 8-bit 8 bpp 4'b0001: 8-bit 12 bpp 4'b0010: 8-bit 16 bpp 4'b0011: 8-bit 18 bpp 4'b0100: 8-bit 24 bpp 4'b0101: 9-bit 18 bpp 4'b0110: 16-bit 8 bpp 4'b0111: 16-bit 12 bpp 4'b1000: 16-bit 16 bpp 4'b1001: 16-bit 18 bpp, option 1 4'b1010: 16-bit 18 bpp, option 2 4'b1011: 16-bit 24 bpp, option 1 4'b1100: 16-bit 24 bpp, option 2

**MIPS DSI DBI PARTITIONING EN**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	partitioning_en 1'b0: partitioning is automatically performed in the mipi_dsi_host. 1'b1: the use of write_memory_continue input commands.

**MIPS DSI DBI CMDSIZE**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	allowed_cmd_size This field configures the maximum allowed size for a DCS write memory command. This field is used to partition a write memory command. This field is used to partition a write memory command into one write_memory_start and a variable number of write_memory_continue commands. It is only used if the partitioning_en bit of the DBI_CFG register is disabled. The size of the DSI packet payload is the actual payload size minus 1, because the DCS command is in the DSI packet payload.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	wr_cmd_size This field configures the size of the DCS write memory commands. The size of DSI packet payload is the actual payload size minus 1, because the DCS command is in the DSI packet payload.

**MIPS DSI PCKHDL CFG**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4	RW	0x0	crc_rx_en 1'b0:disable CRC reception and error reporting. 1'b1:enable CRC reception and error reporting.
3	RW	0x0	ecc_rx_en 1'b0:disable the ECC reception,error correction,and reporting. 1'b1:enable the ECC reception,error correction,and reporting.
2	RW	0x0	bta_en 1'b0:disable the Bus Turn-Around(BTA) request. 1'b1:enable the Bus Turn-Around(BTA) request.
1	RW	0x0	eotp_rx_en 1'b0:disable the EoTp reception. 1'b1:enable the EoTp reception.
0	RW	0x0	eotp_tx_en 1'b0:disable the EoTp transmission. 1'b1:enable the EoTp transmission.

**MIPS DSI GEN VCID**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	gen_vcid_rx This field indicates the Generic interface read-back virtual channel Identification.

**MIPS DSI MODE CFG**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	cmd_video_mode This bit configures the operation mode: 1'b0:Vodeo mode 1'b1:Command mode

**MIPS DSI VID MODE CFG**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	vgp_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	vgp_mode This field is to select the pattern: 0: Color bar (horizontal or vertical). 1: BER pattern (vertical only).
19:17	RO	0x0	reserved
16	RW	0x0	vgp_en 1'b0: disable the video mode pattern generator. 1'b1: enables the video mode pattern generator.
15	RW	0x0	Ip_cmd_en 1'b0: disable the command transmission only in lowpower mode. 1'b1: enables the command transmission only in lowpower mode.
14	RW	0x0	frame_bta_ack_en 1'b0: disable the request for an acknowledge response at the end of a frame. 1'b1: enables the request for an acknowledge response at the end of a frame.
13	RW	0x0	Ip_hfp_en 1'b0: disable the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows. 1'b1: enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows.
12	RW	0x0	Ip_hbp_en 1'b0: disable the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows. 1'b1: enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows.
11	RW	0x0	Ip_vact_en 1'b0: disable the return to low-power inside the Vertical Active (VACT) period when timing allows. 1'b1: enables the return to low-power inside the Vertical Active (VACT) period when timing allows.
10	RW	0x0	Ip_vfp_en 1'b0: disable the return to low-power inside the Vertical Front Porch (VFP) period when timing allows. 1'b1: enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows.
9	RW	0x0	Ip_vbp_en 1'b0: disable the return to low-power inside the Vertical Back Porch (VBP) period when timing allows. 1'b1: enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows.
8	RW	0x0	Ip_vsa_en 1'b0: disable the return to low-power inside the Vertical Sync Time (VSA) period when timing allows. 1'b1: enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows.
7:2	RO	0x00	reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 11: Burst mode

**MIPS DSI VID PKT SIZE**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification.

**MIPS DSI VID NUM CHUNKS**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line.

**MIPS DSI VID NULL SIZE**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets.

**MIPS DSI VID HSA TIME**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

**MIPS DSI VID HBP TIME**

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	vid_hbp_time This field configures the Horizontal Back Porch period in lane byte clock cycles.

**MIPS DSI VID HLINE TIME**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles.

**MIPS DSI VID VSA LINES**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines.

**MIPS DSI VID VBP LINES**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vbp_line This field configures the Vertical Back Porch period measured in number of horizontal lines.

**MIPS DSI VID VFP LINES**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines.

**MIPS DSI VID VACTIVE LINES**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x000000	reserved
13:0	RW	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines.

**MIPS DSI EDPI CMD SIZE**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled.

**MIPS DSI CMD MODE CFG**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 1'b0: High-speed 1'b1: Low-power
23:20	RO	0x0	reserved
19	RW	0x0	dsc_lw_tx This bit configures the DCS long write packet command transmission type: 1'b0: High-speed 1'b1: Low-powe

Bit	Attr	Reset Value	Description
18	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
17	RW	0x0	dsc_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
16	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
15	RO	0x0	reserved
14	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
13	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
12	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
11	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
10	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
9	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power

Bit	Attr	Reset Value	Description
8	RW	0x0	gen_sw_op_tx This bit configures the Generic short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
7:2	RO	0x00	reserved
1	RW	0x0	ack_rqst_en 1'b0: disable the acknowledge request after each packet transmission. 1'b1: enables the acknowledge request after each packet transmission.
0	RW	0x0	tear_fx_en 1'b0: disable the tearing effect acknowledge request. 1'b1: enable the tearing effect acknowledge request.

**MIPS DSI GEN HDR**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	gem_wc_msbyte This field configures the most significant byte of the header packet's word count for long packets or data 1 for short packets.
15:8	RW	0x00	gen_wc_lsbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets.
7:6	RW	0x0	gen_vc This field configures the virtual channel id of the header packet.
5:0	RW	0x00	gen_dt This field configures the packet data type of the header packet.

**MIPS DSI GEN PLD DATA**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload.
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload.
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload.
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload.

**MIPS DSI CMD PKT STATUS**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	dbi_rd_cmd_busy 1'b0: This bit is cleared when the entire response is stored in the FIFO. 1'b1: This bit is set when a read command is issued.

Bit	Attr	Reset Value	Description
13	RO	0x0	dbi_pld_r_full 1'b0: indicates the not full status of the DBI read payload FIFO. 1'b1: indicates the full status of the DBI read payload FIFO.
12	RO	0x1	dbi_pld_r_empty 1'b0: indicates the not empty status of the DBI read payload FIFO. 1'b1: indicates the empty status of the DBI read payload FIFO.
11	RO	0x0	dbi_pld_w_full 1'b0: indicates the not full status of the DBI write payload FIFO. 1'b1: indicates the full status of the DBI write payload FIFO.
10	RO	0x1	dbi_pld_w_empty 1'b0: indicates the not full status of the DBI command FIFO. 1'b1: indicates the full status of the DBI command FIFO.
9	RO	0x0	dbi_cmd_full 1'b0: indicates the not full status of the DBI command FIFO. 1'b1: indicates the full status of the DBI command FIFO.
8	RO	0x1	dbi_cmd_empty 1'b0: indicates the not empty status of the DBI command FIFO. 1'b1: indicates the empty status of the DBI command FIFO.
7	RO	0x0	reserved
6	RO	0x0	gen_rd_cmd_busy 1'b0: This bit is cleared when the entire response is stored in the FIFO. 1'b1: This bit is set when a read command is issued.
5	RO	0x0	gen_pld_r_full 1'b0: indicates the not full status of the generic read payload FIFO. 1'b1: indicates the full status of the generic read payload FIFO.
4	RO	0x1	gen_pld_r_empty 1'b0: indicates the not empty status of the generic read payload FIFO. 1'b1: indicates the empty status of the generic read payload FIFO.
3	RO	0x0	gen_pld_w_full 1'b0: indicates the not full status of the generic write payload FIFO. 1'b1: indicates the full status of the generic write payload FIFO.



Bit	Attr	Reset Value	Description
2	RO	0x1	gen_pld_w_empty 1'b0: indicates the not empty status of the generic write payload FIFO. 1'b1: indicates the empty status of the generic write payload FIFO.
1	RO	0x0	gen_cmd_full 1'b0: indicates the not full status of the generic command FIFO. 1'b1: indicates the full status of the generic command FIFO.
0	RO	0x1	gen_cmd_empty 1'b0: indicates the not empty status of the generic command FIFO. 1'b1: indicates the empty status of the generic command FIFO.

**MIPS DSI TO CNT CFG**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed Transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: $\text{hstx\_to\_cnt} * \text{lanebyteclkperiod} * \text{TO\_CLK\_DIVISION} \geq \text{the time of one FRAME data transmission} * (1 + 10\%)$ In burst mode, RGB pixel packets are time-compressed, leaving more time during a scan line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time, from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: $\text{hstx\_to\_cnt} * \text{lanebyteclkperiod} * \text{TO\_CLK\_DIVISION} \geq \text{the time of one LINE data transmission} * (1 + 10\%)$
15:0	RW	0x0000	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles).

**MIPS DSI HS RD TO CNT**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	hs_rd_to_cnt This field sets a period for which the mipi_dsi_host keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

**MIPS DSI LP RD TO CNT**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	lp_rd_to_cnt This field sets a period for which the mipi_dsi_host keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

**MIPS DSI HS WR TO CNT**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	presp_to_mode 1'b0:disable the peripheral response timeout. 1'b1:enable the peripheral response timeout.
23:16	RO	0x00	reserved
15:0	RW	0x0000	hs_wr_to_cnt This field sets a period for which the mipi_dsi_host keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

**MIPS DSI LP WR TO CNT**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	lp_wr_to_cnt This field sets a period for which the mipi_dsi_host keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

**MIPS DSI BTA TO CNT**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	bta_to_cnt This field sets a period for which the mipi_dsi_host keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

**MIPS DSI LPCLK CTRL**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	auto_clklane_ctrl 1'b0: disable the automatic mechanism to stop providing clock. 1'b1: enable automatic mechanism can stop providing clock in the clock lane when time allows.
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal.

**MIPS DSI PHY TMR LPCLK CFG**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	phy_clkhs2lp_time This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles.
15:10	RO	0x00	reserved
9:0	RW	0x000	phy_clklp2hs_time This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles.

**MIPS DSI PHY TMR CFG**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles.
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles.
15	RO	0x0	reserved
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress.

**MIPS DSI PHY RSTZ**

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3	RW	0x0	phy_forcepll 1'b0: disable the D-PHY PLL. 1'b1: when the D-PHY is in ULPS, enable the D-PHY PLL.
2	RW	0x0	phy_enableclk 1'b0: disable the D-PHY Clock lane module. 1'b1: enable the D-PHY Clock lane module.
1	RW	0x0	phy_rstz 1'b0: enable the digital section of the D-PHY in the reset state. 1'b1: disable the digital section of the D-PHY in the reset state.

Bit	Attr	Reset Value	Description
0	RW	0x0	phy_shutdownz 1'b0: enable D-PHY Clock Lane module. 1'b1: disable D-PHY Clock Lane module.

**MIPS DSI PHY IF CFG**

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state.
7:2	RO	0x00	reserved
1:0	RW	0x0	n_lanes This field configures the number of active data lanes: 2'b00: One data lane (lane 0). 2'b01: Two data lanes (lanes 0 and 1). 2'b10: Three data lanes (lanes 0, 1, and 2). 2'b11: Four data lanes (lanes 0, 1, 2, and 3).

**MIPS DSI PHY ULPS CTRL**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3	RW	0x0	phy_txexitulpslan ULPS mode Exit on all active data lanes.
2	RW	0x0	phy_txrequilpslan ULPS mode Request on all active data lanes.
1	RW	0x0	phy_txexitulpsclk ULPS mode Exit on clock lane.
0	RW	0x0	phy_txrequilpsclk ULPS mode Request on clock lane.

**MIPS DSI PHY TX TRIGGERS**

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3:0	RW	0x0	phy_tx_triggers This field controls the trigger transmissions.

**MIPS DSI PHY STATUS**

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:13	RO	0x000000	reserved
12	RO	0x1	phy_ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal.
11	RO	0x0	phy_stopstatelane This bit indicates the status of phystopstate3lane D-PHY signal.
10	RO	0x1	phy_ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal.

Bit	Attr	Reset Value	Description
9	RO	0x0	phy_stopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal.
8	RO	0x1	phy_ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal.
7	RO	0x0	phy_stopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal.
6	RO	0x0	phy_rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal.
5	RO	0x1	phy_ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal.
4	RO	0x0	phy_stopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal.
3	RO	0x1	phy_ulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal.
2	RO	0x0	hpy_stopstatecklane This bit indicates the status of phystopstatecklane D-PHY signal.
1	RO	0x0	phy_direction This bit indicates the status of phydirection D-PHY signal.
0	RO	0x0	phy_lock This bit indicates the status of phylock D-PHY signal.

**MIPS DSI PHY TST CTRL0**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	phy_testclr This bit is used to clock the TESTDIN bus into the D-PHY.
0	RW	0x1	phy_testclk 1'b0: disable PHY test interface clear. 1'b1: enable PHY test interface clear.

**MIPS DSI PHY TST CTRL1**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	phy_testen PHY test interface operation selector: 1'b1: The address write operation is set on the falling edge of the testclk signal. 1'b0: The data write operation is set on the rising edge of the testclk signal.
15:8	RO	0x00	pht_testdout PHY output 8-bit data bus for read-back and internal probing functionalities.
7:0	RW	0x00	phy_testdin PHY test interface input 8-bit data bus for internal register programming and test functionalities access.

**MIPS DSI INT ST0**

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RO	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.
19	RO	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.
18	RO	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0.
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report.
14	RO	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report.
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report.
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report.
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.
7	RO	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report.
5	RO	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report.
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report.
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.

Bit	Attr	Reset Value	Description
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report.
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report.
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report.

**MIPS DSI INT ST1**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	dbi_illegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission.
16	RO	0x0	dbi_pld_rcv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted.
15	RO	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted.
14	RO	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written.
13	RO	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written.
12	RO	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.

Bit	Attr	Reset Value	Description
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload.
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet.
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected.
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.

**MIPS\_DSI\_INT\_MSK0**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.
18	RW	0x0	dphy_errors_2 This bit indicates ErrControl control error from Lane 0.



Bit	Attr	Reset Value	Description
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report.
14	RW	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report.
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report.
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report.
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.
7	RW	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report.
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge error report.
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report.
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report.
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report.
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report.

**MIPS DSI INT MSK1**

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	dbi_illegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission.
16	RW	0x0	dbi_pld_rcv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted.
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted.
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written.
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written.
12	RW	0x0	gen_pld_rcv_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.

Bit	Attr	Reset Value	Description
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload.
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet.
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected.
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.

**MIPS DSI INT FORCE0**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	WO	0x0	dphy_errors_4 This bit indicates LP1 contention error ErrContentionLP1 from Lane 0.
19	WO	0x0	dphy_errors_3 This bit indicates LP0 contention error ErrContentionLP0 from Lane 0.
18	WO	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0.
17	WO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.
16	WO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	WO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report.
14	WO	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
13	WO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report.
12	WO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.
11	WO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report.

Bit	Attr	Reset Value	Description
10	WO	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report.
9	WO	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.
8	WO	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.
7	WO	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
6	WO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report.
5	WO	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge error report.
4	WO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report.
3	WO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.
2	WO	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report.
1	WO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report.
0	WO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report.

**MIPS DSI INT FORCE1**

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	WO	0x0	dbi_illegal_comm_err_OR_reserved This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission.
16	WO	0x0	dbi_pld_rcv_err_OR_reserved This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted.
15	WO	0x0	dbi_pld_rd_err_OR_reserved This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted.
14	WO	0x0	dbi_pld_wr_err_OR_reserved This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written.

Bit	Attr	Reset Value	Description
13	WO	0x0	dbi_cmd_wr_err_OR_reserved This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written.
12	WO	0x0	gen_pld_recev_err_OR_reserved This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	WO	0x0	gen_pld_rd_err_OR_reserved This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.
10	WO	0x0	gen_pld_send_err_OR_reserve This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	WO	0x0	gen_pld_wr_en_OR_reserved This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.
8	WO	0x0	gen_cmd_wr_err_Or_reserved This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	WO	0x0	dpi_pld_wr_err_OR_reserved This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	WO	0x0	eopt_err This bit indicates that the EoTp packet has not been received at the end of the incoming peripheral transmission.
5	WO	0x0	pkt_size_err This bit indicates that the packet size error has been detected during the packet reception.
4	WO	0x0	cro_err_OR_reserved This bit indicates that the CRC error has been detected in the received packet payload.
3	WO	0x0	ecc_milti_err This bit indicates that the ECC multiple error has been detected in a received packet.
2	WO	0x0	ecc_single_err This bit indicates that the ECC single error has been detected and corrected in a received packet.
1	WO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention has been detected.
0	WO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention has been detected.

**MIPS DSI VID SHADOW CTRL**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	vid_shadow_pin_req 1'b0: ignored the video request is done by external pin. 1'b1: the video request is done by external pin. In this mode, vid_shadow_req is ignored.

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8	RW	0x0	vid_shadow_req 1'b0:disable the DPI registers are copied to the auxiliary registers. 1'b1:When set to 1, the DPI registers are copied to the auxiliary registers. After copying, this bit is auto cleared.
7:1	RO	0x00	reserved
0	RW	0x0	vid_shadow_en When set to 1, DPI receives the active configuration from the auxiliary registers. When this bit is set along with the vid_shadow_req bit, the auxiliary registers are automatically updated.

**MIPS DSI DPI VCID ACT**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets.

**MIPS DSI DPI COLOR CODING ACT**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	loosely18_en 1'b0:disable loosely packed variant to 18-bit configurations. 1'b1:enable loosely packed variant to 18-bit configurations.
7:4	RO	0x0	reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4'b0000: 16-bit configuration 1 4'b0001: 16-bit configuration 2 4'b0010: 16-bit configuration 3 4'b0011: 18-bit configuration 4 4'b0100: 18-bit configuration 4'b0101: 24-bit 4'b0110: 20-bit YCbCr 4:2:2 loosely packed 4'b0111: 24-bit YCbCr 4:2:2 4'b1000: 16-bit YCbCr 4:2:2 4'b1001: 30-bit 4'b1010: 36-bit 4'b1011-1111: 12-bit YCbCr 4:2:0

**MIPS DSI DPI LP CMD TIM ACT**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions.
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region.

**MIPS DSI VID MODE CFG ACT**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	lp_cmd_en 1'b0: disable the command transmission only in lowpower mode. 1'b1: enables the command transmission only in lowpower mode.
14	RO	0x0	frame_bta_ack_en 1'b0: disable the request for an acknowledge response at the end of a frame. 1'b1: enables the request for an acknowledge response at the end of a frame.
13	RO	0x0	lp_hfp_en 1'b0: disable the return to low-power inside the HFP period when timing allows. 1'b1: enables the return to low-power inside the HFP period when timing allows.
12	RO	0x0	lp_hbp_en 1'b0: disable the return to low-power inside the HBP period when timing allows. 1'b1: enables the return to low-power inside the HBP period when timing allows.
11	RO	0x0	lp_vact_en 1'b0: disable the return to low-power inside the VACT period when timing allows. 1'b1: enables the return to low-power inside the VACT period when timing allows.
10	RO	0x0	lp_vfp_en 1'b0: disable the return to low-power inside the VFP period when timing allows. 1'b1: enables the return to low-power inside the VFP period when timing allows.
9	RO	0x0	lp_vbp_en 1'b0: disable the return to low-power inside the VBP period when timing allows. 1'b1: enables the return to low-power inside the VBP period when timing allows.
8	RO	0x0	lp_vsa_en 1'b0: disable the return to low-power inside the VSA period when timing allows. 1'b1: enables the return to low-power inside the VSA period when timing allows.
7:2	RO	0x00	reserved
1:0	RO	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses. 2'b01: Non-burst with sync events. 2'b10 and 11: Burst mode.

**MIPS DSI VID PKT SIZE ACT**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed, this number must be a multiple of four and for YCbCr data types, it must be a multiple of 2, as described in DSI specification.

**MIPS DSI VID NUM CHUNKS ACT**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk is pair made of a video packet and a null packet). If set to 0 or 1, video line is still transmitted in a single packet. If set to 1 that packet is part of a chunk, meaning that a null packet follows it (if vid_null_size>0). Otherwise, multiple chunks are used to transmit each video line.

**MIPS DSI VID NULL SIZE ACT**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables null packets.

**MIPS DSI VID HSA TIME ACT**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles.

**MIPS DSI VID HBP TIME ACT**

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	vid_hbp_time This field configures the Horizontal Back Porch period in lane byte clock cycles.

**MIPS DSI VID HLINE TIME ACT**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles.

**MIPS DSI VID VSA LINES ACT**

Address: Operational Base + offset (0x0154)



Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines.

**MIPS DSI VID VBP LINES ACT**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines.

**MIPS DSI VID VFP LINES ACT**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines.

**MIPS DSI VID VACTIVE LINES ACT**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:14	RO	0x000000	reserved
13:0	RW	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines.

## 7.5 Application Notes

### 7.5.1 Low Power Mode(For DSI Only)

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

Perform the following steps to configure the DPI packet transmission:

Step1: Global configuration:

Configure n\_lanes (PHY\_IF\_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.

Step2: Configure the DPI Interface to define how the DPI interface interacts with the controller.

Configure dpi\_vid (DPI\_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.

Configure dpi\_color\_coding (DPI\_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable\_18\_loosely\_packed is not active, the number of pixels per line should be a multiple of four.

Configure dataen\_active\_low (DPI\_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.

Configure vsync\_active\_low( DPI\_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync\_active\_low( DPI\_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync\_active\_low( DPI\_CFG-[8]): This bit configures the polarity of the dpishutdn

signal and enables if it is active low.

Configure vsync\_active\_low( DPI\_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.

Configure en18\_loosely( DPI\_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi\_color\_coding is 18 bpp. This bit enables loosely packing.

Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.

Configure low-power transitions (VID\_MODE\_CFG-[8:3]): This defines the video line to be transported through the DSI link.

Configure low-power transitions (VID\_MODE\_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.

Configure frame\_BTA\_ack (VID\_MODE\_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.

Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the mipi\_dsi\_host to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.

Configure the register field vid\_mode\_type (VID\_MODE\_CFG-[10]), num\_chunks (VID\_PKT\_CFG-[20:11]), and null\_pkt\_size (VID\_PKT\_CFG-[30:21]) are automatically ignored by the mipi\_dsi\_host.

Non-Burst mode: In this mode, the processor uses the partitioning properties of the mipi\_dsi\_host to divide the video line transmission into several DSI packets. This is done to match the pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.

Configure the vid\_mode\_type field (VID\_MODE\_CFG-[2:1]) with 2'b0x.

Configure the vid\_mode\_type field (VID\_MODE\_CFG-[2:1]) with 2'b00x to enable the transmission of sync pulses.

Configure the vid\_mode\_type field (VID\_MODE\_CFG-[2:1]) with 2'b01 to enable the transmission of sync events.

Configure the vid\_mode\_type field (VID\_MODE\_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.

Configure the en\_multi\_pkt field (VID\_MODE\_CFG-[9]) to enable the division of the active video transmission into more than one packet.

Configure the num\_chunks field (VID\_MODE\_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.

Configure the en\_null\_pkt field (VID\_MODE\_CFG-[10]) to enable the insertion of null packets between video packets.

The field is effective only when en\_multi\_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.

Configure the null\_pkt\_size field (VID\_MODE\_CFG-[30:21]) with the actual size of the inserted null packet.

Step4: Define the DPI Horizontal timing configuration as follows:

Configure the hline\_time field (TMR\_LINE\_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline\_time is a result of a round of a number. If the mipi\_dsi\_host is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the mipi\_dsi\_host can have a number of errors that can cause a malfunction of the video transmission.

Configure the hsa\_time field (TMR\_LINE\_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).

Configure the hbp\_time field (TMR\_LINE\_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.

Step5: Define the Vertical line configuration:

Configure the vsa\_lines field (VTIMING\_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.

Configure the vbp\_lines field (VTIMING\_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.

Configure the vfp\_lines field (VTIMING\_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.

Configure the v\_active\_lines field (VTIMING\_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

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## Chapter 8 Video Capture (VICAP)

### 8.1 Overview

The Video Capture, receives the data from Camera via DVP/MIPI/LVDS, and transfers the data into system main memory by AXI bus.

There are VICAP and VICAP\_LITE in RV1109/RV1126. The features of VICAP are as follow:

- Support BT601 YCbCr 422 8bit input、RAW 8/10/12bit input
- Support BT656 YCbCr 422 8bit input
- Support BT1120 YCbCr 422 8bit input, single/dual-edge sampling
- Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input
- Support YUYV sequence configurable
- Support the polarity of pixel\_clk, hsync and vsync configurable
- Support receiving CSI2 protocol data(up to four IDs)
- Support receiving DSI protocol data(Video mode/Command mode)
- Support receiving LVDS protocol data(up to four IDs)
- Support window cropping
- Support virtual stride when write to DDR
- Support NV16/NV12 output for YUV data
- Support compact/non-compact output for RAW data
- Support MMU

The features of VICAP\_LITE are as follow:

- Support receiving LVDS protocol data(up to four IDs)
- Support window cropping
- Support virtual stride when write to DDR
- Support compact/non-compact output for RAW data
- Support MMU

### 8.2 Block Diagram

VICAP/VICAP\_LITE comprises with:

- AHB Slave

Host configure the registers via the AHB Slave

- AXI Master

Transmit the data to chip memory via the AXI Master

- MMU

Map the virtual address to physical address

- INTERFACE

Translate the input video data(DVP/CSI/LVDS) into the requisite data format

- CROP

Bypass or crop the source video data to a smaller size destination

- DMA

Control the operation of AXI Master

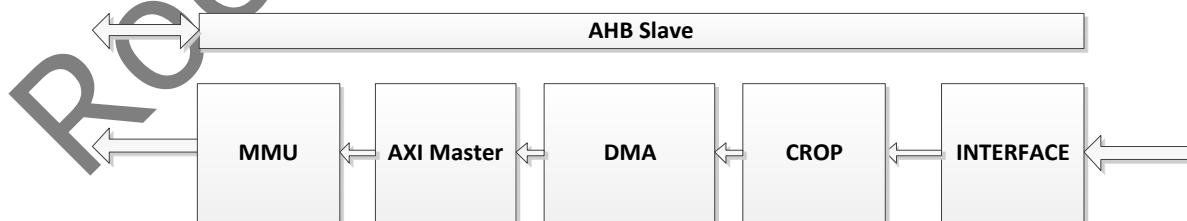


Fig. 8-1 VICAP Block Diagram

### 8.3 Function Description

#### 8.3.1 Interface

Interface module is designed to receive DVP/CSI/LVDS data and transfer to pixel data.

#### 8.3.2 Crop

Crop module is used to crop the received image.

### 8.3.3 DMA

The DMA is used to transfer the data from crop module to the AXI master block which will send the data to the AXI bus.

### 8.3.4 AXI Master

There is an AXI master in VICAP, it is responsible for transferring the DMA output data to AXI bus.

### 8.3.5 MMU

There is a MMU in VICAP, it is responsible for mapping the virtual address to physical address.

## 8.4 VICAP Register Description

### 8.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 8.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VICAP_DVP_CTRL	0x0000	W	0x00007000	DVP path control
VICAP_DVP_INTEN	0x0004	W	0x00000000	DVP path interrupt status
VICAP_DVP_INTSTAT	0x0008	W	0x00000000	DVP path interrupt status
VICAP_DVP_FOR	0x000C	W	0x00000000	DVP path format
VICAP_DVP_MULTI_ID	0x0010	W	0x00000000	Channel ID for multi-ID mode
VICAP_DVP_FRM0_ADDR_Y	0x0014	W	0x00000000	DVP path frame0 y address
VICAP_DVP_FRM0_ADDR_UV	0x0018	W	0x00000000	DVP path frame0 uv address
VICAP_DVP_FRM1_ADDR_Y	0x001C	W	0x00000000	DVP path frame1 y address
VICAP_DVP_FRM1_ADDR_UV	0x0020	W	0x00000000	DVP path frame1 uv address
VICAP_DVP_VIR_LINE_WIDTH	0x0024	W	0x00000000	DVP path virtual line width
VICAP_DVP_SET_SIZE	0x0028	W	0x01E002D0	The expected width and height of received image
VICAP_DVP_LINE_INT_NUM	0x002C	W	0x00000040	DVP path line interrupt number
VICAP_DVP_LINE_CNT	0x0030	W	0x00000000	DVP path line count
VICAP_DVP_CROP	0x0034	W	0x00000000	The start point of DVP path cropping
VICAP_DVP_FIFO_ENTRY	0x0038	W	0x00000000	DVP path FIFO entry
VICAP_DVP_FRAME_STATUS	0x003C	W	0x00000000	DVP path frame status
VICAP_DVP_CUR_DST	0x0040	W	0x00000000	DVP path current destination address
VICAP_DVP_LAST_LINE	0x0044	W	0x00000000	DVP path last frame line number
VICAP_DVP_LAST_PIX	0x0048	W	0x00000000	DVP path last line pixel number
VICAP_DVP_FRM0_ADDR_Y_ID1	0x0050	W	0x00000000	DVP path frame0 y address for ID1
VICAP_DVP_FRM0_ADDR_UV_ID1	0x0054	W	0x00000000	DVP path frame0 uv address for id1
VICAP_DVP_FRM1_ADDR_Y_ID1	0x0058	W	0x00000000	DVP path frame1 y address for id1
VICAP_DVP_FRM1_ADDR_UV_ID1	0x005C	W	0x00000000	DVP path frame1 uv address for id1

Name	Offset	Size	Reset Value	Description
VICAP DVP FRM0 ADDR Y ID2	0x0060	W	0x00000000	DVP path frame0 y address for id2
VICAP DVP FRM0 ADDR UV ID2	0x0064	W	0x00000000	DVP path frame0 uv address for id2
VICAP DVP FRM1 ADDR Y ID2	0x0068	W	0x00000000	DVP path frame1 y address for id2
VICAP DVP FRM1 ADDR UV ID2	0x006C	W	0x00000000	DVP path frame1 uv address for id2
VICAP DVP FRM0 ADDR Y ID3	0x0070	W	0x00000000	DVP path frame0 y address for id3
VICAP DVP FRM0 ADDR UV ID3	0x0074	W	0x00000000	DVP path frame0 uv address for id3
VICAP DVP FRM1 ADDR Y ID3	0x0078	W	0x00000000	DVP path frame1 y address for id3
VICAP DVP FRM1 ADDR UV ID3	0x007C	W	0x00000000	DVP path frame1 uv address for id3
VICAP MIPI LVDS ID0 CTRL0	0x0080	W	0x00000000	MIPI/LVDS path id0 control0
VICAP MIPI LVDS ID0 CTRL1	0x0084	W	0x00000000	MIPI/LVDS path id0 control1
VICAP MIPI LVDS ID1 CTRL0	0x0088	W	0x00000000	MIPI/LVDS path id1 control0
VICAP MIPI LVDS ID1 CTRL1	0x008C	W	0x00000000	MIPI/LVDS path id1 control1
VICAP MIPI LVDS ID2 CTRL0	0x0090	W	0x00000000	MIPI/LVDS path id2 control0
VICAP MIPI LVDS ID2 CTRL1	0x0094	W	0x00000000	MIPI/LVDS path id2 control1
VICAP MIPI LVDS ID3 CTRL0	0x0098	W	0x00000000	MIPI/LVDS path id3 control0
VICAP MIPI LVDS ID3 CTRL1	0x009C	W	0x00000000	MIPI/LVDS path id3 control1
VICAP MIPI LVDS CTRL	0x00A0	W	0x00000001	MIPI/LVDS path control
VICAP MIPI LVDS FRAME 0 ADDR Y ID0	0x00A4	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 ADDR Y ID0	0x00A8	W	0x00000000	First address of odd frame for ID0 Y path
VICAP MIPI LVDS FRAME 0 ADDR UV ID0	0x00AC	W	0x00000000	First address of even frame for ID0 UV path
VICAP MIPI LVDS FRAME 1 ADDR UV ID0	0x00B0	W	0x00000000	First address of odd frame for ID0 UV path
VICAP MIPI LVDS FRAME 0 VLW Y ID0	0x00B4	W	0x00000000	Virtual line width of even frame for ID0 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 VLW Y ID0	0x00B8	W	0x00000000	Virtual line width of odd frame for ID0 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 0 VLW UV ID0	0x00BC	W	0x00000000	Virtual line width of even frame for ID0 UV path
VICAP MIPI LVDS FRAME 1 VLW UV ID0	0x00C0	W	0x00000000	Virtual line width of odd frame for ID0 UV path
VICAP MIPI LVDS FRAME 0 ADDR Y ID1	0x00C4	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 ADDR Y ID1	0x00C8	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path

Name	Offset	Size	Reset Value	Description
VICAP MIPI LVDS FRAME 0 ADDR UV ID1	0x00CC	W	0x00000000	First address of even frame for ID1 UV path
VICAP MIPI LVDS FRAME 1 ADDR UV ID1	0x00D0	W	0x00000000	First address of odd frame for ID1 UV path
VICAP MIPI LVDS FRAME 0 VLW Y ID1	0x00D4	W	0x00000000	Virtual line width of even frame for ID1 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 VLW Y ID1	0x00D8	W	0x00000000	Virtual line width of odd frame for ID1 Y path
VICAP MIPI LVDS FRAME 0 VLW UV ID1	0x00DC	W	0x00000000	Virtual line width of even frame for ID1 UV path
VICAP MIPI LVDS FRAME 1 VLW UV ID1	0x00E0	W	0x00000000	Virtual line width of odd frame for ID1 UV path
VICAP MIPI LVDS FRAME 0 ADDR Y ID2	0x00E4	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 ADDR Y ID2	0x00E8	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 0 ADDR UV ID2	0x00EC	W	0x00000000	First address of even frame for ID2 UV path
VICAP MIPI LVDS FRAME 1 ADDR UV ID2	0x00F0	W	0x00000000	First address of odd frame for ID2 UV path
VICAP MIPI LVDS FRAME 0 VLW Y ID2	0x00F4	W	0x00000000	Virtual line width of even frame for ID2 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 VLW Y ID2	0x00F8	W	0x00000000	Virtual line width of odd frame for ID2 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 0 VLW UV ID2	0x00FC	W	0x00000000	Virtual line width of even frame for ID2 UV path
VICAP MIPI LVDS FRAME 1 VLW UV ID2	0x0100	W	0x00000000	Virtual line width of odd frame for ID2 UV path
VICAP MIPI LVDS FRAME 0 ADDR Y ID3	0x0104	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 ADDR Y ID3	0x0108	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 0 ADDR UV ID3	0x010C	W	0x00000000	First address of even frame for ID3 UV path
VICAP MIPI LVDS FRAME 1 ADDR UV ID3	0x0110	W	0x00000000	First address of odd frame for ID3 UV path
VICAP MIPI LVDS FRAME 0 VLW Y ID3	0x0114	W	0x00000000	Virtual line width of even frame for ID3 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 1 VLW Y ID3	0x0118	W	0x00000000	Virtual line width of odd frame for ID3 Y/RAW/RGB path
VICAP MIPI LVDS FRAME 0 VLW UV ID3	0x011C	W	0x00000000	Virtual line width of even frame for ID3 UV path
VICAP MIPI LVDS FRAME 1 VLW UV ID3	0x0120	W	0x00000000	Virtual line width of odd frame for ID3 UV path
VICAP MIPI LVDS INTEN	0x0124	W	0x00000000	MIPI/LVDS path interrupt enable
VICAP MIPI LVDS INTST AT	0x0128	W	0x00000000	MIPI/LVDS path interrupt status
VICAP MIPI LVDS LINE INT NUM ID0 1	0x012C	W	0x00400040	Line number of the MIPI/LVDS path ID0/1 line interrupt
VICAP MIPI LVDS LINE INT NUM ID2 3	0x0130	W	0x00400040	Line number of the MIPI/LVDS path ID2/3 line interrupt
VICAP MIPI LVDS LINE CNT ID0 1	0x0134	W	0x00000000	Line count of the MIPI/LVDS path ID0/1

Name	Offset	Size	Reset Value	Description
VICAP MIPI LVDS LINE CNT ID2_3	0x0138	W	0x00000000	Line count of the MIPI/LVDS path ID2/3
VICAP MIPI LVDS ID0 CROP START	0x013C	W	0x00000000	The start point of MIPI/LVDS ID0 cropping
VICAP MIPI LVDS ID1 CROP START	0x0140	W	0x00000000	The start point of MIPI/LVDS ID1 cropping
VICAP MIPI LVDS ID2 CROP START	0x0144	W	0x00000000	The start point of MIPI/LVDS ID2 cropping
VICAP MIPI LVDS ID3 CROP START	0x0148	W	0x00000000	The start point of MIPI/LVDS ID3 cropping
VICAP LVDS SAV EAV A CT0 ID0	0x0150	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id0
VICAP LVDS SAV EAV B LK0 ID0	0x0154	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id0
VICAP LVDS SAV EAV A CT1 ID0	0x0158	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id0
VICAP LVDS SAV EAV B LK1 ID0	0x015C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id0
VICAP LVDS SAV EAV A CT0 ID1	0x0160	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id1
VICAP LVDS SAV EAV B LK0 ID1	0x0164	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id1
VICAP LVDS SAV EAV A CT1 ID1	0x0168	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id1
VICAP LVDS SAV EAV B LK1 ID1	0x016C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id1
VICAP LVDS SAV EAV A CT0 ID2	0x0170	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id2
VICAP LVDS SAV EAV B LK0 ID2	0x0174	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id2
VICAP LVDS SAV EAV A CT1 ID2	0x0178	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id2
VICAP LVDS SAV EAV B LK1 ID2	0x017C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id2
VICAP LVDS SAV EAV A CT0 ID3	0x0180	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id3
VICAP LVDS SAV EAV B LK0 ID3	0x0184	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id3
VICAP LVDS SAV EAV A CT1 ID3	0x0188	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id3
VICAP LVDS SAV EAV B LK1 ID3	0x018C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id3
VICAP Y STAT CONTROL	0x0190	W	0x00000000	Y statistics control
VICAP Y STAT VALUE	0x0194	W	0x00000000	Y statistics value
VICAP MMU DTE ADDR	0x0800	W	0x00000000	MMU current page table address
VICAP MMU STATUS	0x0804	W	0x00000000	MMU status register
VICAP MMU COMMAND	0x0808	W	0x00000000	MMU command register
VICAP MMU PAGE FAULT ADDR	0x080C	W	0x00000000	MMU logical address of last page fault
VICAP MMU ZAP ONE LINE	0x0810	W	0x00000000	MMU Zap cache line register
VICAP MMU INT RAWSTAT	0x0814	W	0x00000000	MMU raw interrupt status register



Name	Offset	Size	Reset Value	Description
VICAP MMU INT CLEAR	0x0818	W	0x00000000	MMU interrupt status clear
VICAP MMU INT MASK	0x081C	W	0x00000000	MMU interrupt mask
VICAP MMU INT STATUS	0x0820	W	0x00000000	MMU interrupt status
VICAP MMU AUTO GATING	0x0824	W	0x00000000	MMU auto gating

Notes: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 8.4.3 Detail Registers Description

#### VICAP DVP CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x7	axi_burst_type Burst1~16.
11:5	RO	0x00	reserved
4	RW	0x0	dma_idle_req Write 1 will stop VICAP DVP path dma. When this bit change to 0, dma is stopped really.
3	RO	0x0	reserved
2:1	RW	0x0	work_mode 2'b00: One frame stop mode 2'b01: Ping-pong mode 2'b10: Reserved 2'b11: Reserved Note: BT1120 only support ping-pong mode.
0	RW	0x0	cap_en 1'b0: Disable 1'b1: Enable

#### VICAP DVP INTEN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	dma_frame_end_id3_en ID3 dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	dma_frame_end_id2_en ID2 dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	dma_frame_end_id1_en ID1 dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	line_int_en The specified line end interrupt enable. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pst_inf_frame_end_en Frame end after interface FIFO interrupt enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	pre_inf_frame_end_en Frame end before interface FIFO interrupt enable. 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	W1 C	0x0	bus_err_en Axi master or ahb slave response error interrupt enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	dfifo_of_en DMA FIFO overflow interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ififo_of_en Interface FIFO overflow interrupt enable. 1'b0: Disable 1'b1: Enable
3	W1 C	0x0	pix_err_en The pixel number of last line not equal to the set height interrupt enable. 1'b0: Disable 1'b1: Enable
2	W1 C	0x0	line_err_en The line number of last frame not equal to the set height interrupt enable. 1'b0: Disable 1'b1: Enable
1	W1 C	0x0	line_end_en Line end interrupt enable. 1'b0: Disable 1'b1: Enable
0	W1 C	0x0	dma_frame_end_en Dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable

**VICAP DVP INTSTAT**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	W1 C	0x0	dma_frame_end_id3 ID3 dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt
12	W1 C	0x0	dma_frame_end_id2 ID2 dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt
11	W1 C	0x0	dma_frame_end_id1 ID1 dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
10	RW	0x0	line_int The specified line end interrupt. 1'b0: No interrupt 1'b1: Interrupt
9	RW	0x0	pst_inf_frame_end Frame end after interface FIFO interrupt. 1'b0: No interrupt 1'b1: Interrupt
8	RW	0x0	pre_inf_frame_end Frame end before interface FIFO interrupt. 1'b0: No interrupt 1'b1: Interrupt
7	RO	0x0	reserved
6	W1 C	0x0	bus_err Axi master or ahb slave response error interrupt. 1'b0: No interrupt 1'b1: Interrupt
5	RW	0x0	dfifo_of DMA FIFO overflow interrupt. 1'b0: No interrupt 1'b1: Interrupt
4	RW	0x0	ififo_of Interface FIFO overflow interrupt. 1'b0: No interrupt 1'b1: Interrupt
3	W1 C	0x0	pix_err The pixel number of last line not equal to the set height interrupt. 1'b0: No interrupt 1'b1: Interrupt
2	W1 C	0x0	line_err The line number of last frame not equal to the set height interrupt. 1'b0: No interrupt 1'b1: Interrupt
1	W1 C	0x0	line_end Line end interrupt. 1'b0: No interrupt 1'b1: Interrupt
0	W1 C	0x0	dma_frame_end Dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt

**VICAP\_DVP FOR**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_multi_id_mode 2'd0: 1to1 (ID0 will work) 2'd1: 1to2 (ID0/ID1 will work) 2'd2: 1to4 (ID0/ID1/ID2/ID3 will work) 2'd3: Reserved
29	RW	0x0	sw_multi_id_sel Only for BT1120. 1'b0: Parse the id by data[11:8] 1'b1: Parse the id by data[3:0]

Bit	Attr	Reset Value	Description
28	RW	0x0	sw_multi_id_en 1'b0: Disable multi-ID bt656/bt1120 received 1'b1: Enable multi-ID bt656/bt1120 received
27	RO	0x0	reserved
26	RW	0x0	sw_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for BT1120 mode.
25	RW	0x0	sw_progress_en 1'b0: Interlace 1'b1: Progress Only for BT1120 mode.
24	RW	0x0	sw_dualedge_en 1'b0: Only use single edge of clock 1'b1: Use double edges of clock Only for BT1120 mode.
23:20	RO	0x0	reserved
19	RW	0x0	uv_store_order 1'b0: UVUV 1'b1: VUVU
18	RW	0x0	raw_end 1'b0: Little end 1'b1: Big end
17	RW	0x0	out_420_order 1'b0: UV in the even line 1'b1: UV in the odd line Note: The first line is even line(line 0).
16	RW	0x0	output_420 1'b0: Output is 422 1'b1: Output is 420
15:13	RO	0x0	reserved
12:11	RW	0x0	raw_width 2'b00: 8bit raw data 2'b01: 10bit raw data 2'b10: 12bit raw data 2'b11: Reserve
10	RO	0x0	reserved
9	RW	0x0	field_order 1'b0: Odd field first 1'b1: Even field first
8:7	RO	0x0	reserved
6:5	RW	0x0	yuv_in_order 2'b00: UYVY 2'b01: YVYU 2'b10: VYUY 2'b11: YUYV
4:2	RW	0x0	input_mode 3'b000: YUV 3'b010: PAL 3'b011: NTSC 3'b100: RAW 3'b101: JPEG 3'b110: Reserved 3'b111: BT1120

Bit	Attr	Reset Value	Description
1	RW	0x0	href_pol 1'b0: High active 1'b1: Low active
0	RW	0x0	vsync_pol 1'b0: Low active 1'b1: High active

**VICAP DVP MULTI ID**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_chid_bit_en_id3 Bit enable for chid_id3. Eg: chid_id3 = 4'b1111 and chid_bit_en_id3 = 4'b0011. Then the data[3:0] = 4'bxx11 will be detected.
27:24	RW	0x0	sw_chid_id3 The channel id for id3.
23:20	RW	0x0	sw_chid_bit_en_id2 Bit enable for chid_id2. Eg: chid_id2 = 4'b1111 and chid_bit_en_id2 = 4'b0011. Then the data[3:0] = 4'bxx11 will be detected.
19:16	RW	0x0	sw_chid_id2 The channel id for id2.
15:12	RW	0x0	sw_chid_bit_en_id1 Bit enable for chid_id1. Eg: chid_id1 = 4'b1111 and chid_bit_en_id1 = 4'b0011. Then the data[3:0] = 4'bxx11 will be detected.
11:8	RW	0x0	sw_chid_id1 The channel id for id1.
7:4	RW	0x0	sw_chid_bit_en_id0 Bit enable for chid_id0. Eg: chid_id0 = 4'b1111 and chid_bit_en_id0 = 4'b0011. Then the data[3:0] = 4'bxx11 will be detected.
3:0	RW	0x0	sw_chid_id0 The channel id for id0.

**VICAP DVP FRM0 ADDR Y**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y DVP path frame0 y address.

**VICAP DVP FRM0 ADDR UV**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv DVP path frame0 uv address.

**VICAP DVP FRM1 ADDR Y**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y DVP path frame1 y address.

**VICAP DVP FRM1 ADDR UV**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv DVP path frame1 uv address.

**VICAP DVP VIR LINE WIDTH**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	vir_line_width DVP path virtual line width.

**VICAP DVP SET SIZE**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x01e0	set_height The expected height of received image.
15:13	RO	0x0	reserved
12:0	RW	0x02d0	set_width The expected width of received image.

**VICAP DVP LINE INT NUM**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0040	line_int_num If line_int_num=100, then vicap receive 100th line200th line300th line....the line_int will be 1.

**VICAP DVP LINE CNT**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	line_cnt Current line count.

**VICAP DVP CROP**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	start_y The vertical ordinate of the start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	start_x The horizontal ordinate of the start point.

**VICAP DVP FIFO ENTRY**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	uv_fifo_entry Write 0 clear.
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8:0	RO	0x000	y_fifo_entry Write 0 clear.

**VICAP DVP FRAME STATUS**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	frame_num Completed frame number Write 0 to clear.
15:14	RO	0x0	reserved
13	RO	0x0	f1_sts_id3 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
12	RO	0x0	f0_sts_id3 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.
11:10	RO	0x0	reserved
9	RO	0x0	f1_sts_id2 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
8	RO	0x0	f0_sts_id2 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.
7:6	RO	0x0	reserved
5	RO	0x0	f1_sts_id1 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
4	RO	0x0	f0_sts_id1 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.
3	RO	0x0	reserved
2	RO	0x0	idle 1'b0: Work 1'b1: Idle
1	RO	0x0	f1_sts 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
0	RO	0x0	f0_sts 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.

**VICAP DVP CUR\_DST**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cur_dst DVP path current destination address.

**VICAP DVP LAST LINE**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	last_uv_num UV line number of last frame, only for bt1120 mode.
15:13	RO	0x0	reserved
12:0	RO	0x0000	last_y_num Y line number of last frame.

**VICAP DVP LAST PIX**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	last_uv_num DVP path last line uv number.
15:13	RO	0x0	reserved
12:0	RO	0x0000	last_y_num DVP path last line y number.

**VICAP DVP FRM0 ADDR Y ID1**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y_id1 DVP path frame0 y address for id1.

**VICAP DVP FRM0 ADDR UV ID1**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv_id1 DVP path frame0 uv address for id1.

**VICAP DVP FRM1 ADDR Y ID1**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y_id1 DVP path frame1 y address for id1.

**VICAP DVP FRM1 ADDR UV ID1**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv_id1 DVP path frame1 uv address for id1.

**VICAP DVP FRM0 ADDR Y ID2**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y_id2 DVP path frame0 y address for id2.

**VICAP DVP FRM0 ADDR UV ID2**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv_id2 DVP path frame0 uv address for id2.



**VICAP DVP FRM1 ADDR Y ID2**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y_id2 DVP path frame1 y address for id2.

**VICAP DVP FRM1 ADDR UV ID2**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv_id2 DVP path frame1 uv address for id2.

**VICAP DVP FRM0 ADDR Y ID3**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y_id3 DVP path frame0 y address for id3.

**VICAP DVP FRM0 ADDR UV ID3**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv_id3 DVP path frame0 uv address for id3.

**VICAP DVP FRM1 ADDR Y ID3**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y_id3 DVP path frame1 y address for id3.

**VICAP DVP FRM1 ADDR UV ID3**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv_id3 DVP path frame1 uv address for id3.

**VICAP MIPI LVDS ID0 CTRL0**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_lvds_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when non-compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id0 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id0 Only be used when the sw_lvds_mode_id0=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id0 Only be used when the sw_lvds_mode_id0=3'b011. Choose the fid for id0.

Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_lvds_main_lane_id0 Choose the lane to parse the sync code
23:20	RW	0x0	sw_lvds_lane_en_id0 Lane enable for id0. eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id0 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserverd
16	RW	0x0	sw_lvds_cap_en_id0 Enable to capture lvds id0. 1'b0: Disable 1'b1: Enable
15:10	RW	0x00	sw_mipi_dt_id0 Data type for id0.
9:8	RW	0x0	sw_mipi_vc_id0 Virtual channel for id0.
7	RW	0x0	sw_mipi_uv_swap_id0 1'b0: No swap 1'b1: Swap
6	RW	0x0	sw_mipi_compact_id0 1'b0: raw10/12 will occupy 16bit 1'b1: raw10/12 will be compacted
5	RW	0x0	sw_mipi_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id0 The type of id0. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

**VICAP MIPI LVDS ID0 CTRL1**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_width_id0 Width for id0 if sw_wrddr_type is rgb888, then the width is equal to the number of bytes (not pixel). If sw_crop_en_id0 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12, and must be 24 aligned when sw_wrddr_type is rgb888.

**VICAP MIPI LVDS ID1 CTRL0**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_lvds_align_id1 1'b0: Low alignment (raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment (raw10/12 will in [15:6]/[15:4]) Only be used when non-compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id1 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id1 Only be used when the sw_lvds_mode_id1=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id1 Only be used when the sw_lvds_mode_id1=3'b011. Choose the fid for id1.
25:24	RW	0x0	sw_lvds_main_lane_id1 Choose the lane to parse the sync code.
23:20	RW	0x0	sw_lvds_lane_en_id1 Lane enable for id1. Eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id1 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserved
16	RW	0x0	sw_lvds_cap_en_id1 Enable to capture lvds id1. 1'b0: Disable 1'b1: Enable
15:10	RW	0x00	sw_mipi_dt_id1 Data type for id1.
9:8	RW	0x0	sw_mipi_vc_id1 Virtual channel for id1.
7	RW	0x0	sw_mipi_uv_swap_id1 1'b0: No swap 1'b1: Swap
6	RW	0x0	sw_mipi_compact_id1 1'b0: raw10/12 will occupy 16bit 1'b1: raw10/12 will be compacted

Bit	Attr	Reset Value	Description
5	RW	0x0	sw_mipi_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id1 The type of id1. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

**VICAP MIPI LVDS ID1 CTRL1**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1 if sw_wrddr_type is rgb888, then the width is equal to the number of bytes (not pixel). If sw_crop_en_id1 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12, and must be 24 aligned when sw_wrddr_type is rgb888.

**VICAP MIPI LVDS ID2 CTRL0**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_lvds_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id2 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id2 Only be used when the sw_lvds_mode_id2=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id2 Only be used when the sw_lvds_mode_id2=3'b011. Choose the fid for id2.

Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_lvds_main_lane_id2 Choose the lane to parse the sync code
23:20	RW	0x0	sw_lvds_lane_en_id2 Lane enable for id2. eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id2 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserved
16	RW	0x0	sw_lvds_cap_en_id2 Enable to capture lvds id2. 1'b0: Disable 1'b1: Enable
15:10	RW	0x00	sw_mipi_dt_id2 Data type for id2.
9:8	RW	0x0	sw_mipi_vc_id2 Virtual channel for id2.
7	RW	0x0	sw_mipi_uv_swap_id2 1'b0: No swap 1'b1: Swap
6	RW	0x0	sw_mipi_compact_id2 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
5	RW	0x0	sw_mipi_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id2 The type of id2. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

**VICAP MIPI LVDS ID2 CTRL1**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_width_id2 Width for id2if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel). If sw_crop_en_id2 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddr_type is rgb888.

**VICAP MIPI LVDS ID3 CTRL0**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_lvds_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id3 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id3 Only be used when the sw_lvds_mode_id3=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id3 Only be used when the sw_lvds_mode_id3=3'b011. Choose the fid for id3.
25:24	RW	0x0	sw_lvds_main_lane_id3 Choose the lane to parse the sync code.
23:20	RW	0x0	sw_lvds_lane_en_id3 Lane enable for id3. Eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id3 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserverd
16	RW	0x0	sw_lvds_cap_en_id3 Enable to capture lvds id3. 1'b0: Disable 1'b1: Enable
15:10	RW	0x00	sw_mipi_dt_id3 Data type for id3.
9:8	RW	0x0	sw_mipi_vc_id3 Virtual channel for id3.
7	RW	0x0	sw_mipi_uv_swap_id3 1'b0: No swap 1'b1: Swap
6	RW	0x0	sw_mipi_compact_id3 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted

Bit	Attr	Reset Value	Description
5	RW	0x0	sw_mipi_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id3 The type of id3. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

**VICAP MIPI LVDS ID3 CTRL1**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel). If sw_crop_en_id3 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddr_type is rgb888.

**VICAP MIPI LVDS CTRL**

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_dma_idle 1'b0: Not idle 1'b1: Idle MIPI/LVDS path dma transport
15	RO	0x0	reserved
14:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11	RO	0x0	reserved
10:9	RW	0x0	sw_lvds_width 2'b00: 8bit 2'b01: 10bit 2'b10: 12bit

Bit	Attr	Reset Value	Description
8	RW	0x0	sw_mipi_lvds_sel 1'b0: MIPI path 1'b1: LVDS path
7	RO	0x0	reserved
6:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RW	0x1	sw_water_line_en 1'b0: Disable water line 1'b1: Enable water line

**VICAP MIPI LVDS FRAME0 ADDR Y ID0**

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR Y ID0**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR UV ID0**

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR UV ID0**

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW Y ID0**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id0 Virtual line width of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).



**VICAP MIPI LVDS FRAME1 VLW Y ID0**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id0 Virtual line width of odd frame for ID0 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW UV ID0**

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id0 Virtual line width of even frame for ID0 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW UV ID0**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id0 Virtual line width of odd frame for ID0 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR Y ID1**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR Y ID1**

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR UV ID1**

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR UV ID1**

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW Y ID1**

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_vlw_y_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW Y ID1**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id1 Virtual line width of odd frame for ID1 Y path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW UV ID1**

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id1 Virtual line width of even frame for ID1 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW UV ID1**

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id1 Virtual line width of odd frame for ID1 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR Y ID2**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR Y ID2**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR UV ID2**

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR UV ID2**

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW Y ID2**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id2 Virtual line width of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW Y ID2**

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id2 Virtual line width of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW UV ID2**

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id2 Virtual line width of even frame for ID2 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW UV ID2**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id2 Virtual line width of odd frame for ID2 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR Y ID3**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR Y ID3**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 ADDR UV ID3**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 ADDR UV ID3**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW Y ID3**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id3 Virtual line width of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW Y ID3**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id0 Virtual line width of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

**VICAP MIPI LVDS FRAME0 VLW UV ID3**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id3 Virtual line width of even frame for ID3 UV path(must be aligned to double word).

**VICAP MIPI LVDS FRAME1 VLW UV ID3**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id3 Virtual line width of odd frame for ID3 UV path(must be aligned to double word).

**VICAP MIPI LVDS INTEN**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	dma_lvds_id3_fifo_overflow_inten Enable the interrupt of dma fifo overflow of lvds id3 path. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
25	RW	0x0	dma_lvds_id2_fifo_overflow_inten Enable the interrupt of dma fifo overflow of lvds id2 path. 1'b0: Disable 1'b1: Enable
24	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	config_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

**VICAP MIPI LVDS INTSTAT**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	W1 C	0x0	dma_lvds_id3_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1 C	0x0	dma_lvds_id2_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
24	RW	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
23	RW	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
22	RW	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
21	RW	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1 C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1 C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1 C	0x0	config_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1 C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1 C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1 C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1 C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1 C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1 C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1 C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1 C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1 C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1 C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1 C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
6	W1 C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1 C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1 C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1 C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1 C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1 C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1 C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

**VICAP MIPI LVDS LINE INT NUM ID0 1**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 If line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15:14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 If line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

**VICAP MIPI LVDS LINE INT NUM ID2 3**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 If line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15:14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 If line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

**VICAP MIPI LVDS LINE CNT ID0 1**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved



Bit	Attr	Reset Value	Description
13:0	RO	0x0000	line_cnt_id0 Current line count for id0.

**VICAP MIPI LVDS LINE CNT ID2 3**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	line_cnt_id2 Current line count for id2.

**VICAP MIPI LVDS ID0 CROP START**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

**VICAP MIPI LVDS ID1 CROP START**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

**VICAP MIPI LVDS ID2 CROP START**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2, if sw_wrddr_type is rgb888, then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12, and must be 24 aligned when sw_wrddr_type is rgb888.

**VICAP MIPI LVDS ID3 CROP START**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3, if sw_wrddr_type is rgb888, then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12, and must be 24 aligned when sw_wrddr_type is rgb888.

**VICAP LVDS SAV EAV ACT0 ID0**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id0 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id0 LVDS path sync code of sav_act0.

**VICAP LVDS SAV EAV BLK0 ID0**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id0 LVDS path sync code of eav_blk0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id0 LVDS path sync code of sav_blk0.

**VICAP LVDS SAV EAV ACT1 ID0**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id0 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id0 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID0**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id0 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id0 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT0 ID1**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id1 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id1 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK0 ID1**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id1 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id1 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT1 ID1**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id1 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id1 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID1**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id1 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id1 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT0 ID2**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id2 LVDS path sync code of eav_act0.

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id2 LVDS path sync code of sav_act0.

**VICAP LVDS SAV EAV BLK0 ID2**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id2 LVDS path sync code of eav_blk0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id2 LVDS path sync code of sav_blk2.

**VICAP LVDS SAV EAV ACT1 ID2**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id2 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id2 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID2**

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id2 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id2 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT0 ID3**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id3 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id3 LVDS path sync code of sav_act0.

**VICAP LVDS SAV EAV BLK0 ID3**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id3 LVDS path sync code of eav_blk0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id3 LVDS path sync code of sav_blk0.

**VICAP LVDS SAV EAV ACT1 ID3**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id3 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id3 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID3**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id3 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id3 LVDS path sync code of sav_blk1.

**VICAP Y STAT CONTROL**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:26	RW	0x00	sw_black_level_b Black level for B channel.
25:21	RW	0x00	sw_black_level_g Black level for G channel.
20:16	RW	0x00	sw_black_level_r Black level for R channel.
15:14	RO	0x0	reserved
13:12	RO	0x0	ro_block_id2 The number of block of id2.
11:10	RO	0x0	ro_block_id1 The number of block of id1.
9:8	RO	0x0	ro_block_id0 The number of block of id0.
7:6	WO	0x0	sw_y_stat_rd_block Point to the specified block.
5:4	WO	0x0	sw_y_stat_rd_id 2'b00: Point to ID0 2'b01: Point to ID1 2'b10: Point to ID2 2'b11: Reserved
3	WO	0x0	sw_y_stat_rd Change the y statistics read pointer according to sw_y_stat_rd_id/sw_y_stat_rd_block.
2:1	RW	0x0	sw_bayer_pattern 2'b00: RGGB 2'b01: GRBG 2'b10: GBRG 2'b11: BGGR
0	RW	0x0	sw_y_stat_en 1'b0: Disable y statistics 1'b1: Enable y statistics

**VICAP Y STAT VALUE**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_y_stat_value Y statistics value.

**VICAP MMU DTE ADDR**

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address.

**VICAP MMU STATUS**

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	paging_enabled Paging is enabled.

**VICAP MMU COMMAND**

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE

**VICAP MMU PAGE FAULT ADDR**

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

**VICAP MMU ZAP ONE LINE**

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

**VICAP MMU INT RAWSTAT**

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

**VICAP MMU INT CLEAR**

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error.
0	WO	0x0	page_fault Page fault.

**VICAP MMU INT MASK**

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

**VICAP MMU INT STATUS**

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error.
0	RO	0x0	page_fault Page fault.

**VICAP MMU AUTO GATING**

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self

**8.5 VICAP\_LITE Register Description****8.5.1 Internal Address Mapping**

Slave address can be divided into different length for different usage, which is shown as follows.

**8.5.2 Registers Summary**

Name	Offset	Size	Reset Value	Description
VICAP LVDS ID0 CTRL0	0x0080	W	0x00000000	LVDS path id0 control0
VICAP LVDS ID0 CTRL1	0x0084	W	0x00000000	□LVDS path id0 control1
VICAP LVDS ID1 CTRL0	0x0088	W	0x00000000	□LVDS path id1 control0
VICAP LVDS ID1 CTRL1	0x008C	W	0x00000000	□LVDS path id1 control1
VICAP LVDS ID2 CTRL0	0x0090	W	0x00000000	□LVDS path id2 control0
VICAP LVDS ID2 CTRL1	0x0094	W	0x00000000	□LVDS path id2 control1
VICAP LVDS ID3 CTRL0	0x0098	W	0x00000000	□LVDS path id3 control0
VICAP LVDS ID3 CTRL1	0x009C	W	0x00000000	□LVDS path id3 control1
VICAP LVDS CTRL	0x00A0	W	0x00000001	□LVDS path control
VICAP LVDS FRAME0 ADDR Y ID0	0x00A4	W	0x00000000	First address of even frame for ID0 path
VICAP LVDS FRAME1 ADDR Y ID0	0x00A8	W	0x00000000	First address of odd frame for ID0 path
VICAP LVDS FRAME0 VLW Y ID0	0x00B4	W	0x00000000	Virtual line width of even frame for ID0 path
VICAP LVDS FRAME1 VLW Y ID0	0x00B8	W	0x00000000	Virtual line width of odd frame for ID0 path
VICAP LVDS FRAME0 ADDR Y ID1	0x00C4	W	0x00000000	First address of even frame for ID1 path
VICAP LVDS FRAME1 ADDR Y ID1	0x00C8	W	0x00000000	First address of odd frame for ID1 path
VICAP LVDS FRAME0 VLW Y ID1	0x00D4	W	0x00000000	Virtual line width of even frame for ID1 path
VICAP LVDS FRAME1 VLW Y ID1	0x00D8	W	0x00000000	Virtual line width of odd frame for ID1 path
VICAP LVDS FRAME0 ADDR Y ID2	0x00E4	W	0x00000000	First address of even frame for ID2 path
VICAP LVDS FRAME1 ADDR Y ID2	0x00E8	W	0x00000000	First address of odd frame for ID2 path
VICAP LVDS FRAME0 VLW Y ID2	0x00F4	W	0x00000000	Virtual line width of even frame for ID2 path
VICAP LVDS FRAME1 VLW Y ID2	0x00F8	W	0x00000000	Virtual line width of odd frame for ID2 path
VICAP LVDS FRAME0 ADDR Y ID3	0x0104	W	0x00000000	First address of even frame for ID3 path
VICAP LVDS FRAME1 ADDR Y ID3	0x0108	W	0x00000000	First address of odd frame for ID3 path
VICAP LVDS FRAME0 VLW Y ID3	0x0114	W	0x00000000	Virtual line width of even frame for ID3 path
VICAP LVDS FRAME1 VLW Y ID3	0x0118	W	0x00000000	Virtual line width of odd frame for ID3 path
VICAP LVDS INTEN	0x0124	W	0x00000000	LVDS path interrupt enable
VICAP LVDS INTSTAT	0x0128	W	0x00000000	LVDS path interrupt status
VICAP LVDS LINE INT NUM ID0_1	0x012C	W	0x00400040	Line number of the LVDS path ID0/1 line interrupt
VICAP LVDS LINE INT NUM ID2_3	0x0130	W	0x00400040	Line number of the LVDS path ID2/3 line interrupt
VICAP LVDS LINE CNT ID0_1	0x0134	W	0x00000000	Line count of the LVDS path ID0/1
VICAP LVDS LINE CNT ID2_3	0x0138	W	0x00000000	Line count of the LVDS path ID2/3
VICAP LVDS ID0 CROP START	0x013C	W	0x00000000	The start point of LVDS ID0 cropping



Name	Offset	Size	Reset Value	Description
VICAP LVDS ID1 CROP START	0x0140	W	0x00000000	The start point of LVDS ID1 cropping
VICAP LVDS ID2 CROP START	0x0144	W	0x00000000	The start point of LVDS ID2 cropping
VICAP LVDS ID3 CROP START	0x0148	W	0x00000000	The start point of LVDS ID3 cropping
VICAP LVDS SAV EAV A CT0 ID0	0x0150	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id0
VICAP LVDS SAV EAV B LK0 ID0	0x0154	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id0
VICAP LVDS SAV EAV A CT1 ID0	0x0158	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id0
VICAP LVDS SAV EAV B LK1 ID0	0x015C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id0
VICAP LVDS SAV EAV A CT0 ID1	0x0160	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id1
VICAP LVDS SAV EAV B LK0 ID1	0x0164	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id1
VICAP LVDS SAV EAV A CT1 ID1	0x0168	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id1
VICAP LVDS SAV EAV B LK1 ID1	0x016C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id1
VICAP LVDS SAV EAV A CT0 ID2	0x0170	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id2
VICAP LVDS SAV EAV B LK0 ID2	0x0174	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id2
VICAP LVDS SAV EAV A CT1 ID2	0x0178	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id2
VICAP LVDS SAV EAV B LK1 ID2	0x017C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id2
VICAP LVDS SAV EAV A CT0 ID3	0x0180	W	0x00000000	LVDS sync code of SAV_ACT0/EAV_ACT0 for id3
VICAP LVDS SAV EAV B LK0 ID3	0x0184	W	0x00000000	LVDS sync code of SAV_BLK0/EAV_BLK0 for id3
VICAP LVDS SAV EAV A CT1 ID3	0x0188	W	0x00000000	LVDS sync code of SAV_ACT1/EAV_ACT1 for id3
VICAP LVDS SAV EAV B LK1 ID3	0x018C	W	0x00000000	LVDS sync code of SAV_BLK1/EAV_BLK1 for id3
VICAP Y STAT CONTROL	0x0190	W	0x00000000	Y statistics control
VICAP Y STAT VALUE	0x0194	W	0x00000000	Y statistics value
VICAP MMU DTE ADDR	0x0800	W	0x00000000	MMU current page table address
VICAP MMU STATUS	0x0804	W	0x00000000	MMU status register
VICAP MMU COMMAND	0x0808	W	0x00000000	MMU command register
VICAP MMU PAGE FAULT ADDR	0x080C	W	0x00000000	MMU logical address of last page fault
VICAP MMU ZAP ONE LINE	0x0810	W	0x00000000	MMU Zap cache line register
VICAP MMU INT RAWSTAT	0x0814	W	0x00000000	MMU raw interrupt status register
VICAP MMU INT CLEAR	0x0818	W	0x00000000	MMU interrupt status clear
VICAP MMU INT MASK	0x081C	W	0x00000000	MMU interrupt mask
VICAP MMU INT STATUS	0x0820	W	0x00000000	MMU interrupt status

Name	Offset	Size	Reset Value	Description
VICAP MMU AUTO GATING	0x0824	W	0x00000000	MMU auto gating

Notes: **Size: B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 8.5.3 Detail Registers Description

#### **VICAP LVDS ID0 CTRL0**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_lvds_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when non-compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id0 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id0 Only be used when the sw_lvds_mode_id0=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id0 Only be used when the sw_lvds_mode_id0=3'b011. Choose the fid for id0.
25:24	RW	0x0	sw_lvds_main_lane_id0 Choose the lane to parse the sync code
23:20	RW	0x0	sw_lvds_lane_en_id0 Lane enable for id0. eg : 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id0 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserved
16	RW	0x0	sw_lvds_cap_en_id0 Enable to capture lvds id0. 1'b0: Disable 1'b1: Enable
15:0	RO	0x0000	reserved

#### **VICAP LVDS ID0 CTRL1**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id0 Width for id0.

#### **VICAP LVDS ID1 CTRL0**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_lvds_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when non-compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id1 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id1 Only be used when the sw_lvds_mode_id1=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id1 Only be used when the sw_lvds_mode_id1=3'b011. Choose the fid for id1.
25:24	RW	0x0	sw_lvds_main_lane_id1 Choose the lane to parse the sync code.
23:20	RW	0x0	sw_lvds_lane_en_id1 Lane enable for id1. Eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id1 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserved
16	RW	0x0	sw_lvds_cap_en_id1 Enable to capture lvds id1. 1'b0: Disable 1'b1: Enable
15:0	RO	0x0000	reserved

**VICAP LVDS ID1 CTRL1**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1.

**VICAP LVDS ID2 CTRL0**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_lvds_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id2 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted

Bit	Attr	Reset Value	Description
28	RW	0x0	sw_lvds_hdr_frame_id2 Only be used when the sw_lvds_mode_id2=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id2 Only be used when the sw_lvds_mode_id2=3'b011. Choose the fid for id2.
25:24	RW	0x0	sw_lvds_main_lane_id2 Choose the lane to parse the sync code
23:20	RW	0x0	sw_lvds_lane_en_id2 Lane enable for id2. eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id2 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserved
16	RW	0x0	sw_lvds_cap_en_id2 Enable to capture lvds id2. 1'b0: Disable 1'b1: Enable
15:0	RO	0x0000	reserved

**VICAP LVDS ID2 CTRL1**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2.

**VICAP LVDS ID3 CTRL0**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_lvds_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: High alignment(raw10/12 will in [15:6]/[15:4]) Only be used when compacted mode.
30	RO	0x0	reserved
29	RW	0x0	sw_lvds_compact_id3 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
28	RW	0x0	sw_lvds_hdr_frame_id3 Only be used when the sw_lvds_mode_id3=3'b010. 1'b0: 2 frames hdr 1'b1: 3 frames hdr
27:26	RW	0x0	sw_lvds_fid_id3 Only be used when the sw_lvds_mode_id3=3'b011. Choose the fid for id3.
25:24	RW	0x0	sw_lvds_main_lane_id3 Choose the lane to parse the sync code.

Bit	Attr	Reset Value	Description
23:20	RW	0x0	sw_lvds_lane_en_id3 Lane enable for id3. Eg: 4'b0011 represent lane 0/1 is enable.
19:17	RW	0x0	sw_lvds_mode_id3 There are 4 modes. 3'b000: Ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 3'b001: Fs-le...ls-fe 3'b010: Sony dol hdr pattern 1 3'b011: Sony dol hdr pattern 2 other: Reserved
16	RW	0x0	sw_lvds_cap_en_id3 Enable to capture lvds id3. 1'b0: Disable 1'b1: Enable
15:0	RO	0x0000	reserved

**VICAP LVDS ID3 CTRL1**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3.

**VICAP LVDS CTRL**

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_dma_idle 1'b0: Not idle 1'b1: Idle LVDS path dma transport
15	RO	0x0	reserved
14:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11	RO	0x0	reserved
10:9	RW	0x0	sw_lvds_width 2'b00: 8bit 2'b01: 10bit 2'b10: 12bit
8:7	RO	0x0	reserved
6:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%
0	RW	0x1	sw_water_line_en 1'b0: Disable water line 1'b1: Enable water line

**VICAP LVDS FRAME0 ADDR Y ID0**

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 path(must be aligned to double word).

**VICAP LVDS FRAME1 ADDR Y ID0**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

**VICAP LVDS FRAME0 VLW Y ID0**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id0 Virtual line width of even frame for ID0 path(must be aligned to double word).

**VICAP LVDS FRAME1 VLW Y ID0**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id0 Virtual line width of odd frame for ID0 path(must be aligned to double word).

**VICAP LVDS FRAME0 ADDR Y ID1**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 path(must be aligned to double word).

**VICAP LVDS FRAME1 ADDR Y ID1**

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 path(must be aligned to double word).

**VICAP LVDS FRAME0 VLW Y ID1**

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id1 Virtual line width of even frame for ID1 path(must be aligned to double word).

**VICAP LVDS FRAME1 VLW Y ID1**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id1 Virtual line width of odd frame for ID1 path(must be aligned to double word).

**VICAP LVDS FRAME0 ADDR Y ID2**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 path(must be aligned to double word).

**VICAP LVDS FRAME1 ADDR Y ID2**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 path(must be aligned to double word).

**VICAP LVDS FRAME0 VLW Y ID2**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id2 Virtual line width of even frame for ID2 path(must be aligned to double word).

**VICAP LVDS FRAME1 VLW Y ID2**

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id2 Virtual line width of odd frame for ID2 path(must be aligned to double word).

**VICAP LVDS FRAME0 ADDR Y ID3**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 path(must be aligned to double word).

**VICAP LVDS FRAME1 ADDR Y ID3**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 path(must be aligned to double word).

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 path(must be aligned to double word).

**VICAP LVDS FRAME0 VLW Y ID3**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id3 Virtual line width of even frame for ID3 path(must be aligned to double word).

**VICAP LVDS FRAME1 VLW Y ID3**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id0 Virtual line width of odd frame for ID3 path(must be aligned to double word).

**VICAP LVDS INTEN**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	dma_lvds_id3_fifo_overflow_inten Enable the interrupt of dma fifo overflow of lvds id3 path. 1'b0: Disable 1'b1: Enable
25	RW	0x0	dma_lvds_id2_fifo_overflow_inten Enable the interrupt of dma fifo overflow of lvds id2 path. 1'b0: Disable 1'b1: Enable
24	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable
20	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	config_fifo_overflow_inten 1'b0: Disable 1'b1: Enable



Bit	Attr	Reset Value	Description
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

**VICAP LVDS INTSTAT**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	W1 C	0x0	dma_lvds_id3_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
25	W1 C	0x0	dma_lvds_id2_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
24	RW	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
23	RW	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
22	RW	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
21	RW	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1 C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1 C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1 C	0x0	config_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
17	W1 C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
16	W1 C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1 C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1 C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1 C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1 C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1 C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1 C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1 C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1 C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1 C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1 C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1 C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1 C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1 C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1 C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1 C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1 C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

**VICAP LVDS LINE INT NUM ID0 1**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 If line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15:14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 If line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

**VICAP LVDS LINE INT NUM ID2 3**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 If line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15:14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 If line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

**VICAP LVDS LINE CNT ID0 1**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	line_cnt_id0 Current line count for id0.

**VICAP LVDS LINE CNT ID2 3**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	line_cnt_id2 Current line count for id2.

**VICAP LVDS ID0 CROP START**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0.

**VICAP LVDS ID1 CROP START**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1.

**VICAP LVDS ID2 CROP START**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2.

**VICAP LVDS ID3 CROP START**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3.

**VICAP LVDS SAV EAV ACT0 ID0**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id0 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id0 LVDS path sync code of sav_act0.

**VICAP LVDS SAV EAV BLK0 ID0**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id0 LVDS path sync code of eav_blk0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id0 LVDS path sync code of sav_blk0.

**VICAP LVDS SAV EAV ACT1 ID0**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id0 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_lvds_sav_act1_id0 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID0**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id0 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id0 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT0 ID1**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id1 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id1 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK0 ID1**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id1 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id1 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT1 ID1**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id1 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id1 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID1**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id1 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id1 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT0 ID2**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id2 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id2 LVDS path sync code of sav_act0.

**VICAP LVDS SAV EAV BLK0 ID2**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id2 LVDS path sync code of eav_blk0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id2 LVDS path sync code of sav_blk2.

**VICAP LVDS SAV EAV ACT1 ID2**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id2 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id2 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID2**

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id2 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id2 LVDS path sync code of sav_blk1.

**VICAP LVDS SAV EAV ACT0 ID3**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act0_id3 LVDS path sync code of eav_act0.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act0_id3 LVDS path sync code of sav_act0.

**VICAP LVDS SAV EAV BLK0 ID3**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk0_id3 LVDS path sync code of eav_blk0.

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk0_id3 LVDS path sync code of sav_blk0.

**VICAP LVDS SAV EAV ACT1 ID3**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act1_id3 LVDS path sync code of eav_act1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act1_id3 LVDS path sync code of sav_act1.

**VICAP LVDS SAV EAV BLK1 ID3**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk1_id3 LVDS path sync code of eav_blk1.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk1_id3 LVDS path sync code of sav_blk1.

**VICAP Y STAT CONTROL**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:26	RW	0x00	sw_black_level_b Black level for B channel.
25:21	RW	0x00	sw_black_level_g Black level for G channel.
20:16	RW	0x00	sw_black_level_r Black level for R channel.
15:14	RO	0x0	reserved
13:12	RO	0x0	ro_block_id2 The number of block of id2.
11:10	RO	0x0	ro_block_id1 The number of block of id1.
9:8	RO	0x0	ro_block_id0 The number of block of id0.
7:6	WO	0x0	sw_y_stat_rd_block Point to the specified block.
5:4	WO	0x0	sw_y_stat_rd_id 2'b00: Point to ID0 2'b01: Point to ID1 2'b10: Point to ID2 2'b11: Reserved
3	WO	0x0	sw_y_stat_rd Change the y statistics read pointer according to sw_y_stat_rd_id/sw_y_stat_rd_block.



Bit	Attr	Reset Value	Description
2:1	RW	0x0	sw_bayer_pattern 2'b00: RGGB 2'b01: GRBG 2'b10: GBRG 2'b11: BGGR
0	RW	0x0	sw_y_stat_en 1'b0: Disable y statistics 1'b1: Enable y statistics

**VICAP Y STAT VALUE**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_y_stat_value Y statistics value.

**VICAP MMU DTE ADDR**

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address.

**VICAP MMU STATUS**

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	paging_enabled Paging is enabled.

**VICAP MMU COMMAND**

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE

**VICAP MMU PAGE FAULT ADDR**

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

**VICAP MMU ZAP ONE LINE**

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

**VICAP MMU INT RAWSTAT**

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

**VICAP MMU INT CLEAR**

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error.
0	WO	0x0	page_fault Page fault.

**VICAP MMU INT MASK**

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

**VICAP MMU INT STATUS**

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error.

Bit	Attr	Reset Value	Description
0	RO	0x0	page_fault Page fault.

**VICAP MMU AUTO GATING**

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self

**8.6 Interface Description**

Table 8-1 VICAP Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
vicap_clkout	O	CIF_CLKOUT_M0/RGMII_TXCLK_M0/ UART3_TX_M0/GPIO3_C6_d	GRF_GPIO3C_IOMUX_H[11:8]=0x1
	O	LCDC_D21/RGMII_TXD2_M1/CIF_CLK OUT_M1/I2S1_SCLK_M2/GPIO2_D1_ d	GRF_GPIO2D_IOMUX_L[7:4]=0x3
vicap_clkin	I	CIF_CLKIN_M0/CLK_OUT_ETHERNET M0/UART3_CTSN_M0/GPIO3_C5_d	GRF_GPIO3C_IOMUX_H[7:4]=0x1
	I	LCDC_D22/RGMII_TXCLK_M1/CIF_CL KIN_M1/I2S1_LRCK_M2/GPIO2_D2_d	GRF_GPIO2D_IOMUX_L[11:8]=0x3
vicap_href	I	CIF_HSYNC_M0/RGMII_RXCLK_M0/U ART3_RX_M0/GPIO3_C7_d	GRF_GPIO3C_IOMUX_H[15:12]=0x1
	I	LCDC_D23/RGMII_RXCLK_M1/CIF_H SYNC_M1/I2S1_SDI_M2/GPIO2_D3_ d	GRF_GPIO2D_IOMUX_L[15:12]=0x3
vicap_vsync	I	CIF_VSYNC_M0/RGMII_MDC_M0/UAR T3_RTSN_M0/GPIO3_C4_d	GRF_GPIO3C_IOMUX_H[3:0]=0x1
	I	LCDC_D20/RGMII_RXD3_M1/CIF_VS YNC_M1/I2S1_SDO_M2/GPIO2_D0_d	GRF_GPIO2D_IOMUX_L[3:0]=0x3
vicap_data0	I	CIF_D0_M0/I2S0_SCLK_TX_M1/UART 4_TX_M0/I2C3_SCL_M0/PWM8_M0/G PIO3_A4_d	GRF_GPIO3A_IOMUX_H[3:0]=0x1
	I	LCDC_D0/RGMII_TXD3_M1/CIF_D0_ M1/UART4_RTSN_M1/GPIO2_A4_d	GRF_GPIO2A_IOMUX_H[3:0]=0x3
vicap_data1	I	CIF_D1_M0/RGMII_CRS_M0/I2S0_LR CK_TX_M1/UART4_RX_M0/I2C3_SDA M0/PWM9_M0/GPIO3_A5_d	GRF_GPIO3A_IOMUX_H[7:4]=0x1
	I	LCDC_D1/RGMII_CRS_M1/CIF_D1_M 1/UART4_CTSN_M1/I2C5_SCL_M0/G PIO2_A5_d	GRF_GPIO2A_IOMUX_H[7:4]=0x3
vicap_data2	I	CIF_D2_M0/RGMII_COL_M0/I2S0_SD O0_M1/UART5_TX_M0/CAN_RXD_M1 /PWM10_M0/GPIO3_A6_d	GRF_GPIO3A_IOMUX_H[11:8]=0x1
	I	LCDC_D2/RGMII_COL_M1/CIF_D2_M 1/UART4_TX_M1/PWM5_M1/GPIO2_A 6_d	GRF_GPIO2A_IOMUX_H[11:8]=0x3
vicap_data3	I	CIF_D3_M0/RGMII_RXD2_M0/I2S0_S DIO_M1/UART5_RX_M0/CAN_TXD_M 1/PWM11_IR_M0/GPIO3_A7_d	GRF_GPIO3A_IOMUX_H[15:12]=0x1
	I	LCDC_D7/I2S2_MCLK_M1/CIF_D3_M 1/UART5_CTSN_M1/PWM0_M1/SPI0_ CS1N_M2/I2C5_SDA_M0/GPIO2_B3_ d	GRF_GPIO2B_IOMUX_L[15:12]=0x3
vicap_data4	I	CIF_D4_M0/RGMII_RXD3_M0/I2S0_ MCLK_M1/UART5_RTSN_M0/I2C5_SC L_M1/GPIO3_B0_d	GRF_GPIO3B_IOMUX_L[3:0]=0x1
	I	LCDC_D8/RGMII_RXDV_M1/CIF_D4_ M1/GPIO2_B4_d	GRF_GPIO2B_IOMUX_H[3:0]=0x3
vicap_data5	I	CIF_D5_M0/RGMII_TXD2_M0/I2S0_S CLK_RX_M1/UART5_CTSN_M0/I2C5_ SDA_M1/GPIO3_B1_d	GRF_GPIO3B_IOMUX_L[7:4]=0x1

Module Pin	Dir	Pin Name	IOMUX Setting
	I	LCDC_D9/RGMII_RXD0_M1/CIF_D5_M1/GPIO2_B5_d	GRF_GPIO2B_IOMUX_SEL_H[7:4]=0x3
vicap_data6	I	CIF_D6_M0/RGMII_TXD3_M0/I2S0_LRCK_RX_M1/UART4_RTSN_M0/GPIO3_B2_d	GRF_GPIO3B_IOMUX_L[11:8]=0x1
	I	LCDC_D10/RGMII_RXD1_M1/CIF_D6_M1/GPIO2_B6_d	GRF_GPIO2B_IOMUX_H[11:8]=0x3
vicap_data7	I	CIF_D7_M0/RGMII_TXD0_M0/I2S0_SDO1_SDI3_M1/UART4_CTSN_M0/GPIO3_B3_d	GRF_GPIO3B_IOMUX_L[15:12]=0x1
	I	LCDC_D11/RGMII_CLK_M1/CIF_D7_M1/GPIO2_B7_d	GRF_GPIO2B_IOMUX_H[15:12]=0x3
vicap_data8	I	CIF_D8_M0/RGMII_TXD1_M0/I2S0_SDO2_SDI2_M1/SPI1_CS1N_M0/GPIO3_B4_d	GRF_GPIO3B_IOMUX_H[3:0]=0x1
	I	LCDC_D12/RGMII_RXER_M1/CIF_D8_M1/GPIO2_C0_d	GRF_GPIO2C_IOMUX_L[3:0]=0x3
vicap_data9	I	CIF_D9_M0/RGMII_TXEN_M0/I2S0_SDO3_SDI1_M1/SPI1_CS0N_M0/GPIO3_B5_d	GRF_GPIO3B_IOMUX_H[7:4]=0x1
	I	LCDC_D13/RGMII_MDIO_M1/CIF_D9_M1/GPIO2_C1_d	GRF_GPIO2C_IOMUX_L[7:4]=0x3
vicap_data10	I	CIF_D10_M0/RGMII_RXD0_M0/PDM_SDI2_M1/SPI1_MOSI_M0/GPIO3_B6_d	GRF_GPIO3B_IOMUX_H[11:8]=0x1
	I	LCDC_D14/RGMII_MDC_M1/CIF_D10_M1/GPIO2_C2_d	GRF_GPIO2C_IOMUX_L[11:8]=0x3
vicap_data11	I	CIF_D11_M0/RGMII_RXD1_M0/PDM_SDI3_M1/SPI1_MISO_M0/GPIO3_B7_d	GRF_GPIO3B_IOMUX_H[15:12]=0x1
	I	LCDC_D15/RGMII_TXD0_M1/CIF_D11_M1/GPIO2_C3_d	GRF_GPIO2C_IOMUX_L[15:12]=0x3
vicap_data12	I	CIF_D12_M0/RGMII_CLK_M0/PDM_CLK0_M1/SPI1_CLK_M0/GPIO3_C0_d	GRF_GPIO3C_IOMUX_L[3:0]=0x1
	I	LCDC_D16/RGMII_TXD1_M1/CIF_D12_M1/GPIO2_C4_d	GRF_GPIO2C_IOMUX_H[3:0]=0x3
vicap_data13	I	CIF_D13_M0/RGMII_RXDV_M0/PDM_SDI0_M1/GPIO3_C1_d	GRF_GPIO3C_IOMUX_L[7:4]=0x1
	I	LCDC_D17/CLK_OUT_ETHERNET_M1/CIF_D13_M1/GPIO2_C5_d	GRF_GPIO2C_IOMUX_H[7:4]=0x3
vicap_data14	I	CIF_D14_M0/RGMII_RXER_M0/PDM_SDI1_M1/GPIO3_C2_d	GRF_GPIO3C_IOMUX_L[11:8]=0x1
	I	LCDC_D18/RGMII_TXEN_M1/CIF_D14_M1/GPIO2_C6_d	GRF_GPIO2C_IOMUX_H[11:8]=0x3
vicap_data15	I	CIF_D15_M0/RGMII_MDIO_M0/PDM_CLK1_M1/GPIO3_C3_d	GRF_GPIO3C_IOMUX_L[15:12]=0x1
	I	LCDC_D19/RGMII_RXD2_M1/CIF_D15_M1/I2S1_MCLK_M2/GPIO2_C7_d	GRF_GPIO2C_IOMUX_H[15:12]=0x3

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

## 8.7 Application Notes

### 8.7.1 DVP receiving Application

The most important configuration requirement of all operations is the DVP\_CAP\_EN bit must be set after all the mode selection is ready. The configuration order of the input/output data format, YUV order, the address, frame size/width, AXI burst length and other options do not need to care.

There are many debug registers to make it easy to read the internal operation information of VICAP. The line number of last frame and the pixel number of last line can be known by read the DVP\_LAST\_LINE and DVP\_LAST\_PIX.

If 1/2/4 mixed BT656/BT1120 is received, sw\_multi\_id\_en/sw\_multi\_id\_mode must be configured. And sw\_chid\_idx/sw\_chid\_bit\_en\_idx should be configured according the

encoding rules. Eg: the different videos are distinguished by the [3:2] bits in sync code, so we can configure `sw_chid_bit_en_idx=4'b1100`.

If M1 interface is connected, `GRF_IOFUNC_CON1[0]` should be configured to 1.

If DVP data is double edge sampling, `GRF_CIFIO_CON[8]` should be configured to 1. And the user can adjust the clock phase by `GRF_CIFIO_CON[7:0]`.

### **8.7.2 MIPI receiving Application**

VICAP support receiving up to four MIPI IDs at the same time. VICAP could receive all ID value via configuring the `sw_vc_id0/1/2/3` and `sw_dt_id0/1/2/3`, but VICAP could only transform MIPI data to RAW8/10/12, RGB888, YUV422SP, YUV420SP, YUV400 via configuring the `sw_wrddr_type`. The register `sw_height` must be same as the received image, and the register `sw_width` is useless when `sw_crop_en` is disable. If `sw_wrddr_type` is rgb888, then the `sw_width` and `sw_start_x` are equal to the number of bytes.

There are two mipi rx paths in RV1109/RV1126. If the user want to receive from dphy1 by VICAP, the `GRF_IOFUNC_CON3[9]` must be configured to 1.

If AXI bus is too busy to transfer sensor data, you can enable `sw_hurry_en/sw_press_en` and `sw_water_line_en`.

### **8.7.3 LVDS receiving Application**

VICAP/VICAP\_LITE support receiving up to four LVDS IDs at the same time. The sync code register (`sw_lvds_sav_act0_id0,sw_lvds_eav_act0_id0...`) must be configured correctly by the user. There are four LVDS sync mode can be selected by `sw_lvds_mode_idx`. Mode0: ls-le...fs-fe or sav\_act-eav\_act...sav\_blk-eav\_blk. Mode1:fs-le...ls-fe. Mode2: sony dol hdr pattern 1. Mode3:sony dol hdr pattern 2. And if the mode is mode2, the user also need configure the register `sw_lvds_hdr_frame_idx`. If the mode is mode3, the user also need configure the register `sw_lvds_fid_idx`.

The register `sw_mipi_lvds_sel` must be configured to 1.

There are two LVDS rx paths in RV1109/RV1126. If the user want to receive from dphy1 by VICAP/VICAP\_LITE, the `GRF_IOFUNC_CON3[9]/GRF_IOFUNC_CON3[11]` must be configured to 1.

## Chapter 9 MIPI CSI DPHY

### 9.1 Overview

The features of MIPI CSI DPHY are as follow:

- Analog mixed-signal hard-macro LP/HS Receiver solution
- Designed to MIPI v1.2 Specifications
- Integrated PHY Protocol Interface(PPI) interfaces to DSI/CSI and UniPro MIPI protocols
- 2.5 Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 10 Gbps transfer rate
- HS-RX, LP-RX, LP-TX and Calibration supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- LOW-Power dissipation: less than 1.5mA/Lane in D-PHY HS RX mode
- Buffers with tunable On-Die-Termination
- Includes embedded ESD, boundary scan and BIST
- SubLVDS/LVDS supported, up to 1Gbps data transfer rate per lane

### 9.2 Block Diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane types. The requirements for the 'Control and Interface Logic'(CIL) function depend on the Lane type and Lane side.

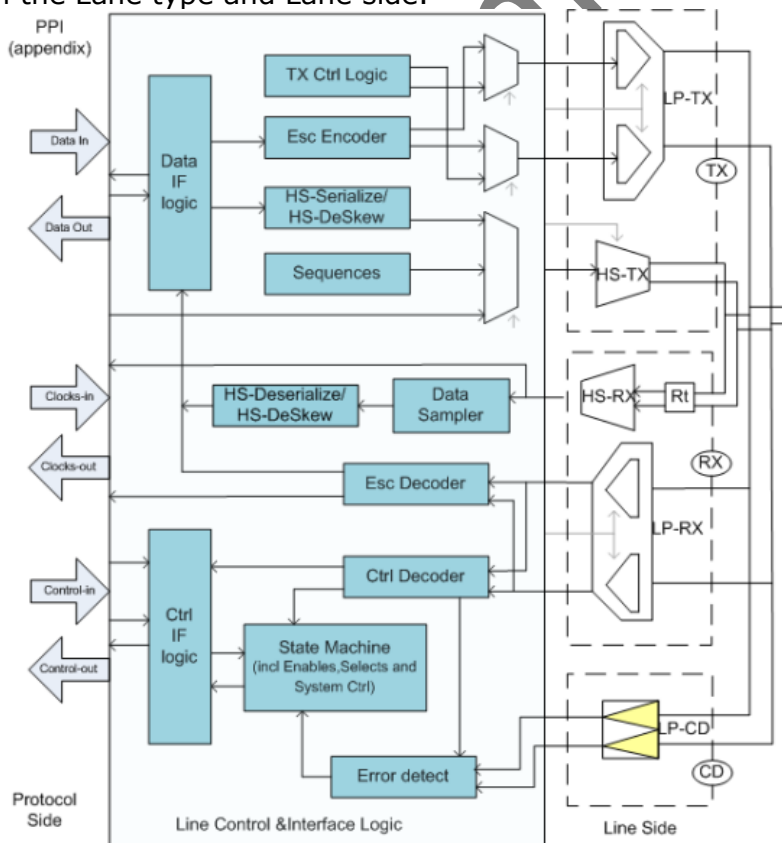


Fig. 9-1 MIPI CSI DPHY Block Diagram

### 9.3 Register Description

#### 9.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

#### 9.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DPHYRX_LANE_EN	0x0000	W	0x00000000	Clk/data lane enable
DPHYRX_DIGITAL_CLK_PHASE	0x0034	W	0x00000000	Digital clock phase
DPHYRX_LANE_CLK_3_PHASE	0x0038	W	0x00000000	Lane clock/3 phase
DPHYRX_LANE_2_1_0_PHASE	0x003C	W	0x00000000	Data lane 2/1/0 phase
DPHYRX_DIGITAL_CLK_REVERSE	0x0048	W	0x00000000	Digital clock reverse
DPHYRX_MIPI_LVDS_ENABLE	0x0080	W	0x00000000	MIPI/LVDS enable
DPHYRX_LANE_CK_MODE	0x0128	W	0x00000000	Clock lane mode
DPHYRX_LANE_CK_MSB	0x0138	W	0x00000000	MSB enable
DPHYRX_LANE_CK_TTAGO	0x0140	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_CK_TTASURE	0x0144	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_CK_TTAWAIT	0x0148	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_CK_THSSETTLE	0x0160	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_CK_CAL_EN	0x0168	W	0x00000000	Calibration reception enable
DPHYRX_LANE_0_MSB	0x01B8	W	0x00000000	MSB enable
DPHYRX_LANE_0_TTAGO	0x01C0	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_0_TTASURE	0x01C4	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_0_TTAWAIT	0x01C8	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_0_THSSETTLE	0x01E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_0_CAL_EN	0x01E8	W	0x00000000	Calibration reception enable
DPHYRX_LANE_1_MSB	0x0238	W	0x00000000	MSB enable
DPHYRX_LANE_1_TTAGO	0x0240	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_1_TTASURE	0x0244	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_1_TTAWAIT	0x0248	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_1_THSSETTLE	0x0260	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_1_CAL_EN	0x0268	W	0x00000000	Calibration reception enable
DPHYRX_LANE_2_MSB	0x02B8	W	0x00000000	MSB enable
DPHYRX_LANE_2_TTAGO	0x02C0	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_2_TTASURE	0x02C4	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_2_TTAWAIT	0x02C8	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_MIPI_LVDS_MODEL	0x02CC	W	0x00000064	MIPI/LVDS model enable

Name	Offset	Size	Reset Value	Description
DPHYRX_LANE_2_THSSETTLE	0x02E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_2_CAL_EN	0x02E8	W	0x00000000	Calibration reception enable
DPHYRX_LVDS_MODE	0x0300	W	0x00000000	LVDS mode
DPHYRX_LANE_3_MSB	0x0338	W	0x00000000	MSB enable
DPHYRX_LANE_3_TTAGO	0x0340	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_3_TTASUR	0x0344	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_3_TTAWAIT	0x0348	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_3_THSSETTLE	0x0360	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_3_CAL_EN	0x0368	W	0x00000000	Calibration reception enable

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 9.3.3 Detail Registers Description

#### DPHYRX\_LANE\_EN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	reserved
6	RW	0x0	lane_en_ck Enable D-PHY clock lane:active high.
5	RW	0x0	lane_en_3 Enable D-PHY lane3:active high.
4	RW	0x0	lane_en_2 Enable D-PHY lane2:active high.
3	RW	0x0	lane_en_1 Enable D-PHY lane1:active high.
2	RW	0x0	lane_en_0 Enable D-PHY lane0:active high.
1:0	RO	0x0	reserved

#### DPHYRX\_DIGITAL\_CLK\_PHASE

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	digital_clk_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

#### DPHYRX\_LANE\_CLK\_3\_PHASE

Address: Operational Base + offset (0x0038)



Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	lane_clk_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
3:1	RW	0x0	lane_3_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
0	RW	0x0	lane_2_phase_msb See lane_2_phase for the details of the register.

**DPHYRX LANE 2 1 0 PHASE**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7:6	RW	0x0	lane_2_phase lane_2_phase_msb, lane_2_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
5:3	RW	0x0	lane_1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

Bit	Attr	Reset Value	Description
2:0	RW	0x0	lane_0_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

**DPHYRX DIGITAL CLK REVERSE**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	digital_clk_reverse 1'b0: Make the digital sample clock positive(default value) 1'b1: Reverse the digital sample clock
6:0	RO	0x00	reserved

**DPHYRX MIPI LVDS ENABLE**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	lvds_reg_en 1'b0: Disable 1'b1: Enable
4:1	RO	0x0	reserved
0	RW	0x1	mipi_en 1'b0: Disable 1'b1: Enable

**DPHYRX LANE CK MODE**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

**DPHYRX LANE CK MSB**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_ck_msb MSB enable for pin_rxdats_*
5:0	RO	0x00	reserved

**DPHYRX LANE CK TTAGO**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

**DPHYRX LANE CK TTASURE**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

**DPHYRX LANE CK TTAWAIT**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHYRX LANE CK THSSETTLE**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_ck_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI)    Value(HEX) 80-110MHz            02 110-150MHz           03 150-200MHz           06 200-250MHz           06 250-300MHz           06 300-400MHz           08 400-500MHz           0b 500-600MHz           0e 600-700MHz           10 700-800MHz           12 800-1000MHz           16 1000-1200MHz           1e 1200-1400MHz           23 1400-1600MHz           2d 1600-1800MHz           32 1800-2000MHz           37 2000-2200MHz           3c 2200-2400MHz           41 2400-2500MHz           46

**DPHYRX LANE CK CAL EN**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

**DPHYRX LANE 0 MSB**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_0_msb MSB enable for pin_rxdahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

**DPHYRX LANE 0 TTAGO**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_0_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

**DPHYRX LANE 0 TTASURE**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_0_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

**DPHYRX LANE 0 TTAWAIT**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHYRX LANE 0 THSSETTLE**

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_0_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI)    Value(HEX) 80-110MHz            02 110-150MHz          03 150-200MHz          06 200-250MHz          06 250-300MHz          06 300-400MHz          08 400-500MHz          0b 500-600MHz          0e 600-700MHz          10 700-800MHz          12 800-1000MHz        16 1000-1200MHz       1e 1200-1400MHz       23 1400-1600MHz       2d 1600-1800MHz       32 1800-2000MHz       37 2000-2200MHz       3c 2200-2400MHz       41 2400-2500MHz       46

**DPHYRX LANE 0 CAL EN**

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_0_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

**DPHYRX LANE 1 MSB**

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_1_msb MSB enable for pin_rxdaths_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

**DPHYRX LANE 1 TTAGO**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

**DPHYRX LANE 1 TTASURE**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

**DPHYRX LANE 1 TTAWAIT**

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHYRX LANE 1 THSSETTLE**

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI)    Value(HEX) 80-110MHz            02 110-150MHz          03 150-200MHz          06 200-250MHz          06 250-300MHz          06 300-400MHz          08 400-500MHz          0b 500-600MHz          0e 600-700MHz          10 700-800MHz          12 800-1000MHz        16 1000-1200MHz       1e 1200-1400MHz       23 1400-1600MHz       2d 1600-1800MHz       32 1800-2000MHz       37 2000-2200MHz       3c 2200-2400MHz       41 2400-2500MHz       46

**DPHYRX LANE 1 CAL EN**

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x0000000	reserved
7	RW	0x0	lane_1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

**DPHYRX LANE 2 MSB**

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_2_msb MSB enable for pin_rxdats_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

**DPHYRX LANE 2 TTAGO**

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_2_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

**DPHYRX LANE 2 TTASURE**

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_2_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

**DPHYRX LANE 2 TTAWAIT**

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_2_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHYRX MIPI LVDS MODEL**

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	lvds_model_en 1'b0: Disable 1'b1: Enable
1	RW	0x1	mipi_model_en 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

**DPHYRX LANE 2 THSETTLE**

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_2_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI)      Value(HEX) 80-110MHz              02 110-150MHz            03 150-200MHz            06 200-250MHz            06 250-300MHz            06 300-400MHz            08 400-500MHz            0b 500-600MHz            0e 600-700MHz            10 700-800MHz            12 800-1000MHz           16 1000-1200MHz          1e 1200-1400MHz          23 1400-1600MHz          2d 1600-1800MHz          32 1800-2000MHz          37 2000-2200MHz          3c 2200-2400MHz          41 2400-2500MHz          46

**DPHYRX LANE 2 CAL EN**

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_2_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

**DPHYRX LVDS MODE**

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lvds_mode 2'b00: 10bit mode 2'b01: 12bit mode 2'b10: 8bit mode
3:1	RO	0x0	reserved
0	RW	0x0	lvds_en 1'b0: Disable 1'b1: Enable

**DPHYRX LANE 3 MSB**

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved



Bit	Attr	Reset Value	Description
6	RW	0x0	lane_3_msb MSB enable for pin_rxdats_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

**DPHYRX LANE 3 TTAGO**

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_3_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

**DPHYRX LANE 3 TTASURE**

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_3_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

**DPHYRX LANE 3 TTAWAIT**

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

**DPHYRX LANE 3 THSETTLE**

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_3_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI)      Value(HEX) 80-110MHz              02 110-150MHz            03 150-200MHz            06 200-250MHz            06 250-300MHz            06 300-400MHz            08 400-500MHz            0b 500-600MHz            0e 600-700MHz            10 700-800MHz            12 800-1000MHz           16 1000-1200MHz          1e 1200-1400MHz          23 1400-1600MHz          2d 1600-1800MHz          32 1800-2000MHz          37 2000-2200MHz          3c 2200-2400MHz          41 2400-2500MHz          46

**DPHYRX LANE 3 CAL EN**

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_3_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

**9.4 Application Notes**

There two D-PHY RX in RV1109/RV1126, the following is the D-PHY0 4lane example.

**9.4.1 MIPI Mode Application**

step1: send 0x7d to register LANE\_EN. Enable the D-PHY.

step2: send 0x03f003f0 to register GRF\_CSIPHY0\_CON.

**9.4.2 LVDS Mode Application**

step1: send 0x7d to register LANE\_EN. Enable the D-PHY.

step2: send 0x3e to register MIPI\_LVDS\_ENABLE. Disable MIPI internal logical and switch to LVDS bank.

step3: send 0x04 to register MIPI\_LVDS\_MODEL. Enable LVDS mode.

step4: send 0x0f/0x1f/0x2f to register LVDS\_MODE. Enable LVDS internal logical and select 10bit/12bit/8bit mode.

step5: send 0x01f001f0 to register GRF\_CSIPHY0\_CON.

## Chapter 10 MIPI CSI HOST

### 10.1 Overview

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY configured as a Slave acts as the physical layer.

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY following PHY Protocol Interface, as defined in "MIPI Alliance Specification for D-PHY, Version 1.1-7 November 2011"
- Up to four D-PHY RX data lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
  - RGB, YUV, and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction
  - PHY level
  - Packet level
  - Line level
  - Frame level
- Support DSI video mode/command mode

### 10.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

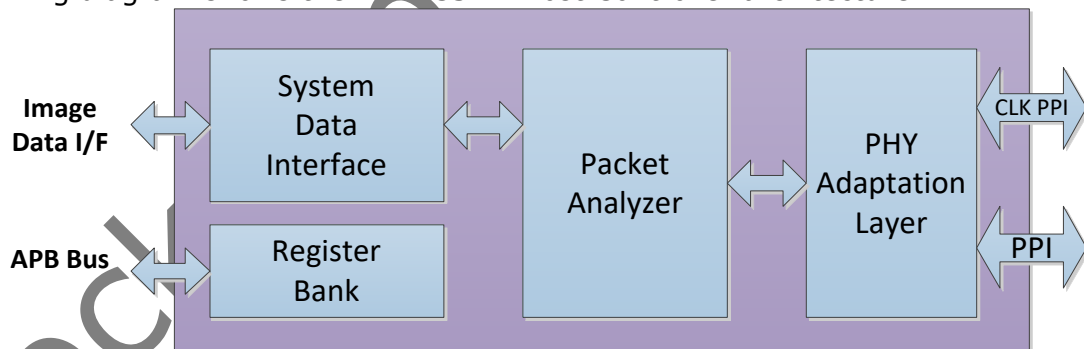


Fig. 10-1 MIPI CSI-2 Host Controller Architecture

- **PHY Adaptation Layer:** Manages the D-PHY PPI interface
- **Packet Analyzer:** Merges the data from the different lanes
- **Image Data Interface:** Reorders pixels into 32-bit data for memory storage and generates timing accurate video synchronization signals
- **AMBA-APB Register Bank:** Provides access to configuration and control registers

### 10.3 Function Description

#### 10.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the minimum number of lanes that support a specific CSI-2 device.

Following table presents some predefined and supported camera settings, assuming the

following:

- Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.
- No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of following table presents the minimum number of lanes required for each configuration.

Table 10-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY at 1 Gbps Number of Lanes	D-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
<b>Video Formats</b>						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

### 10.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

- Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End
- Line errors such as incorrect line sequence and mismatch between Line Start and Line End
- Packet errors such as ECC or CRC mismatch
- D-PHY errors such as synchronization pattern mismatch

Following table shows all the errors that CSI-2 Host Controller can identify.

Table 10-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface
phy_erresc_*	Escape entry error (ULPM) on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

Error	Description	Level	Action
phy_errsoths_*	Start of transmission error on data lane* but synchronization can still be achieved	PHY	Informative only since PHY can recover from this error. Error is acknowledged in register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packets	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packets	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packets	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packets	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_mismatch_vc*	Error matching Frame Start with Frame End for virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_vc*	Last received frame, in virtual channel*, had at least one CRC error	Frame	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

## 10.4 Register Description

### 10.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 10.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI2HOST_VERSION	0x0000	W	0x00000000	Controller version identification
CSI2HOST_N_LANES	0x0004	W	0x00000000	Number of active data lanes
CSI2HOST_CSI2_RESETN	0x0010	W	0x00000000	CSI2 controller reset
CSI2HOST_PHY_STATE	0x0014	W	0x00000000	General settings for all blocks
CSI2HOST_DATA_IDS_1	0x0018	W	0x00000000	Data IDS for which IDI reports line boundary matching errors
CSI2HOST_DATA_IDS_2	0x001C	W	0x00000000	Data IDS for which IDI reports line boundary matching errors
CSI2HOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSI2HOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSI2HOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSI2HOST_MSK2	0x002C	W	0x00000000	Masks for errors 2

Name	Offset	Size	Reset Value	Description
CSI2HOST_CONTROL	0x0040	W	0x0C204000	Control

Notes: **Size: B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 10.4.3 Detail Registers Description

#### CSI2HOST\_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	version Version of the csi2host.

#### CSI2HOST\_N\_LANES

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	n_lanes Number of active data lanes. 2'b00: 1 data lane(lane 0) 2'b01: 2 data lanes(lane0 and 1) 2'b10: 3 data lanes(lane0,1,and 2) 2'b11: 4 data lanes(ALL) Can only be updated when the D-PHY lane is in the Stop state.

#### CSI2HOST\_CSI2\_RESETN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	csi2_rese CSI2 controller reset output. Active low.

#### CSI2HOST\_PHY\_STATE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x000000	reserved
11	RW	0x0	bypass_2ecc_tst Payload Bypass test mode for double ECC errors.
10	RO	0x0	phy_stopstateclk Clock lane in Stop state.
9	RO	0x0	phy_rxulpsclknot This signal indicates that the clock lane module has entered the Ultra Low Power state. Active low.
8	RO	0x0	phy_rxclkactivehs Indicates that the clock lane is actively receiving a DDR clock.
7	RO	0x0	phy_stopstatedata_3 Data lane 3 in Stop state.
6	RO	0x0	phy_stopstatedata_2 Data lane 2 in Stop state.
5	RO	0x0	phy_stopstatedata_1 Data lane 1 in Stop state.

Bit	Attr	Reset Value	Description
4	RO	0x0	phy_stopstatedata_0 Data lane 0 in Stop state.
3	RO	0x0	phy_rxulpsesc_3 Lane module0 has entered the Ultra Low Power mode.
2	RO	0x0	phy_rxulpsesc_2 Lane module2 has entered the Ultra Low Power mode.
1	RO	0x0	phy_rxulpsesc_1 Lane module1 has entered the Ultra Low Power mode.
0	RO	0x0	phy_rxulpsesc_0 Lane module0 has entered the Ultra Low Power mode.

**CSI2HOST DATA IDS 1**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	di3_vc Data ID 3 virtual channel.
29:24	RW	0x00	di3_dt Data ID 3 data type.
23:22	RW	0x0	di2_vc Data ID 2 virtual channel.
21:16	RW	0x00	di2_dt Data ID 2 data type.
15:14	RW	0x0	di1_vc Data ID 1 virtual channel.
13:8	RW	0x00	di1_dt Data ID 1 data type.
7:6	RW	0x0	di0_vc Data ID 0 virtual channel.
5:0	RW	0x00	di0_dt Data ID 0 data type.

**CSI2HOST DATA IDS 2**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	di7_vc Data ID 7 virtual channel.
29:24	RW	0x00	di7_dt Data ID 7 data type.
23:22	RW	0x0	di6_vc Data ID 6 virtual channel.
21:16	RW	0x00	di6_dt Data ID 6 data type.
15:14	RW	0x0	di5_vc Data ID 5 virtual channel.
13:8	RW	0x00	di5_dt Data ID 5 data type.
7:6	RW	0x0	di4_vc Data ID 4 virtual channel.
5:0	RW	0x00	di4_dt Data ID 4 data type.

**CSI2HOST ERR1**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	err_ph_crc_lane2 Packet crc error of lane2 when sw_cphy_en=1.
30	RW	0x0	err_ph_crc_lane1 Packet crc error of lane1 when sw_cphy_en=1.
29	RW	0x0	err_ph_crc_lane0 Packet crc error of lane0 when sw_cphy_en=1.
28	RO	0x0	err_ecc_double Header ECC contains 2 errors,unrecoverable.
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3.
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2.
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1.
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0.
23:16	RO	0x00	reserved
15	RO	0x0	err_frame_data_vc3 Last received frame,in virtual channel 3,had at least one CRC error.
14	RO	0x0	err_frame_data_vc2 Last received frame,in virtual channel 2,had at least one CRC error.
13	RO	0x0	err_frame_data_vc1 Last received frame,in virtual channel 1,had at least one CRC error.
12	RO	0x0	err_frame_data_vc0 Last received frame,in virtual channel 0,had at least one CRC error.
11	RO	0x0	err_f_seq_vc3 Incorrect frame sequence detected in virtual channel 3.
10	RO	0x0	err_f_seq_vc2 Incorrect frame sequence detected in virtual channel 2.
9	RO	0x0	err_f_seq_vc1 Incorrect frame sequence detected in virtual channel 1.
8	RO	0x0	err_f_seq_vc0 Incorrect frame sequence detected in virtual channel 0.
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3.
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2.
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1.
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0.
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3.
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2.
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1.
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0(no synchronization achieved).



**CSI2HOST\_ERR2**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	phy_errcodehs_3 Lane 3 receiv error code.
26	RW	0x0	phy_errcodehs_2 Lane 2 receiv error code.
25	RW	0x0	phy_errcodehs_1 Lane 1 receiv error code.
24	RW	0x0	phy_errcodehs_0 Lane 0 receiv error code.
23:16	RO	0x00	reserved
15	RW	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3.
14	RW	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2.
13	RW	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1.
12	RW	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0.
11	RW	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3.
10	RW	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2.
9	RW	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1.
8	RW	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0.
7	RW	0x0	phy_errsoths_3 Start of transmission error on data lane 3(synchronization can still be achieved).
6	RW	0x0	phy_errsoths_2 Start of transmission error on data lane 2(synchronization can still be achieved).
5	RW	0x0	phy_errsoths_1 Start of transmission error on data lane 1(synchronization can still be achieved).
4	RW	0x0	phy_errsoths_0 Start of transmission error on data lane 0(synchronization can still be achieved).
3	RW	0x0	phy_erresc_3 Escape entry error(ULPM) on data lane 3.
2	RW	0x0	phy_erresc_2 Escape entry error(ULPM) on data lane 2.
1	RW	0x0	phy_erresc_1 Escape entry error(ULPM) on data lane 1.
0	RW	0x0	phy_erresc_0 Escape entry error(ULPM) on data lane 0.

**CSI2HOST\_MSK1**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RW	0x0	mask_err_ph_crc_lane2 Mask for err_ph_crc_lane2.
30	RW	0x0	mask_err_ph_crc_lane1 Mask for err_ph_crc_lane1.
29	RW	0x0	mask_err_ph_crc_lane0 Mask for err_ph_crc_lane0.
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double.
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc.
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc.
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc.
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3.
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2.
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1.
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0.
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3.
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2.
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1.
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0.
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc3.
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc2.
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1.
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0.
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3.
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2.
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1.
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0.

**CSI2HOST\_MSK2**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	mask_phy_errcodehs_3 Mask for phy_errcodehs_3.
26	RW	0x0	mask_phy_errcodehs_2 Mask for phy_errcodehs_2.
25	RW	0x0	mask_phy_errcodehs_1 Mask for phy_errcodehs_1.
24	RW	0x0	mask_phy_errcodehs_0 Mask for phy_errcodehs_0.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_id_vc3 Mask for err_id_vc3.
14	RW	0x0	mask_err_id_vc2 Mask for err_id_vc2.
13	RW	0x0	mask_err_id_vc1 Mask for err_id_vc1.
12	RW	0x0	mask_err_id_vc0 Mask for err_id_vc0.
11	RW	0x0	mask_vc3_err_ecc_corrected Mask for vc3_err_ecc_corrected.
10	RW	0x0	mask_vc2_err_ecc_corrected Mask for vc2_err_ecc_corrected.
9	RW	0x0	mask_vc1_err_ecc_corrected Mask for vc1_err_ecc_corrected.
8	RW	0x0	mask_vc0_err_ecc_corrected Mask for vc0_err_ecc_corrected.
7	RW	0x0	mask_phy_errsoths_3 Mask for phy_errsoths_3.
6	RW	0x0	mask_phy_errsoths_2 Mask for phy_errsoths_2.
5	RW	0x0	mask_phy_errsoths_1 Mask for phy_errsoths_1.
4	RW	0x0	mask_phy_errsoths_0 Mask for phy_errsoths_0.
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3.
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2.
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1.
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0.

**CSI2HOST CONTROL**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RW	0x03	sw_datatype_le The datatype of line end.
25:20	RW	0x02	sw_datatype_ls The datatype of line start.
19:14	RW	0x01	sw_datatype_fe The datatype of frame end.
13:8	RW	0x00	sw_datatype_fs The datatype of frame start.

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4	RW	0x0	sw_dsi_en 1'b0: For csi2 1'b1: For dsi
3:1	RO	0x0	reserved
0	RW	0x0	sw_cphy_en 1'b0: For dphy 1'b1: For cphy

### 10.5 Application Notes

The most important step is configuring the right CSI2HOST\_N\_LANES before pulling up csi\_resetrn. If the host is used to receive DSI data, the sw\_dsi\_en must be enabled, and the sw\_datatype\_fs, sw\_datatype\_fe, sw\_datatype\_ls, sw\_datatype\_le must be configured correctly. When the sw\_dsi\_en is enabled, those debug or error detection registers are useless.

## Chapter 11 Raster Graphic Acceleration (RGA2)

### 11.1 Overview

RGA2 is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as point/line drawing, image scaling, rotation, BitBLT, alpha blending.

### 11.2 Features

- **Data format**
  - Input data:
    - ◆ ARGB/RGB888/RGB565/RGB4444/RGB5551
    - ◆ YUV420/YUV422/YVYU422/YVYU420/YUV422SP10bit/YUV420SP10bit
  - Output data:
    - ◆ ARGB/RGB888/RGB565/RGB4444/RGB5551
    - ◆ YUV420/YUV422/YUV400/Y4/YVYU422/YVYU420
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror & rotation operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT:
    - A+B=B only BitBLT, A support rotate&scale when B fixed
    - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- **Others**
  - Support NN quantize (CLIP((source + offset) \* scale) for RGB channel)
  - Floyd–Steinberg dither (RGB888 or 565 TO Y4 ; RGB888 or 565 DITHER TO Y4)
- **MMU**
  - 4k/64k page size
  - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
  - TLB pre-fetch

#### Constrain:

- (1) YUV420/422-8bit virtual stride need 8byte align, xoff/yoff need 2byte align;
- (2) YUV420/422-10bit virtual stride need 16byte align, not support xoff/yoff;
- (3) Vertical scale down or not && Horizontal bi-cubic scale up src0 width<=2048;  
Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928;
- (4) Vertical scale down or not && Horizontal bilinear scale up src0 width<=4096;  
Vertical scale up && Horizontal bilinear scale up src0 width<=3856;

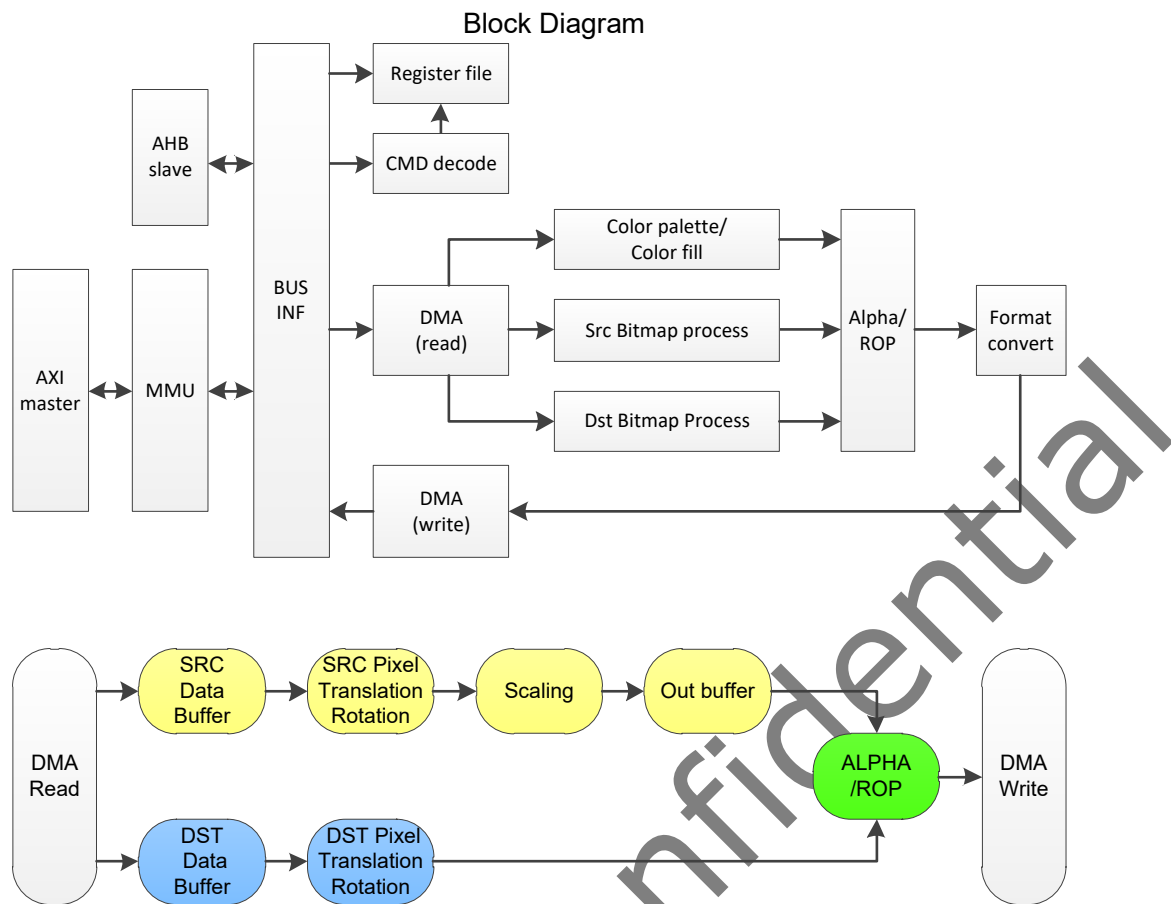


Fig. 11-1 RGA2 Block Diagram

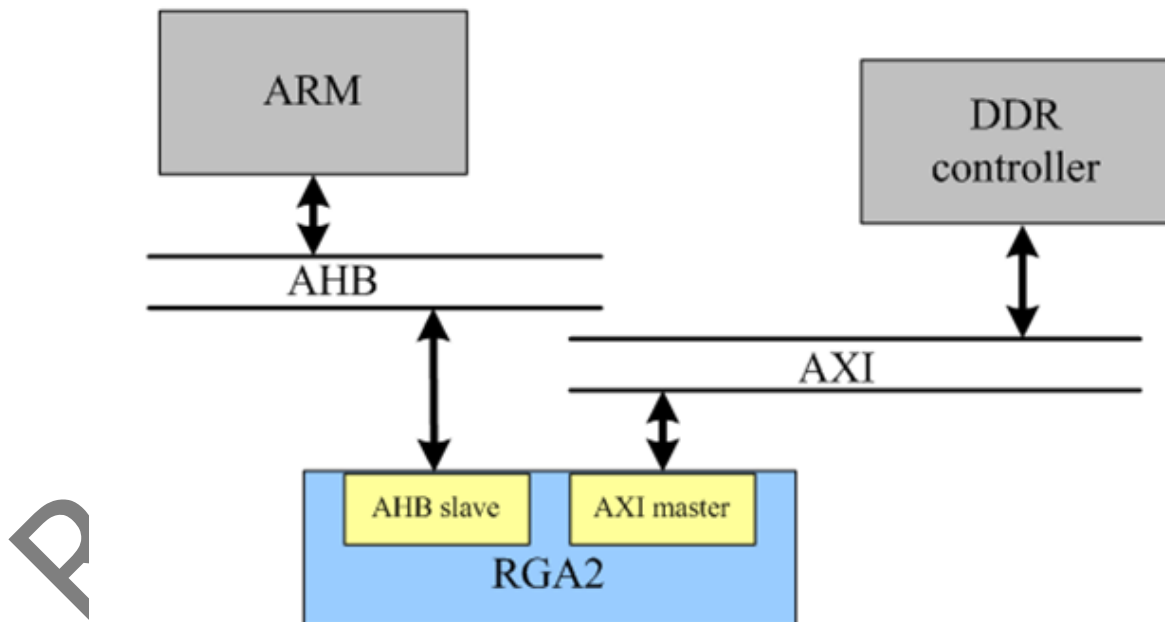


Fig. 11-2 RGA2 in SOC

## 11.3 Function Description

### 11.3.1 Data Format



Fig. 11-3 RGA Input Data Format

All input data (defined by SRC\_IN\_FMT/DST\_IN\_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST\_OUT\_FMT).

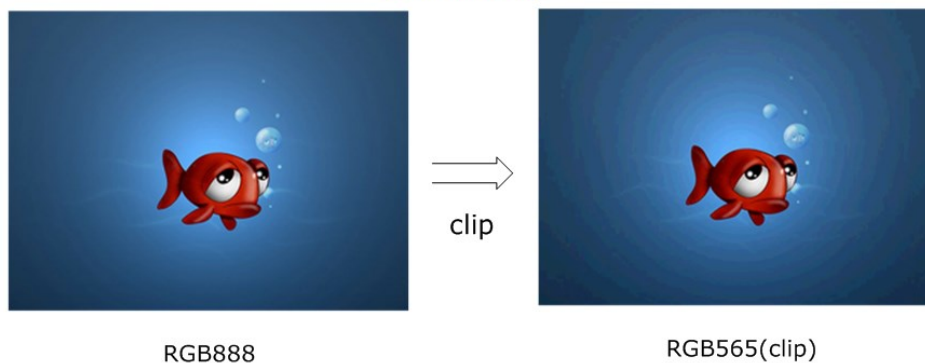
### 11.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

## Clip effect

(low quality)

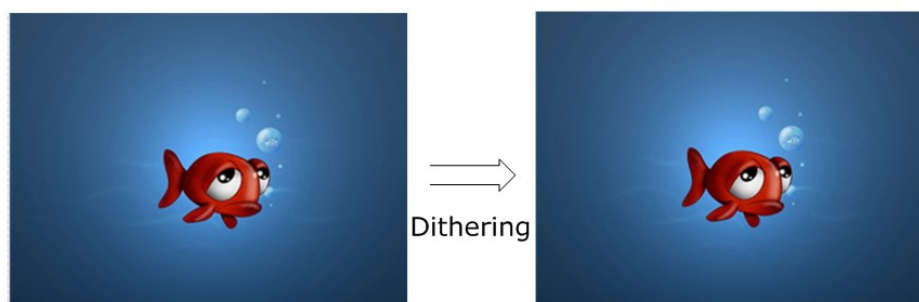


RGB888

RGB565(clip)

## Dithering effect

(better quality)

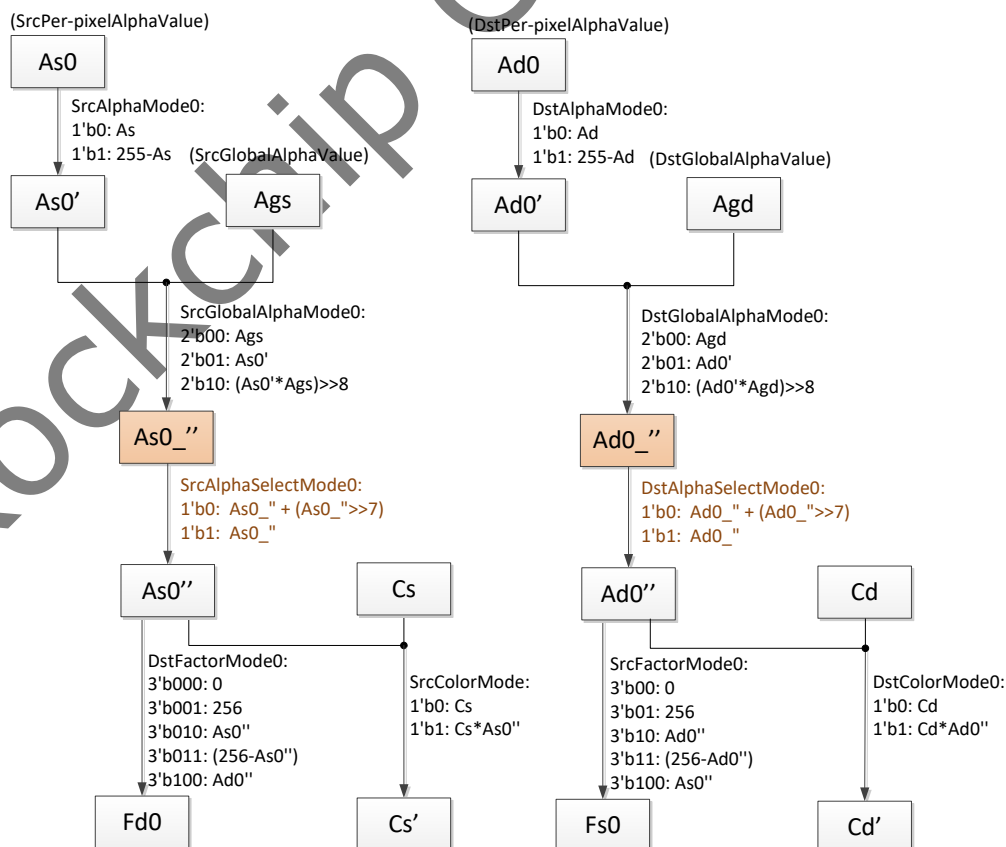


RGB888

RGB565(dithering)

Fig. 11-4 RGA Dither effect

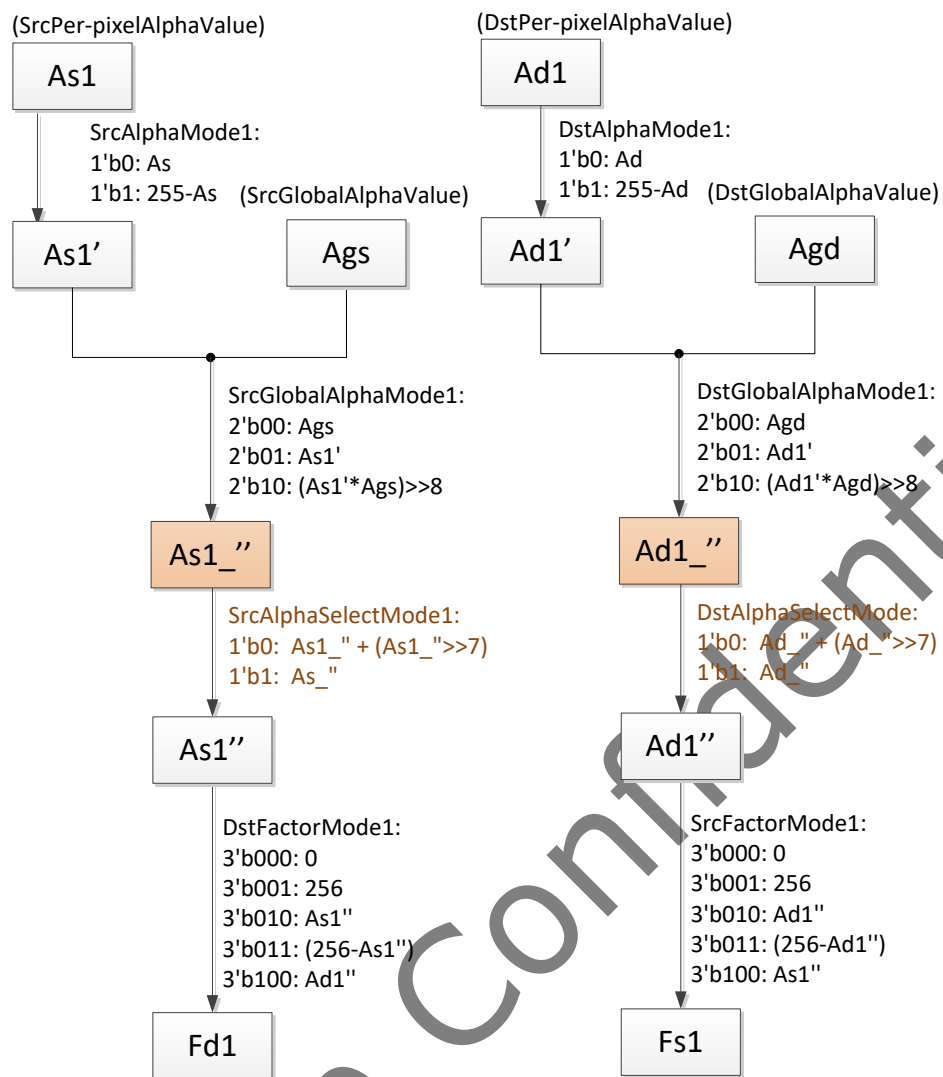
## 11.3.3 Alpha mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')





$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1'' – dst alpha'')

Fig. 11-5 alpha mode configure description

### 11.3.4 Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

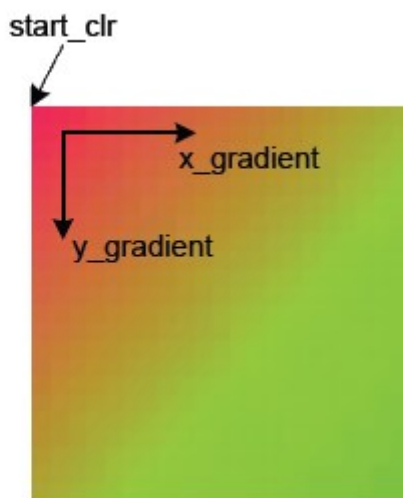


Fig. 11-6 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different

coordinary.

$A\_cur = (A\_start + x * x\_A\_gradient) + y * y\_A\_gradient;$

$R\_cur = (R\_start + x * x\_R\_gradient) + y * y\_R\_gradient;$

$G\_cur = (G\_start + x * x\_G\_gradient) + y * y\_G\_gradient;$

$B\_cur = (B\_start + x * x\_B\_gradient) + y * y\_B\_gradient;$

A\_start, R\_start, G\_start, B\_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

### 11.3.5 Scaling

The scaling operation is the imageresizing processing of source image. Scaling is done base on ARGB8888 format.

There are three sampling modes: scale down (Average); scale up(Bi-cubic).

### 11.3.6 NN quantize

The NN quantize is for NN pre\_process using. The function is  $CLIP((source + offset) * scale)$  for R G B channel. When use this function, the signal sw\_dst\_nn\_quantize\_en and reg NN\_QUANTIZE\_SCALE, NN\_QUANTIZE\_OFFSET need be configured.

### 11.3.7 Y4 output format and Floyd–Steinberg dither

The Y4 output format and Floyd–Steinberg dither is used for Eink panel. RGA supports RGB888 or 565 to Y4 directly. In this mode, signal sw\_dst\_fmt\_y4\_en needs set to 1. There is a 16 segments LUT could be used in Y4 output mode (reg is RGA2\_DST\_Y4MAP\_LUT0 and RGA2\_DST\_Y4MAP\_LUT1).

RGA also supports RGB888 or 565 dither to Y4. In this mode, the signals sw\_dst\_fmt\_y4\_en, sw\_dither\_down, sw\_dither\_mode need be configured.

**note:** If sw\_dither\_mode is set Y8 to Y1 mode, the output format is still Y4 format.

## 11.4 Register description

### 11.4.1 Register Summary

Slave address can be divided into different length for different usage, which is shown as follows.

Name	Offset	Size	Reset Value	Description
<u>RGA2_SYS_CTRL</u>	0x0000	W	0x00000044	RGA system control register
<u>RGA2_CMD_CTRL</u>	0x0004	W	0x00000000	RGA command control register
<u>RGA2_CMD_BASE</u>	0x0008	W	0x00000000	RGA command codes base address register
<u>RGA2_STATUS1</u>	0x000C	W	0x00000000	RGA status register
<u>RGA2_INT</u>	0x0010	W	0x00000000	RGA interrupt register
<u>RGA2_MMU_CTRL0</u>	0x0014	W	0x00000000	RGA MMU control 0 register
<u>RGA2_MMU_CMD_BASE</u>	0x0018	W	0x00000000	Register0000 Description
<u>RGA2_STATUS2</u>	0x001C	W	0x00000000	RGA status register
<u>RGA2_WORK_CNT</u>	0x0020	W	0x00000000	RGA work counter
<u>RGA2_VERSION_INFO</u>	0x0028	W	0x03256726	RTL version and FPGA version information
<u>RGA2_PERF_LATENCY_CTRL0</u>	0x0040	W	0x00000024	Axi performance latency module control register0
<u>RGA2_PERF_LATENCY_CTRL1</u>	0x0044	W	0x00000021	Axi performance latency module control register1
<u>RGA2_PERF_RD_MAX_LATENCY_NUM0</u>	0x0048	W	0x00000000	Read max latency number
<u>RGA2_PERF_RD_LATENCY_SAMP_NUM</u>	0x004C	W	0x00000000	The number of bigger than configured threshold value
<u>RGA2_PERF_RD_LATENCY_ACC_SUM</u>	0x0050	W	0x00000000	Total sample number
<u>RGA2_PERF_RD_AXI_TOTAL_BYTE</u>	0x0054	W	0x00000000	perf_rd_axi_total_byte
<u>RGA2_PERF_WR_AXI_TOTAL_BYTE</u>	0x0058	W	0x00000000	perf_wr_axi_total_byte
<u>RGA2_PERF_WORKING_CNT</u>	0x005C	W	0x00000000	perf_working_cnt
<u>RGA2_DST_CSC_00</u>	0x0060	W	0x000000bc	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_01</u>	0x0064	W	0x00000274	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_02</u>	0x0068	W	0x00000040	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_OFF0</u>	0x006C	W	0x00004200	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_10</u>	0x0070	W	0x00000798	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_11</u>	0x0074	W	0x000006a4	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_12</u>	0x0078	W	0x000001c0	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_OFF1</u>	0x007C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_20</u>	0x0080	W	0x000001c0	sw_dst_csc_mode[2]=1'b1 used csc factor

Name	Offset	Size	Reset Value	Description
<u>RGA2_DST_CSC_21</u>	0x0084	W	0x00000668	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_22</u>	0x0088	W	0x000007d8	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_DST_CSC_OFF2</u>	0x008C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
<u>RGA2_MODE_CTRL</u>	0x0100	W	0x00000000	RGA mode control register
<u>RGA2_SRC_INFO</u>	0x0104	W	0x00000000	RGA source information register
<u>RGA2_SRC_BASE0</u>	0x0108	W	0x00000000	RGA source image Y/RGB base address register
<u>RGA2_SRC_BASE1</u>	0x010C	W	0x00000000	RGA source image Cb/Cbr base address register
<u>RGA2_SRC_BASE2</u>	0x0110	W	0x00000000	RGA source image Cr base address register
<u>RGA2_SRC_BASE3</u>	0x0114	W	0x00000000	RGA source image 1 base address register
<u>RGA2_SRC_VIR_INFO</u>	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number register
<u>RGA2_SRC_ACT_INFO</u>	0x011C	W	0x00000000	RGA source image active width/height register
<u>RGA2_SRC_X_FACTOR</u>	0x0120	W	0x00000000	RGA source image horizontal scaling factor
<u>RGA2_SRC_Y_FACTOR</u>	0x0124	W	0x00000000	RGA source image vertical scaling factor
<u>RGA2_SRC_BG_COLOR</u>	0x0128	W	0x00000000	RGA source image background color
<u>RGA2_SRC_FG_COLOR</u>	0x012C	W	0x00000000	RGA source image foreground color
<u>RGA2_SRC_TR_COLOR0</u>	0x0130	W	0x00000000	RGA source image transparency color min value
<u>RGA2_CP_GR_A</u>	0x0130	W	0x00000000	RGA color gradient fill step register (color fill mode)
<u>RGA2_SRC_TR_COLOR1</u>	0x0134	W	0x00000000	RGA source image transparency color max value
<u>RGA2_CP_GR_B</u>	0x0134	W	0x00000000	RGA color gradient fill step register (color fill mode)
<u>RGA2_DST_INFO</u>	0x0138	W	0x00000000	RGA destination format register
<u>RGA2_DST_BASE0</u>	0x013C	W	0x00000000	RGA destination image base address 0 register
<u>RGA2_DST_BASE1</u>	0x0140	W	0x00000000	RGA destination image base address 1 register
<u>RGA2_DST_BASE2</u>	0x0144	W	0x00000000	RGA destination image base address 2 register
<u>RGA2_DST_VIR_INFO</u>	0x0148	W	0x00000000	RGA destination image virtual width/height register
<u>RGA2_DST_ACT_INFO</u>	0x014C	W	0x00000000	RGA destination image active width/height register
<u>RGA2_ALPHA_CTRL0</u>	0x0150	W	0x00000000	Alpha control register 0
<u>RGA2_ALPHA_CTRL1</u>	0x0154	W	0x00000000	Register0000 Description
<u>RGA2_FADING_CTRL</u>	0x0158	W	0x00000000	Fading control register
<u>RGA2_PAT_CON</u>	0x015C	W	0x00000000	Pattern size/offset register
<u>RGA2_ROP_CON0</u>	0x0160	W	0x76543210	ROP code 0 control register

Name	Offset	Size	Reset Value	Description
<u>RGA2_CP_GR_G</u>	0x0160	W	0x76543210	RGA color gradient fill step register (color fill mode)
<u>RGA2_DST_Y4MAP_LUT0</u>	0x0160	W	0x76543210	Y4MAP LUT REGS from lut0 to lut7
<u>RGA2_NN_QUANTIZE_SCALE</u>	0x0160	W	0x36543210	Quantize scale of RGB (2bit integer+8bit fraction, 0~3.99)
<u>RGA2_NN_QUANTIZE_OFFSET</u>	0x0164	W	0x00000000	Quantize offset of RGB (1bit signed + 8bit integer)
<u>RGA2_CP_GR_R</u>	0x0164	W	0xfedcba98	RGA color gradient fill step register (color fill mode)
<u>RGA2_DST_Y4MAP_LUT1</u>	0x0164	W	0xfedcba98	Y4MAP LUT REGS from lut8 to lut15
<u>RGA2_ROP_CON1</u>	0x0164	W	0x00000000	ROP code 1 control register
<u>RGA2_MASK_BASE</u>	0x0168	W	0x00000000	RGA mask base address register
<u>RGA2_MMU_CTRL1</u>	0x016C	W	0x00000000	RGA MMU control register 1
<u>RGA2_MMU_SRC_BASE</u>	0x0170	W	0x00000000	RGA source MMU TLB base address
<u>RGA2_MMU_SRC1_BASE</u>	0x0174	W	0x00000000	RGA source1 MMU TLB base address
<u>RGA2_MMU_DST_BASE</u>	0x0178	W	0x00000000	RGA destination MMU TLB base address
<u>RGA2_MMU_ELS_BASE</u>	0x017C	W	0x00000000	RGA ELSE MMU TLB base address

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access **DW**- Double WORD (64 bits) access

### 11.4.2 Detail Register Description

#### RGA2\_SYS\_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	sw_rst_handsave_p It would save protect-rstn into initial status if long time dead in protect-rstn status(auto clear into '0').
6	RW	0x1	sw_rst_protect_e Protect-rstn mode enable. It would be ensure all axi write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid.
5	RW	0x0	sw_auto_rst It would auto-resetn after one frame finish. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.

Bit	Attr	Reset Value	Description
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 1'b0: Disable 1'b1: Enable
1	WO	0x0	sw_cmd_mode RGA command mode 1'b0: Slave mode 1'b1: Master mode
0	W1 C	0x0	sw_cmd_op_st_p Only used in passive (slave) control mode

**RGA2\_CMD\_CTRL**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total command number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total command number would reset to RGA_INCR_CMD_NUM.

**RGA2\_CMD\_BASE**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cmd_base RGA command codes base address

**RGA2\_STATUS1**

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	Reserved Reserved
0	RO	0x0	sw_rga_sta RGA engine status 1'b0: Idle 1'b1: Working

**RGA2\_INT**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

**RGA2\_MMU\_CTRL0**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved

Bit	Attr	Reset Value	Description
10:9	RW	0x0	sw_els_ch_priority The priority of this channel
8:7	RW	0x0	sw_dst_ch_priority The priority of this channel
6:5	RW	0x0	sw_src1_ch_priority The priority of this channel
4:3	RW	0x0	sw_src_ch_priority The priority of this channel
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 1'b0: 4KB page 1'b1: 64KB page

**RGA2 MMU CMD BASE**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

**RGA2 STATUS2**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	Reserved
12:11	RO	0x0	rpp_mkram_rready Rpp mkram rready
10:6	RO	0x00	dstrpp_outbuf_rready Dstrpp outbuf rready
5:2	RO	0x0	srcrpp_outbuf_rready Srcrpp outbuf rready
1	RO	0x0	bus_error Bus error status
0	RO	0x0	rpp_error RPP error status

**RGA2 WORK CNT**



Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved
26:0	RO	0x0000000	sw_work_cnt RGA total working counter

**RGA2\_VERSION\_INFO**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x03	major Used for IP structure version infomation
23:20	RW	0x2	minor Big feature change under same structure
19:0	RW	0x56726	svnbuild Rtl current svn number

**RGA2\_PERF\_LATENCY\_CTRL0**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr
7:4	RW	0x2	sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type
2	RW	0x1	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enalbe
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

**RGA2\_PERF\_LATENCY\_CTRL1**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id
7:4	RW	0x2	sw_ar_count_id

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type
1:0	RW	0x1	sw_addr_align_type

**RGA2 PERF RD MAX LATENCY NUM0**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 Read max latency value of channel 0

**RGA2 PERF RD LATENCY SAMP NUM**

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 Read latency thr number channel 0

**RGA2 PERF RD LATENCY ACC SUM**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

**RGA2 PERF RD AXI TOTAL BYTE**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte

**RGA2 PERF WR AXI TOTAL BYTE**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte

**RGA2 PERF WORKING CNT**

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt

**RGA2\_DST\_CSC\_00**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x0bc	sw_dst_coe_00 1bit signed+8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

**RGA2\_DST\_CSC\_01**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x274	sw_dst_coe_01 1bit signed+8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

**RGA2\_DST\_CSC\_02**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x040	sw_dst_coe_02 1bit signed+8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

**RGA2\_DST\_CSC\_OFF0**

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x04200	sw_dst_coe_off0 1bit signed+8.8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

**RGA2\_DST\_CSC\_10**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RW	0x798	sw_dst_coe_10 1bit signed+8bit factor U: $sw\_dst\_coe\_10 * R + sw\_dst\_coe\_11 * G + sw\_dst\_coe\_12 * B + sw\_dst\_coe\_off1$

**RGA2\_DST\_CSC\_11**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x6a4	sw_dst_coe_11 1bit signed+8bit factor U: $sw\_dst\_coe\_10 * R + sw\_dst\_coe\_11 * G + sw\_dst\_coe\_12 * B + sw\_dst\_coe\_off1$

**RGA2\_DST\_CSC\_12**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x1c0	sw_dst_coe_12 1bit signed+8bit factor U: $sw\_dst\_coe\_10 * R + sw\_dst\_coe\_11 * G + sw\_dst\_coe\_12 * B + sw\_dst\_coe\_off1$

**RGA2\_DST\_CSC\_OFF1**

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x20200	sw_dst_coe_off1 1bit signed+8.8bit factor U: $sw\_dst\_coe\_10 * R + sw\_dst\_coe\_11 * G + sw\_dst\_coe\_12 * B + sw\_dst\_coe\_off1$

**RGA2\_DST\_CSC\_20**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x1c0	sw_dst_coe_20 1bit signed+8bit factor V: $sw\_dst\_coe\_20 * R + sw\_dst\_coe\_21 * G + sw\_dst\_coe\_22 * B + sw\_dst\_coe\_off2$

**RGA2\_DST\_CSC\_21**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x668	sw_dst_coe_21 1bit signed+8bit factor $V: sw\_dst\_coe\_20 * R + sw\_dst\_coe\_21 * G + sw\_dst\_coe\_22 * B + sw\_dst\_coe\_off2$

**RGA2\_DST\_CSC\_22**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x7d8	sw_dst_coe_22 1bit signed+8bit factor $V: sw\_dst\_coe\_20 * R + sw\_dst\_coe\_21 * G + sw\_dst\_coe\_22 * B + sw\_dst\_coe\_off2$

**RGA2\_DST\_CSC\_OFF2**

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x20200	sw_dst_coe_off2 1bit signed+8.8bit factor $V: sw\_dst\_coe\_20 * R + sw\_dst\_coe\_21 * G + sw\_dst\_coe\_22 * B + sw\_dst\_coe\_off2$

**RGA2\_MODE\_CTRL**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 1'b0: Clip 1'b1: Not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 1'b0: Solid color 1'b1: Pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 1'b0: SRC + DST => DST 1'b1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 3'b000: Bitblt 3'b001: Color palette 3'b010: Rectangle fill 3'b011: Update palette LUT/pattern ram

**RGA2 SRC INFO**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_src_yuv10_round_e This bit valid when RGA2E/2L support yuv 10bit picture input 1'b0: Yuv 10bit to 8bit round disable 1'b1: Yuv 10bit to 8bit round enable
27	RW	0x0	sw_src_yuv10_e This bit valid when RGA2E/2L support yuv 10bit picture input. 1'b0: Yuv 10bit disable 1'b1: Yuv 10bit enable
26	RW	0x0	sw_vsp_mode 1'b0: Bi-cubic 1'b1: Bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC bicubic scaling coefficient select 2'b00: CATROM 2'b01: MITCHELL 2'b10: HERMITE 2'b11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 1'b0: Normal stencil test (color key) 1'b1: Inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 2'b00: No scaling 2'b01: Down-scaling 2'b10: Up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 2'b00: No scaling 2'b01: Down-scaling 2'b10: Up-scaling
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 2'b00: No mirror 2'b01: X mirror 2'b10: Y mirror 2'b11: X mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 2'b00: 0 degree 2'b01: 90 degree 2'b10: 180 degree 2'b11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 2'b00: Bypass 2'b01: BT.601-range0(limit range) 2'b10: BT.601-range1(full range) 2'b11: BT.709-range0(limit range)
7	RW	0x0	sw_cp_endian Source Color palette endian swap 1'b0: Big endian 1'b1: Little endian

Bit	Attr	Reset Value	Description
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 1'b0: CrCb 1'b1: CbCr For YVYU422 mode, UV swap 1'b0: YVYU422(U LSB) 1'b1: YUYV422(V LSB)
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 1'b0: BGR 1'b1: RGB For YVYU422 mode, YC swap 1'b0: YVYU422(U LSB) 1'b1: VYUY422(Y LSB)
3:0	RW	0x0	sw_src_fmt Source bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 4'b0111: YVYU422(U LSB) 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P 4'b1100: 1BPP (color palette) 4'b1101: 2BPP (color palette) 4'b1110: 4BPP (color palette) 4'b1111: 8BPP (color palette)

**RGA2\_SRC\_BASE0**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 Source image Y/RGB base address

**RGA2\_SRC\_BASE1**

Address: Operational Base + offset (0x010c)



Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 Source image Cb base address (YUV422/420-P) Source image Cb/Cr base address (YU,V422/420-SP)

**RGA2\_SRC\_BASE2**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base2 Source image Cr base address (YUV422/420-P)

**RGA2\_SRC\_BASE3**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base3 Source image 1 RGB base address(source bitblt mode1)

**RGA2\_SRC\_VIR\_INFO**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:16	RW	0x000	sw_mask_vir_stride Mask image virtual stride (words)
15	RW	0x0	Reserved Reserved
14:0	RW	0x0000	sw_src_vir_stride Src image virtual stride (words)

**RGA2\_SRC\_ACT\_INFO**

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved
28:16	RW	0x0000	sw_src_act_height Source image active height
15:13	RW	0x0	Reserved1 Reserved
12:0	RW	0x0000	sw_src_act_width Source image active width

**RGA2\_SRC\_X\_FACTOR**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor $=((\text{SRC\_ACT\_WIDTH}-1)/(\text{DST\_ACT\_WIDTH}-1)) * 65536$
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor $=(\text{DST\_ACT\_WIDTH}/(\text{SRC\_ACT\_WIDTH}) * 65536 + 1$

**RGA2\_SRC\_Y\_FACTOR**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor $=((\text{SRC\_ACT\_HEIGHT}-1)/(\text{DST\_ACT\_HEIGHT}-1)) * 65536$
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor $=(\text{DST\_ACT\_HEIGHT}/(\text{SRC\_ACT\_HEIGHT}) * 65536 + 1$

**RGA2\_SRC\_BG\_COLOR**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

**RGA2\_SRC\_FG\_COLOR**

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

**RGA2\_SRC\_TR\_COLOR0**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin Source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin Source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin Source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin Source image transparency color R min value

**RGA2\_CP\_GR\_A**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

**RGA2\_SRC\_TR\_COLOR1**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax Source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax Source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax Source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax Source image transparency color R max value

**RGA2\_CP\_GR\_B**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

**RGA2\_DST\_INFO**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	sw_dst_nn_quantize_en Destination output RGB quantize calculate 1'b0: Quantize calculate disable 1'b1: Quantize calculate enable
25	RW	0x0	sw_dst_fmt_y4_en Destination output Y channel 4bit and UV 0bit 1'b0: Y4 out disable 1'b1: Y4 out enable
24	RW	0x0	sw_dst_fmt_yuv400_en Destination Cb-Cr output disable (valid for YUV420/2 P/SP format) 1'b0: CbCr output normal 1'b1: CbCr output disable

Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22	RW	0x0	sw_src1_csc_clip Src1 read BGR2YUV Clip mode(RGB from 0~255 clip to 36~235) 1'b0: Unclip 1'b1: Clip enable
21:20	RW	0x0	sw_src1_csc_mode SRC1 read bitmap RGB2YUV conversion mode 2'b00: Bypass 2'b01: BT.601-range0,BT601_l, Y00,255, UV00,255 2'b10: BT.601-range1,BT601_f, Y16,235, UV19,237 2'b11: BT.709-range0,BT709_l, Y16,255, UV16,237
19	RW	0x0	sw_dst_csc_mode_2 sw_dst_csc_mode[2]+sw_dst_csc_mode[1:0]; DST read bitmap CSC(r2y/y2y) conversion mode under sw_dst_csc_mode[2]=1'b0: 3'b10x: Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0 U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1 V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2 without clip 3'b110: Defulat BT.709-range1,BT601_f,Y16,235,UV16,240 clip 3'b111: Defulat BT.709-range1,BT601_f,Y16,235,UV16,237 clip
18	RW	0x0	sw_dst_csc_clip Dst write RGB2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b1: Clip enable 1'b0: Unclip
17:16	RW	0x0	sw_dst_csc_mode_01 sw_dst_csc_mode[1:0] under sw_dst_csc_mode[2]=1'b0: DST read bitmap RGB2YUV conversion mode 3'b000: Bypass 3'b001: BT.601-range0,BT601_l,Y00,255,UV00,255 3'b010: BT.601-range1,BT601_f,Y16,235,UV19,237 3'b011: BT.709-range0,BT709_l,Y16,255,UV16,237
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 2'b00: 888 to 666 2'b01: 888 to 565 2'b10: 888 to 555 2'b11: 888 to 444 DST YUV dither down bit mode 2'b00: Y8 to Y4 others:Y8 to Y1

Bit	Attr	Reset Value	Description
13	RW	0x0	sw_dither_down DST dither down enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 1'b0: BGR 1'b1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 3'b000: ABGR888 3'b001: XBGR888 3'b010: BGR packed 3'b100: RGB565 3'b101: ARGB1555 3'b110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 1'b0: CrCb 1'b1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 1'b0: BGR 1'b1: RGB

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 when sw_dst_fmt_yuv400_en=1, YUV420/2 P/SP format will change to YUV400: 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P only RGA2E has yuyv output format feature: 4'b1100: YVYU422(U, LSB) 4'b1101: YVYU420(U, LSB) 4'b1110: VYUY422(Y, LSB) 4'b1111: VYUY420(Y, LSB)

**RGA2\_DST\_BASE0**

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 Destination image Y/RGB base address

**RGA2\_DST\_BASE1**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 Destination image Cb/CbCr base address

**RGA2\_DST\_BASE2**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 Destination image Cr base address

**RGA2\_DST\_VIR\_INFO**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x000	sw_src1_vir_stride Source image 1 virtual stride (words)
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_vir_stride Destination image virtual stride(words)

**RG2 DST ACT INFO**

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_act_width Destination image active width

**RG2 ALPHA CTRL0**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved Reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 1'b0: Big endian 1'b1: Little endian
19:12	RW	0x00	sw_dst_global_alpha Global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha Global alpha value of SRC(Ags) Fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 2'b00: ROP 2 2'b01: ROP 3 2'b10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 1'b0: Alpha 1'b1: ROP

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 1'b0: Disable 1'b1: Enable

**RG2 ALPHA CTRL1**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 Src Transparent/opaque of alpha channel (As1') 1'b0: As 1'b1: 255-As
28	RW	0x0	sw_dst_alpha_m1 Dst Transparent/opaque of alpha channel (Ad1') 1'b0: Ad 1'b1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha src blend mode select of alpha channel (As1'') 2'b00: Ags 2'b01: As1' 2'b10: (As1'*Ags)>>8 2'b11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha dst blend mode select of alpha channel(Ad1'') 2'b00: Agd 2'b01: Ad1' 2'b10: (Ad1'*Agd)>>8 2'b11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha src calculate mode of alpha channel(As1'') 1'b0: As1''= As1_'' + (As1_''>>7) 1'b1: As1''= As1_''
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha dst calculate mode of alpha channel(Ad1'') 1'b0: Ad1''= Ad1_'' + (Ad1_''>>7) 1'b1: Ad1''= Ad1_''
21:19	RW	0x0	w_src_factor_m1 Src factore mode of alpha channel(Fs1) 3'b000: 0 3'b001: 256 3'b010: Ad1'' 3'b011: 256-Ad1'' 3'b100: As1''



Bit	Attr	Reset Value	Description
18:16	RW	0x0	sw_dst_factor_m1 Dst factore mode of alpha channel(Fd1) 3'b000: 0 3'b001: 256 3'b010: As1'' 3'b011: 256-As1'' 3'b100: Ad1''
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0') 1'b0: As 1'b1: 255-As
14	RW	0x0	sw_dst_alpha_m0 Dst Transparent/opaque of color channel (Ad0') 1'b0: Ad 1'b1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha src blend mode select of color channel (As0_''') 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 2'b11: Reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha dst blend mode select of color channel(Ad0_''') 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8 2'b11: Reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0''') 1'b0: As0'''= As0_''' + (As0_'''>>7) 1'b1: As0'''= As0_'''
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0''') 1'b0: Ad0'''= Ad0_''' + (Ad0_'''>>7) 1'b1: Ad0'''= Ad0_'''
7:5	RW	0x0	sw_src_factor_m0 Src factore mode of color channel(Fs0) 3'b000: 0 3'b001: 256 3'b010: Ad0'' 3'b011: 256-Ad0'' 3'b100: As0''

Bit	Attr	Reset Value	Description
4:2	RW	0x0	sw_dst_factor_m0 Dst factore mode of color channel(Fd0) 3'b000: 0 3'b001: 256 3'b010: As0'' 3'b011: 256-As0'' 3'b100: Ad0''
1	RW	0x0	sw_src_color_m0 SRC color select(Cs') 1'b0: Cs 1'b1: Cs * As0''
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd') 1'b0: Cd 1'b1: Cd * Ad0''

**RG2 FADING CTRL**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

**RG2 PAT CON**

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

**RGA2\_ROP\_CON0**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:25	RW	0x3b	Reserved Reserved
24:0	RW	0x0543210	sw_rop3_code0 Rop3 code 0 control bits

**RGA2\_CP\_GR\_G**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x7654	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x3210	sw_gradient_x_g X gradient value of Green (signed 8.8)

**RGA2\_DST\_Y4MAP\_LUT0**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x76543210	sw_dst_y4map_lut0 Y4 lut from lut0 to lut7

**RGA2\_NN\_QUANTIZE\_SCALE**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x365	sw_nn_quantize_scale_b Quantize scale of Blue (2bit integer+8bit fraction, 0--3.99)
19:10	RW	0x10c	sw_nn_quantize_scale_g Quantize scale of Green (2bit integer+8bit fraction, 0--3.99)
9:0	RW	0x210	sw_nn_quantize_scale_r Quantize scale of Red (2bit integer+8bit fraction, 0--3.99)

**RGA2\_NN\_QUANTIZE\_OFFSET**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	sw_nn_quantize_offset_b Quantize offset of Blue(1bit signed + 8bit integer)
19	RO	0x0	reserved
18:10	RW	0x000	sw_nn_quantize_offset_g Quantize offset of Green (1bit signed + 8bit integer)
9	RO	0x0	reserved
8:0	RW	0x000	sw_nn_quantize_offset_r Quantize offset of Red(1bit signed + 8bit integer)

**RGA2 CP GR R**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0xfedc	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0xba98	sw_gradient_x_r X gradient value of Red(signed 8.8)

**RGA2 DST Y4MAP LUT1**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0xfedcba98	sw_dst_y4map_lut1 Y4 lut from lut8 to lut15

**RGA2 ROP CON1**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:25	RW	0x7f	Reserved Reserved
24:0	RW	0x0dcba98	sw_rop3_code1 Rop3 code 1 control bits

**RGA2 MASK BASE**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base Mask base address in ROP4 mode LUT/ pattern load base address

**RGA2 MMU CTRL1**

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved
13	RW	0x0	sw_els_mmu_flush RGA ELSE channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
12	RW	0x0	sw_els_mmu_en RGA ELSE channel MMU enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
11	RW	0x0	sw_dst_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
10	RW	0x0	sw_dst_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	sw_dst_mmu_flush RGA DST channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
8	RW	0x0	sw_dst_mmu_en RGA DST channel MMU enable 1'b0: Disable 1'b1: Enable
7	RW	0x0	sw_src1_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
6	RW	0x0	sw_src1_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
4	RW	0x0	sw_src1_mmu_en RGA SRC1 channel MMU enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	sw_src_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
2	RW	0x0	sw_src_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 1'b0: Disable 1'b1: Enable

**RGA2 MMU SRC BASE**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address (128-bit)

**RGA2 MMU SRC1 BASE**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address (128-bit)

**RGA2 MMU DST BASE**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address (128-bit)

**RGA2 MMU ELS BASE**

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address (128-bit)

**11.5 Application Notes****11.5.1 Register Partition**

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

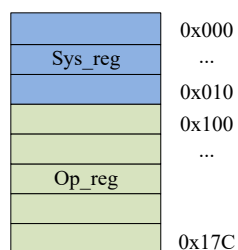


Fig. 11-7 RGA software main register-region

**11.5.2 Command Modes**

RGA has two command modes: slave mode and master mode. In slave mode (RGA\_SYS\_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA\_SYS\_CTRL[0] to '1'. In master mode (RGA\_SYS\_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA\_CMD\_CTRL[12:3], writing '1' to RGA\_CMD\_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA\_CMD\_ADDR) and command number

(RGA\_CMD\_CTRL[12:3]) should be set, then write '1' to cmd\_line\_st (RGA\_CMD\_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd\_incr\_num (RGA\_CMD\_CTRL[12:3]) and cmd\_incr\_valid (RGA\_CMD\_CTRL[1]=1'b1).

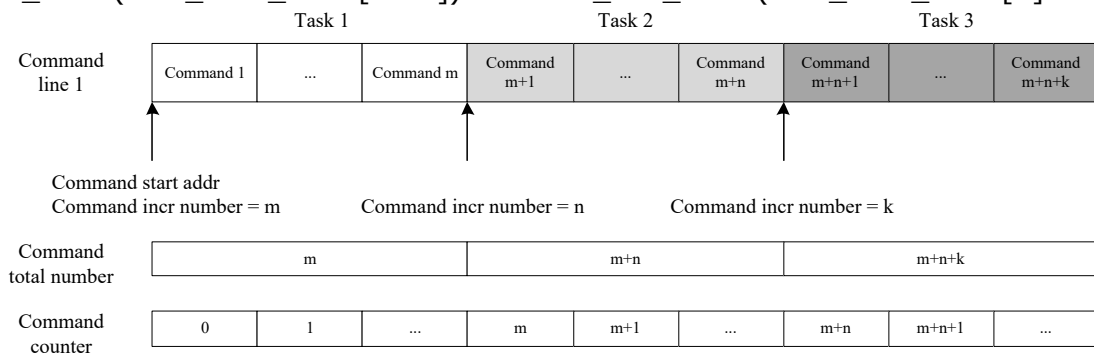


Fig. 11-8 RGA command line and command counter

### 11.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.

In master command mode, user can enable the current\_cmd\_int (sw\_intr\_cf), command by command to generate a interrupt at the end point of target command operation.

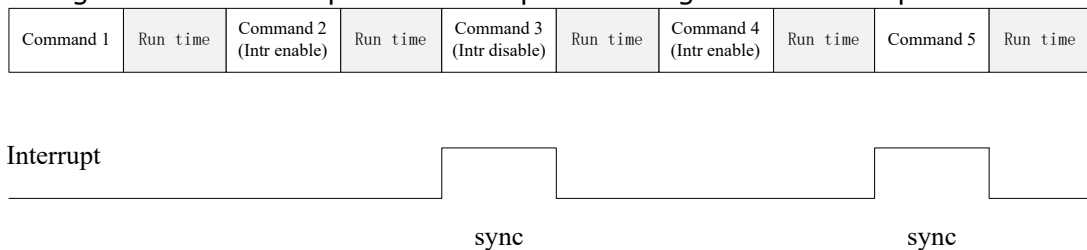


Fig. 11-9 RGA command sync generation

### 11.5.4 ColorPalette Application Notes

1. Palette/LUT Load into special RAM in ELS\_BUF\_CTRL.
2. ColorPalette/Pattern interval operations no need to initial LUT/pattern ram if LUT/pattern content no update.

### 11.5.5 Some special application constraint

1. The algorithm of vertical scale up: must select bicubic algorithm when source picture is smaller or equal to 2k and must select bilinear when bigger than 2k.
2. The effects that The output's definition is near 2k or 4k may not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of 2%(such as: 2048x32→2008x64).
3. At the scenario A+B->C, the size among the A B C has some constraints:  
A's size must be equal to C. C's size must equal to B when A+C is no rotation. C's rotation (90degree )size must equal to B1 when A+C is rotation 90 degree.

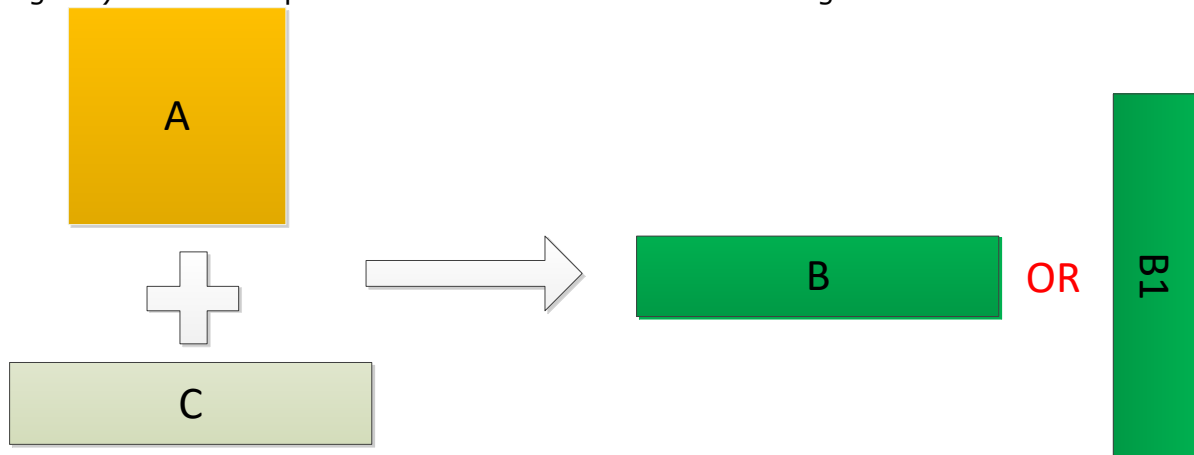


Fig. 11-10 The size constraint among A B C

4. YUV420/422-8bit virtual stride need 8byte align, xoff/yoff need 2byte align.
5. YUV420/422-10bit virtual stride need 16byte align, not support xoff/yoff.

6. Vertical scale down or not && Horizontal bi-cubic scale up src0 width<=2048.  
Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928.
7. Vertical scale down or not && Horizontal bilinear scale up src0 width<=4096.  
Vertical scale up && Horizontal bilinear scale up src0 width<=3856.



## Chapter 12 Image Enhancement Processor (IEP)

### 12.1 Overview

The Image Enhancement Processor (IEP) receives data from system main memory and transmits data to system main memory by AXI bus.

**The features of IEP are as follows:**

- **Image format**
  - Input data: YUV420/YUV422; semi-planar/planar; UV swap
  - Output data: YUV420/YUV422; semi-planar; UV swap; Tile mode
  - YUV down sampling conversion from 422 to 420
  - Max resolution for dynamic image up to 1920x1080
- **De-interlace**
  - **I5O2**: Input 5 Fields Output 2 frames mode
  - **I5O1T**: Input 5 Fields Output 1 Top frame mode
  - **I5O1B**: Input 5 Fields Output 1 Bottom frame mode
  - **I2O2**: Input 2 Fields Output 2 frames mode
  - **I1O1T**: Input 1 Field Output 1 Top frame mode
  - **I1O1B**: Input 1 Field Output 1 Bottom frame mode
  - **PULLDOWN\_REC**: Pull down Recovery mode
  - **DETECT\_ONLY**: Detect Only mode
  - **MVHIST**: De-interlace MV Histogram
  - **MD**: Motion Detection
  - **ME**: Motion Estimate
  - **MC**: Motion Compensation
  - **EEDI**: Enhanced Edge based Interpolation
  - **OSD DETECT**: On-Screen Display Detection
  - **FF DETECT**: Frame Field Detection
  - **FO DETECT**: Field Order Detection
  - **PD DETECT**: Pull down Detection
  - **CC**: Combining Check
- **Interface**
  - 32bit AHB bus slave
  - 128bit AXI bus master
  - Combined interrupt output

### 12.2 Block Diagram

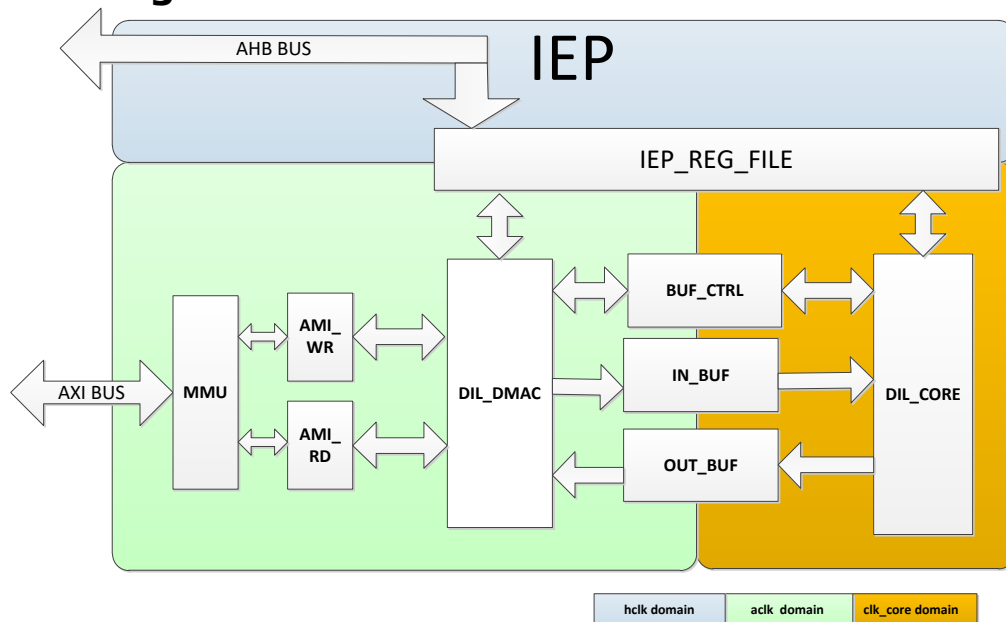


Fig. 12-1 IEP block diagram

The data path in IEP is in the previously diagram. The IEP comprises with:

## Deinterlace Core Processing

There are eight deinterlace modes (refer to feature description above) in the DIL\_CORE block. Some important functions for deinterlace are in this module such as MD, ME, MC, EEDI.

### DMA

DMA block responses for reading interlaced video data from DDR and writing frame data to DDR.

### REG FILE

All configurable signals will be configured in this block and send to other function modules for using. Detect data and MVHIST data will be read back to user in this module by AHB bus.

## 12.3 Function Description

### 12.3.1 Deinterlace

There are eight deinterlace modes including I5O2, I5O1B, I5O1T, I2O2, I1O1B, I1O1T and detect only mode in the deinterlace block.

#### I5O2 mode

The I5O2 mode represents for 5 fields of input images and 2 frames of output images. This mode is the most frequently used. The input source images are stored as interlaced mode which means top field and bottom field are stored by the method that one top field line follows one bottom field or conversely. So, current, next and preview input frame address (SRC\_ADDR\_CURY, SRC\_ADDR\_NXTY and SRC\_ADDR\_PERY for Y channel) need to be configured. Top frame and bottom frame address (DST\_ADDR\_TOPY, DST\_ADDR\_BOTY for Y channel) need to be configured for output 2 frames.

#### I5O1B/T mode

The I5O1B and I5O1T mode have the same input images as the I4O2 mode, but only one frame output is generated once which means only need configure one output frame address(top frame address for I5O1T mode and bottom frame address for I5O1B mode).

#### I2O2 mode

The I2O2 mode only need current input source frame, output is the same as I5O2 mode. This mode is the fastest and the most bandwidth saving.

#### I1O1B/T mode

The I1O1B and I1O1T mode have the same input as I2O2 mode and the same output as I5O1B and I5O1T mode.

#### Bypass mode

If bypass mode is selected, there are not any deinterlace operations.

#### Pulldown Recovery mode

If the Pulldown Detection block detects the current source is pulldown interlace video. IEP supports Pulldown Recovery by setting this mode.

#### Detect Only mode

This mode has no output frames for saving power and bandwidth. All of the detection results will be read back though AHB bus.

## 12.4 Register Description

### 12.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
IEP2_FRM_START	0x0000	W	0x00000000	Frame start and frame state register
IEP2_IEP_CONFIG0	0x0004	W	0x00000303	IEP configuration register0
IEP2_GATING_CTRL	0x0010	W	0x00000800	IEP auto gating register
IEP2_STATUS	0x0014	W	0x00000000	IEP status
IEP2_INT_EN	0x0020	W	0x00000011	IEP interrupt enable
IEP2_INT_CLR	0x0024	W	0x00000000	IEP interrupt clear
IEP2_INT_STS	0x0028	W	0x00000000	IEP interrupt status
IEP2_INT_RAW_STS	0x002C	W	0x00000000	IEP int raw status
IEP2_VIR_SRC_IMG_WID_TH	0x0030	W	0x00000000	Source Image virtual width

Name	Offset	Size	Reset Value	Description
<u>IEP2 VIR DST IMG WID TH</u>	0x0034	W	0x00000000	Destination Image virtual width
<u>IEP2 SRC IMG SIZE</u>	0x0038	W	0x00000000	Source image size
<u>IEP2 DIL CONFIG0</u>	0x0040	W	0x00029F01	Deinterlace config register0
<u>IEP2 IEP TIMEOUT CFG</u>	0x0050	W	0x0065B9AA	Timeout config
<u>IEP2 IEP VERSION INFO</u>	0x0054	W	0x20056471	IEP version info
<u>IEP2 DBG FRM CNT</u>	0x0058	W	0x00000000	Frame counter
<u>IEP2 DBG TIMEOUT CNT</u>	0x005C	W	0x00000000	Timeout cnt
<u>IEP2 SRC ADDR CUR Y</u>	0x0060	W	0x00000000	Start address of source current image(Y), frame addr
<u>IEP2 SRC ADDR NXT Y</u>	0x0064	W	0x00000000	Start address of source next image(Y), frame addr
<u>IEP2 SRC ADDR PRE Y</u>	0x0068	W	0x00000000	Start address of source previous image(Y), frame addr
<u>IEP2 SRC ADDR CUR UV</u>	0x006C	W	0x00000000	Start address of source current image(UV), SP MODE UV frame or U PMODE frame addr
<u>IEP2 SRC ADDR CUR V</u>	0x0070	W	0x00000000	Start address of source current image(V), P MODE V frame addr
<u>IEP2 SRC ADDR NXT UV</u>	0x0074	W	0x00000000	Start address of source next image(UV), SP MODE UV frame or U PMODE frame addr
<u>IEP2 SRC ADDR NXT V</u>	0x0078	W	0x00000000	Start address of source next image(V), P MODE V frame addr
<u>IEP2 SRC ADDR PRE UV</u>	0x007C	W	0x00000000	Start address of source previous image(UV), SP MODE UV frame addr or U PMODE frame addr
<u>IEP2 SRC ADDR PRE V</u>	0x0080	W	0x00000000	Start address of source previous image(V), P MODE V frame addr
<u>IEP2 SRC ADDR MD</u>	0x0084	W	0x00000000	MD LOAD ADDR BASE register0
<u>IEP2 SRC ADDR MV</u>	0x0088	W	0x00000000	MV LOAD ADDR BASE register0
<u>IEP2 ROI ADDR</u>	0x008C	W	0x00000000	ROI ADDR register
<u>IEP2 DST ADDR TOP Y</u>	0x00B0	W	0x00000000	DST TOP FRAME LUMA ADDR Register
<u>IEP2 DST ADDR BOT Y</u>	0x00B4	W	0x00000000	DST BOT FRAME LUMA ADDR Register
<u>IEP2 DST ADDR TOP C</u>	0x00B8	W	0x00000000	DST TOP FRAME CHROMA ADDR Register
<u>IEP2 DST ADDR BOT C</u>	0x00BC	W	0x00000000	DST BOT FRAME CHROMA ADDR Register
<u>IEP2 DST ADDR MD</u>	0x00C0	W	0x00000000	MD SAVE ADDR BASE register0
<u>IEP2 DST ADDR MV</u>	0x00C4	W	0x00000000	MV SAVE ADDR BASE register0
<u>IEP2 MD CONFIG0</u>	0x00E0	W	0x00000044	Motion dect config
<u>IEP2 DECT CONFIG0</u>	0x00E4	W	0x3C3C001E	Frame field dect, pulldown dect, OSD dect, comb dect
<u>IEP2 OSD LIMIT CONFIG</u>	0x00F0	W	0x00000000	OSD limite area dect config
<u>IEP2 OSD LIMIT AREA0</u>	0x00F4	W	0x00000000	OSD limite area 0
<u>IEP2 OSD LIMIT AREA1</u>	0x00F8	W	0x00000000	OSD limite area 1
<u>IEP2 OSD CONFIG0</u>	0x00FC	W	0x00020032	OSD dect config
<u>IEP2 OSD AREA CONF0</u>	0x0100	W	0x00000000	OSD area 0
<u>IEP2 OSD AREA CONF1</u>	0x0104	W	0x00000000	OSD area 1
<u>IEP2 OSD AREA CONF2</u>	0x0108	W	0x00000000	OSD area 2
<u>IEP2 OSD AREA CONF3</u>	0x010C	W	0x00000000	OSD area 3

Name	Offset	Size	Reset Value	Description
IEP2 OSD AREA CONF4	0x0110	W	0x00000000	OSD area 4
IEP2 OSD AREA CONF5	0x0114	W	0x00000000	OSD area 5
IEP2 OSD AREA CONF6	0x0118	W	0x00000000	OSD area 6
IEP2 OSD AREA CONF7	0x011C	W	0x00000000	OSD area 7
IEP2 ME CONFIG0	0x0120	W	0x001443A4	ME search config
IEP2 ME LIMIT CONFIG	0x0124	W	0x00001B25	ME SERACH LIMITE
IEP2 MV TRU LIST0	0x0128	W	0x00000000	MV trust list0~3
IEP2 MV TRU LIST1	0x012C	W	0x00000000	MV trust list4~7
IEP2 EEDI CONFIG0	0x0130	W	0x0000000C	EEDI CONFIG register0
IEP2 BLE CONFIG0	0x0134	W	0x00000001	BLE CONFIG register0
IEP2 COMB CONFIG0	0x0138	W	0x001004FF	COMB DECT CONFIG register0
IEP2 DIL MTN TAB0	0x0140	W	0x00000000	DIL_MTN_TAB0 table value
IEP2 DIL MTN TAB1	0x0144	W	0x00000000	DIL_MTN_TAB1 table value
IEP2 DIL MTN TAB2	0x0148	W	0x00000000	DIL_MTN_TAB2 table value
IEP2 DIL MTN TAB3	0x014C	W	0x00000000	DIL_MTN_TAB3 table value
IEP2 DIL MTN TAB4	0x0150	W	0x01010000	DIL_MTN_TAB4 table value
IEP2 DIL MTN TAB5	0x0154	W	0x06050302	DIL_MTN_TAB5 table value
IEP2 DIL MTN TAB6	0x0158	W	0x0F0D0A08	DIL_MTN_TAB6 table value
IEP2 DIL MTN TAB7	0x015C	W	0x1C191512	DIL_MTN_TAB7 table value
IEP2 DIL MTN TAB8	0x0160	W	0x2B282420	DIL_MTN_TAB8 table value
IEP2 DIL MTN TAB9	0x0164	W	0x3634312E	DIL_MTN_TAB9 table value
IEP2 DIL MTN TAB10	0x0168	W	0x3D3C3A38	DIL_MTN_TAB10 table value
IEP2 DIL MTN TAB11	0x016C	W	0x40403F3E	DIL_MTN_TAB11 table value
IEP2 DIL MTN TAB12	0x0170	W	0x40404040	DIL_MTN_TAB12 table value
IEP2 DIL MTN TAB13	0x0174	W	0x40404040	DIL_MTN_TAB13 table value
IEP2 DIL MTN TAB14	0x0178	W	0x40404040	DIL_MTN_TAB14 table value
IEP2 DIL MTN TAB15	0x017C	W	0x40404040	DIL_MTN_TAB15 table value
IEP2 RO PD TCNT	0x0400	W	0x00000000	Pulldown dect top field cnt
IEP2 RO PD BCNT	0x0404	W	0x00000000	Pulldown dect bot field cnt
IEP2 RO FF CUR TCNT	0x0408	W	0x00000000	Frame field dect current frame top field cnt
IEP2 RO FF CUR BCNT	0x040C	W	0x00000000	Frame field dect current frame bot field cnt
IEP2 RO FF NXT TCNT	0x0410	W	0x00000000	Frame field dect next frame top field cnt
IEP2 RO FF NXT BCNT	0x0414	W	0x00000000	Frame field dect next frame bot field cnt
IEP2 RO FF BLE TCNT	0x0418	W	0x00000000	Frame field dect current and next frame blend top field cnt
IEP2 RO FF BLE BCNT	0x041C	W	0x00000000	Frame field dect current and next frame blend bot field cnt
IEP2 RO FF COMB NZ	0x0420	W	0x00000000	Frame field dect current frame comb dect none zero num
IEP2 RO FF COMB F	0x0424	W	0x00000000	Frame field dect current frame comb dect num
IEP2 RO OSD NUM	0x0428	W	0x00000000	OSD area dect number
IEP2 RO OUT COMB CNT	0x042C	W	0x00000000	Deinterlace output comb dect
IEP2 RO FF GRADT TCNT	0x0430	W	0x00000000	Frame field dect, gradt top field cnt
IEP2 RO FF GRADT BCNT	0x0434	W	0x00000000	Frame field dect, gradt bot field cnt

Name	Offset	Size	Reset Value	Description
IEP2 RO MC VLD CNT	0x0438	W	0x00000000	MC valid cnt
IEP2 RO OSD AREA0 X	0x0440	W	0x00000000	OSD area dect area0 x
IEP2 RO OSD AREA0 Y	0x0444	W	0x00000000	OSD area dect area0 y
IEP2 RO OSD AREA1 X	0x0448	W	0x00000000	OSD area dect area1 x
IEP2 RO OSD AREA1 Y	0x044C	W	0x00000000	OSD area dect area1 y
IEP2 RO OSD AREA2 X	0x0450	W	0x00000000	OSD area dect area2 x
IEP2 RO OSD AREA2 Y	0x0454	W	0x00000000	OSD area dect area2 y
IEP2 RO OSD AREA3 X	0x0458	W	0x00000000	OSD area dect area3 x
IEP2 RO OSD AREA3 Y	0x045C	W	0x00000000	OSD area dect area3 y
IEP2 RO OSD AREA4 X	0x0460	W	0x00000000	OSD area dect area4 x
IEP2 RO OSD AREA4 Y	0x0464	W	0x00000000	OSD area dect area4 y
IEP2 RO OSD AREA5 X	0x0468	W	0x00000000	OSD area dect area5 x
IEP2 RO OSD AREA5 Y	0x046C	W	0x00000000	OSD area dect area5 y
IEP2 RO OSD AREA6 X	0x0470	W	0x00000000	OSD area dect area6 x
IEP2 RO OSD AREA6 Y	0x0474	W	0x00000000	OSD area dect area6 y
IEP2 RO OSD AREA7 X	0x0478	W	0x00000000	OSD area dect area7 x
IEP2 RO OSD AREA7 Y	0x047C	W	0x00000000	OSD area dect area7 y
IEP2 RO MV HIST BIN0	0x0480	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN1	0x0484	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN2	0x0488	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN3	0x048C	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN4	0x0490	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN5	0x0494	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN6	0x0498	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN7	0x049C	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN8	0x04A0	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN9	0x04A4	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN10	0x04A8	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN11	0x04AC	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN12	0x04B0	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN13	0x04B4	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN14	0x04B8	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN15	0x04BC	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN16	0x04C0	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN17	0x04C4	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN18	0x04C8	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN19	0x04CC	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN20	0x04D0	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN21	0x04D4	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN22	0x04D8	W	0x00000000	MV histogram

Name	Offset	Size	Reset Value	Description
IEP2 RO MV HIST BIN2 <u>3</u>	0x04DC	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN2 <u>4</u>	0x04E0	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN2 <u>5</u>	0x04E4	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN2 <u>6</u>	0x04E8	W	0x00000000	MV histogram
IEP2 RO MV HIST BIN2 <u>7</u>	0x04EC	W	0x00000000	MV histogram
IEP2 PERF LATENCY CTR <u>L0</u>	0x0600	W	0x00000010	Only exist when this IP has axi_performance monitor feature
IEP2 PERF LATENCY CTR <u>L1</u>	0x0604	W	0x00000011	Only exist when this IP has axi_performance monitor feature
IEP2 PERF RD MAX LAT <u>ENCY NUM0</u>	0x0608	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2 PERF RD LATENCY <u>SAMP NUM</u>	0x060C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2 PERF RD LATENCY <u>ACC SUM</u>	0x0610	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2 PERF WR AXI TOT <u>AL BYTE</u>	0x0614	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2 PERF WORKING CN <u>T</u>	0x0618	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2 PERF RD AXI TOTA <u>L BYTE</u>	0x061C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2 MMU DTE ADDR	0x0800	W	0x00000000	MMU DTE address
IEP2 MMU STATUS	0x0804	W	0x00000018	MMU status
IEP2 MMU CMD	0x0808	W	0x00000000	MMU command
IEP2 MMU PAGE FAULT <u>ADDR</u>	0x080C	W	0x00000000	Page fault address
IEP2 MMU ZAP ONE LIN <u>E</u>	0x0810	W	0x00000000	MMU zap one line
IEP2 MMU INT RAWSTAT	0x0814	W	0x00000000	MMU interruption raw status
IEP2 MMU INT CLEAR	0x0818	W	0x00000000	MMU interruption clear
IEP2 MMU INT MASK	0x081C	W	0x00000000	MMU interruption mask
IEP2 MMU INT STATUS	0x0820	W	0x00000000	MMU interruption status
IEP2 MMU AUTO GATING	0x0824	W	0x00000001	MMU auto gating config
IEP2 MMU ID	0x0828	W	0x00000000	MMU ID

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access **DW**- Double WORD (64 bits) access

## 12.4.2 Detail Register Description

### IEP2 FRM START

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_iep_frm_en Frame start, Write 1, frame work enable, frame end self clear

### IEP2 IEP CONFIG0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22	RW	0x0	sw_iep_init_dis 1'b1: Frame start not init 1'b0: Frame start initial
21	W1C	0x0	sw_iep_sreset_p Write 1 to global reset iep, auto clear
20	RW	0x0	sw_iep_rst_protect_dis Dma bus error, default protect soft reset, 1'b0: Protect reset; 1'b1: Direct reset;
19:17	RO	0x0	reserved
16	RW	0x0	sw_iep_debug_data_en If assert this bit, the debug signals will have data(just for power saving).
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_iep_dst_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: Reserved
11:10	RO	0x0	reserved
9:8	RW	0x3	sw_iep_dst_fmt 2'b00, 2'b01: Reserved 2'b10: YUV422 2'b11: YUV420
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_iep_src_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: P
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_iep_src_fmt 2'b00, 2'b01: Reserved 2'b10: YUV422 2'b11: YUV420

**IEP2 GATING CTRL**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x1	sw_reg_clk_on Reg clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
10	RW	0x0	sw_dma_clk_on Aclk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
9	RW	0x0	sw_ram_clk_on All ram clk always on 1'b0: Clk gating 1'b1: Clk always on
8	RW	0x0	sw_ctrl_clk_on CTRL clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
7	RW	0x0	sw_out_clk_on OUT clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.

Bit	Attr	Reset Value	Description
6	RW	0x0	sw_ble_clk_on BLE clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
5	RW	0x0	sw_eedi_clk_on EEDI clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
4	RW	0x0	sw_mc_clk_on MC clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
3	RW	0x0	sw_me_clk_on ME clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
2	RW	0x0	sw_dect_clk_on DECT clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
1	RW	0x0	sw_md_clk_on MD clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
0	RW	0x0	sw_iep_clk_on IEP clk is auto gating, if write 1, clk always on, not gating.

**IEP2 STATUS**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	ro_arst_finish_done IEP protect safety reset success status, write 1 clear or frame start clear.

**IEP2 INT EN**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5	RW	0x0	sw_iep_timeout_int_en Timeout int enable
4	RW	0x1	sw_iep_bus_error_en Bus error int enable
3:2	RO	0x0	reserved
1	RW	0x0	sw_iep_osd_max_en Frame process OSD dect done interrupt 1'b0: Inactive 1'b1: Active
0	RW	0x1	sw_iep_frm_done_en Frame process done interrupt 1'b0: Inactive 1'b1: Active

**IEP2 INT CLR**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5	W1C	0x0	sw_iep_timeout_int_clr Time out interruption clear
4	W1C	0x0	sw_iep_bus_error_clr Bus error interruption clear



Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	W1 C	0x0	sw_iep_osd_max_clr OSD max interruption clear
0	W1 C	0x0	sw_iep_frm_done_clr Frame process done interrupt clear

**IEP2 INT STS**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_sts Timeout error int status
4	RO	0x0	ro_bus_error_sts Bus error interruption status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_sts Frame process OSD dect done interrupt status
0	RO	0x0	ro_frm_done_sts Frame process done interrupt status

**IEP2 INT RAW STS**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_raw Timeout int raw status
4	RO	0x0	ro_bus_error_raw Bus error int raw status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_raw OSD max int raw status
0	RO	0x0	ro_frm_done_raw Frame done int raw status

**IEP2 VIR SRC IMG WIDTH**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_iep_src_vir_uv_stride Source uv virtual image width(word align)
15:0	RW	0x0000	sw_iep_src_vir_y_stride Source y virtual image width(word align)

**IEP2 VIR DST IMG WIDTH**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_iep_dst_vir_stride Destination virtual image width(word align)

**IEP2 SRC IMG SIZE**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_iep_src_pic_height Source and destination image height(pixel align and need minus 1, for example 1080 need config 1079)
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_iep_src_pic_width Source and destination image width(pixel align and need minus 1, for example 1920 need config 1919)

**IEP2 DIL CONFIG0**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x1	sw_dil_mv_hist_en Deinterlace MV histogram enable. 1'b1: Deinterlace need MV histogram 1'b0: MV histogram not work
16	RW	0x0	sw_dil_roi_en Deinterlace roi enable 1'b1: Deinterlace use roi mode 1'b0: ROI not work When ROI mode enable, each tile has 4bit for ROI mode 4'b0000: Normal mode 4'b0001: Bypass mode 4'b0010: EEDI only mode 4'b0011: Ma only mode 4'b0100: Ma mc mode(no cc) 4'b0101: Mc EEDI mode 4'b0110:4'b0111:Reserved 4'b1xxx: Mc only mode(MC's MV will be appointed by global MV based on roi[2:0] )
15	RW	0x1	sw_dil_comb_en Deinterlace output result comb dect, if is comb block back to original data, else select deinterlace result. 1'b1: Output data comb dect enable 1'b0: Output data not comb dect
14:13	RO	0x0	reserved
12	RW	0x1	sw_dil_memc_en Deinterlace use me, mc result. 1'b1: ME, MC work enable 1'b0: ME, MC not work enable
11	RW	0x1	sw_dil_osd_en On screen display dect enable. 1'b1: OSD dect enable 1'b0: OSD not dect
10	RW	0x1	sw_dil_pd_en Pulldown dect enable. 1'b1: Pulldown dect enable 1'b0: Pulldown not dect
9	RW	0x1	sw_dil_ff_en Frame field dect work enable. 1'b1: Frame field dect enable 1'b0: Frame field not dect
8	RW	0x1	sw_dil_md_pre_en 1'b1: MD use previous frame data enable 1'b0: MD only use current frame data to calc md

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5	RW	0x0	sw_dil_field_order Field display order. 1'b0: TFF, top field display first 1'b1: BFF, bot field display first
4	RW	0x0	sw_dil_out_mode Output deinterlace result to DDR, line mode or tile mode. 1'b0: LINE mode 1'b1: TILE mode
3:0	RW	0x1	sw_dil_mode 4'b0000: DIL DISABLE 4'b0001: ISO2 mode 4'b0010: ISO1T mode 4'b0011: ISO1B mode 4'b0100: I2O2 mode 4'b0101: I1O1T mode 4'b0110: I1O1B mode 4'b0111: Pulldown recovery mode 4'b1000: Bypass mode 4'b1001: Detect only mode other,reserved

**IEP2 IEP TIMEOUT CFG**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_iep_timeout_en IEP timeout enable
30:0	RW	0x0065b9aa	sw_iep_timeout_cnt When sw_iep_timeout_en ==1, timeout_cnt == sw_iep_timeout_cnt, iep timeout

**IEP2 IEP VERSION INFO**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x2	major Used for IP structure version information
27:20	RO	0x00	minor Big feature change under same structure
19:0	RO	0x56471	svnbuild Rtl current svn number

**IEP2 DBG FRM CNT**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	dbg_frm_cnt Self increase one after a frame operation is finished. Write arbitrary value to clear to zero.

**IEP2 DBG TIMEOUT CNT**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	dbg_timeout_cnt When sw_iep_timeout_en==1, frame cnt, frame start auto clear.

**IEP2\_SRC\_ADDR\_CURY**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_cury Current frame luma addr, frame addr

**IEP2\_SRC\_ADDR\_NXTY**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxty Next frame luma addr, frame addr

**IEP2\_SRC\_ADDR\_PREY**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_preY Start address of source previous image(Y), frame addr

**IEP2\_SRC\_ADDR\_CURUV**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_curuv Start address of source current image(UV), SP MODE UV frame addr or U PMODE frame addr

**IEP2\_SRC\_ADDR\_CURV**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_curv Start address of source current image(V), P MODE V frame addr

**IEP2\_SRC\_ADDR\_NXTUV**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxtuv Start address of source next image(UV), SP MODE UV frame addr or U PMODE frame addr

**IEP2\_SRC\_ADDR\_NXTV**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxtv Start address of source next image(V), P MODE V frame addr

**IEP2\_SRC\_ADDR\_PREUV**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_preuv Start address of source previous image(UV),SP MODE UV frame addr or U PMODE frame addr

**IEP2\_SRC\_ADDR\_PREV**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_prev Start address of source previous image(V), P MODE V frame addr

**IEP2\_SRC\_ADDR\_MD**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_md Md addr, save previous frame md gradt

**IEP2\_SRC\_ADDR\_MV**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_MV Md addr, save previous frame MV

**IEP2\_ROI\_ADDR**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_addr_roi ROI addr base

**IEP2\_DST\_ADDR\_TOPY**

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_topy Dst top frame luma start addr

**IEP2\_DST\_ADDR\_BOTY**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_boty Dst bot frame luma start addr

**IEP2\_DST\_ADDR\_TOPC**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_topc Dst top frame chroma start addr, uv save together

**IEP2\_DST\_ADDR\_BOTC**

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_botc Dst bot frame chroma start addr, uv save together

**IEP2\_DST\_ADDR\_MD**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_md MD addr, save previous frame md gradt, and also save current frame md grad

**IEP2\_DST\_ADDR\_MV**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_MV Output MV addr, save previous frame MV and also save current frame MV

**IEP2 MD CONFIG0**

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	sw_md_theta $\text{GRADtc} = \text{CLIP}(\text{GRADtf} - \text{sw\_md\_theta}, 0, 255);$
7:4	RW	0x4	sw_md_r $\text{Gradtf} * \text{md\_r} * 63 / (\text{gradtf} * \text{md\_r} * 63 + \text{gradv})$
3:0	RW	0x4	sw_md_lambda Current grad * md_lambda/8 + pre grad*(8-md_lambda)/8, value range from 0~8

**IEP2 DECT CONFIG0**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x3c	sw_osd_gradv_thr Original data grad compare with gradv thr, if more than gradv_thr, may be OSD area.
23:16	RW	0x3c	sw_osd_gradh_thr Original data grad compare with gradh thr, if more than gradh_thr, may be OSD area.
15:12	RO	0x0	reserved
11:8	RW	0x0	sw_osd_area_num OSD area number, frame field dect, pulldown not dect this area, comb dect also use this value, 0~8.
7:0	RW	0x1e	sw_dect_resi_thr For resi to bin, frame field, pulldown, OSD dect use this value.

**IEP2 OSD LIMIT CONFIG**

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4	RW	0x0	sw_osd_pos_limit_num OSD constrain area dect num, real value = OSD_pos_num+1
3:1	RO	0x0	reserved
0	RW	0x0	sw_osd_pos_limit_en OSD area constrain dect enable

**IEP2 OSD LIMIT AREA0**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area0 OSD constrain area 0 [6:0]: OSD constrain area0 x start, 16pixel num [13:7]: OSD constrain area0 x end, 16pixel num [22:14]: OSD constrain area0 y start, 4 pixel num [31:23]: OSD constrain area0 y end, 4 pixel num

**IEP2 OSD LIMIT AREA1**

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area1 OSD limite area 1 [6:0]: OSD constrain area0 x start, 16pixel num [13:7]: OSD constrain area0 x end, 16pixel num [22:14]: OSD constrain area0 y start, 4 pixel num [31:23]: OSD constrain area0 y end, 4 pixel num

**IEP2 OSD CONFIG0**

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x002	sw_osd_line_num Dect line num should more than OSD_line_num*4, this lines may be OSD area.
15:11	RO	0x00	reserved
10:0	RW	0x032	sw_osd_pec_thr A line should more than OSD_per_thr, this line may be OSD area.

**IEP2 OSD AREA CONF0**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end0 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta0 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end0 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta0 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF1**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end1 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta1 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end1 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta1 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF2**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end2 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta2 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end2 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta2 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF3**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end3 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta3 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end3 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta3 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF4**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end4 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta4 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end4 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta4 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF5**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end5 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta5 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end5 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta5 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF6**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end6 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta6 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end6 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta6 OSD area x start, 16pixel num

**IEP2 OSD AREA CONF7**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end7 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta7 OSD area y start, 4 pixel num



Bit	Attr	Reset Value	Description
13:7	RW	0x00	sw_osd_x_end7 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta7 OSD area x start, 16pixel num

**IEP2 ME CONFIG0**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x14	sw_me_thr_offset me_thr = me_thr(from md module) - sw_me_thr_offset. This signal is signed from(-128 ~127).
15:12	RW	0x4	sw_mv_similar_num_thr0 MV similar check result = MV_similar_invld_num < sw_mv_similar_num_thr0
11:8	RW	0x3	sw_mv_similar_thr surround MV similar =  cur_MV - surround_MV  < sw_mv_similar_thr
7:4	RW	0xa	sw_mv_bonus MVc calc MV,the same MV range value
3:0	RW	0x4	sw_me_pena balance resi and grad, grad*me_pena/8, me_pena value range from 0~8

**IEP2 ME LIMIT CONFIG**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x1b	sw_mv_right_limt MV right range limit, from 0~27, default 27
7:6	RO	0x0	reserved
5:0	RW	0x25	sw_mv_left_limt MV left range limit, from -27~0, default-27

**IEP2 MV TRU LIST0**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list3_mv MV trust list MV3
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list3_vld MV trust list MV3 vld
23:18	RW	0x00	sw_mv_tru_list2_mv MV trust list MV2
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list2_vld MV trust list MV2 vld
15:10	RW	0x00	sw_mv_tru_list1_mv MV trust list MV1
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list1_vld MV trust list MV1 vld
7:2	RW	0x00	sw_mv_tru_list0_mv MV trust list MV0

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list0_vld MV trust list MV0 vld

**IEP2 MV TRU LIST1**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list7_mv MV trust list MV7
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list7_vld MV trust list MV7 vld
23:18	RW	0x00	sw_mv_tru_list6_mv MV trust list MV6
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list6_vld MV trust list MV6 vld
15:10	RW	0x00	sw_mv_tru_list5_mv MV trust list MV5
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list5_vld MV trust list MV5 vld
7:2	RW	0x00	sw_mv_tru_list4_mv MV trust list MV4
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list4_vld MV trust list MV4 vld

**IEP2 EEDI CONFIG0**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RW	0x0c	sw_eedi_thr0 EEDI thr0

**IEP2 BLE CONFIG0**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x1	sw_ble_backtoma_num Left and right colum of frame will back to ma, give up mc.

**IEP2 COMB CONFIG0**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	sw_comb_cnt_thr Top or bot frame comb dect compare with original comb dect
23:22	RO	0x0	reserved
21:16	RW	0x10	sw_comb_feature_thr Top or bot frame comb dect compare with original comb dect
15:8	RW	0x04	sw_comb_t_thr Different line compare use comb_t_thr

Bit	Attr	Reset Value	Description
7:0	RW	0xff	sw_comb_osd_vld OSD area dect comb block back to original [0] area0,[1]area1....[7]area7 1'b1: Back to original 1'b0: Not back to original

**IEP2 DIL MTN TAB0**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab03 sw_mtn_sub_tab03
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab02 sw_mtn_sub_tab02
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab01 sw_mtn_sub_tab01
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab00 sw_mtn_sub_tab00

**IEP2 DIL MTN TAB1**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab07 sw_mtn_sub_tab07
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab06 sw_mtn_sub_tab06
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab05 sw_mtn_sub_tab05
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab04 sw_mtn_sub_tab04

**IEP2 DIL MTN TAB2**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab11 sw_mtn_sub_tab11
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab10 sw_mtn_sub_tab10
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab09 sw_mtn_sub_tab09
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab08 sw_mtn_sub_tab08

**IEP2 DIL MTN TAB3**

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab15 sw_mtn_sub_tab15
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab14 sw_mtn_sub_tab14
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab13 sw_mtn_sub_tab13
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab12 sw_mtn_sub_tab12

**IEP2 DIL MTN TAB4**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x01	sw_mtn_sub_tab19 sw_mtn_sub_tab19
23	RO	0x0	reserved
22:16	RW	0x01	sw_mtn_sub_tab18 sw_mtn_sub_tab18
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab17 sw_mtn_sub_tab17
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab16 sw_mtn_sub_tab16

**IEP2 DIL MTN TAB5**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x06	sw_mtn_sub_tab23 sw_mtn_sub_tab23
23	RO	0x0	reserved
22:16	RW	0x05	sw_mtn_sub_tab22 sw_mtn_sub_tab22
15	RO	0x0	reserved
14:8	RW	0x03	sw_mtn_sub_tab21 sw_mtn_sub_tab21
7	RO	0x0	reserved
6:0	RW	0x02	sw_mtn_sub_tab20 sw_mtn_sub_tab20

**IEP2 DIL MTN TAB6**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x0f	sw_mtn_sub_tab27 sw_mtn_sub_tab27
23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:16	RW	0x0d	sw_mtn_sub_tab26 sw_mtn_sub_tab26
15	RO	0x0	reserved
14:8	RW	0x0a	sw_mtn_sub_tab25 sw_mtn_sub_tab25
7	RO	0x0	reserved
6:0	RW	0x08	sw_mtn_sub_tab24 sw_mtn_sub_tab24

**IEP2 DIL MTN TAB7**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	sw_mtn_sub_tab31 sw_mtn_sub_tab31
23	RO	0x0	reserved
22:16	RW	0x19	sw_mtn_sub_tab30 sw_mtn_sub_tab30
15	RO	0x0	reserved
14:8	RW	0x15	sw_mtn_sub_tab29 sw_mtn_sub_tab29
7	RO	0x0	reserved
6:0	RW	0x12	sw_mtn_sub_tab28 sw_mtn_sub_tab28

**IEP2 DIL MTN TAB8**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x2b	sw_mtn_sub_tab35 sw_mtn_sub_tab35
23	RO	0x0	reserved
22:16	RW	0x28	sw_mtn_sub_tab34 sw_mtn_sub_tab34
15	RO	0x0	reserved
14:8	RW	0x24	sw_mtn_sub_tab33 sw_mtn_sub_tab33
7	RO	0x0	reserved
6:0	RW	0x20	sw_mtn_sub_tab32 sw_mtn_sub_tab32

**IEP2 DIL MTN TAB9**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x36	sw_mtn_sub_tab39 sw_mtn_sub_tab39
23	RO	0x0	reserved
22:16	RW	0x34	sw_mtn_sub_tab38 sw_mtn_sub_tab38
15	RO	0x0	reserved
14:8	RW	0x31	sw_mtn_sub_tab37 sw_mtn_sub_tab37
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x2e	sw_mtn_sub_tab36 sw_mtn_sub_tab36

**IEP2 DIL MTN TAB10**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x3d	sw_mtn_sub_tab43 sw_mtn_sub_tab43
23	RO	0x0	reserved
22:16	RW	0x3c	sw_mtn_sub_tab42 sw_mtn_sub_tab42
15	RO	0x0	reserved
14:8	RW	0x3a	sw_mtn_sub_tab41 sw_mtn_sub_tab41
7	RO	0x0	reserved
6:0	RW	0x38	sw_mtn_sub_tab40 sw_mtn_sub_tab40

**IEP2 DIL MTN TAB11**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab47 sw_mtn_sub_tab47
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab46 sw_mtn_sub_tab46
15	RO	0x0	reserved
14:8	RW	0x3f	sw_mtn_sub_tab45 sw_mtn_sub_tab45
7	RO	0x0	reserved
6:0	RW	0x3e	sw_mtn_sub_tab44 sw_mtn_sub_tab44

**IEP2 DIL MTN TAB12**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab51 sw_mtn_sub_tab51
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab50 sw_mtn_sub_tab50
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab49 sw_mtn_sub_tab49
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab48 sw_mtn_sub_tab48

**IEP2 DIL MTN TAB13**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab55 sw_mtn_sub_tab55
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab54 sw_mtn_sub_tab54
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab53 sw_mtn_sub_tab53
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab52 sw_mtn_sub_tab52

**IEP2 DIL MTN TAB14**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab59 sw_mtn_sub_tab59
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab58 sw_mtn_sub_tab58
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab57 sw_mtn_sub_tab57
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab56 sw_mtn_sub_tab56

**IEP2 DIL MTN TAB15**

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab63 sw_mtn_sub_tab63
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab62 sw_mtn_sub_tab62
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab61 sw_mtn_sub_tab61
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab60 sw_mtn_sub_tab60

**IEP2 RO PD TCNT**

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_tcnt Pulldown dect top field cnt

**IEP2 RO PD BCNT**

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_bcnc Pulldown dect bot field cnt

**IEP2 RO FF CUR TCNT**

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_tcnc Frame field dect current frame top field cnt

**IEP2 RO FF CUR BCNT**

Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_bcnc Frame field dect current frame bot field cnt

**IEP2 RO FF NXT TCNT**

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_tcnc Frame field dect next frame top field cnt

**IEP2 RO FF NXT BCNT**

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_bcnc Frame field dect next frame bot field cnt

**IEP2 RO FF BLE TCNT**

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_tcnc Frame field dect current and next frame blend top field cnt

**IEP2 RO FF BLE BCNT**

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_bcnc Frame field dect current and next frame blend bot field cnt

**IEP2 RO FF COMB NZ**

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_nz Frame field dect current frame none zero num

**IEP2 RO FF COMB F**

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_comb_f Frame field dect current frame comb dect num



**IEP2 RO OSD NUM**

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ro_dect_osd_cnt OSD area dect number

**IEP2 RO OUT COMB CNT**

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_out_osd_comb_cnt Top frame and bot frame OSD area comb num
15:0	RO	0x0000	ro_out_comb_cnt Top frame and bot frame comb num

**IEP2 RO FF GRADT TCNT**

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_tcmt Frame field dect, gradt top field cnt

**IEP2 RO FF GRADT BCNT**

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_bcmt Frame field dect, gradt bot field cnt

**IEP2 RO MC VLD CNT**

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	ro_mc_vld_cnt OSD area dect number

**IEP2 RO OSD AREA0 X**

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta0 1 pixel

**IEP2 RO OSD AREA0 Y**

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta0 1 pixel

**IEP2 RO OSD AREA1 X**

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta1 1 pixel

**IEP2 RO OSD AREA1 Y**

Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta1 1 pixel

**IEP2 RO OSD AREA2 X**

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta2 1 pixel

**IEP2 RO OSD AREA2 Y**

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta2 1 pixel

**IEP2 RO OSD AREA3 X**

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta3 1 pixel

**IEP2 RO OSD AREA3 Y**

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26:16	RO	0x000	ro_y_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta3 1 pixel

**IEP2 RO OSD AREA4 X**

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta4 1 pixel

**IEP2 RO OSD AREA4 Y**

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta4 1 pixel

**IEP2 RO OSD AREA5 X**

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta5 1 pixel

**IEP2 RO OSD AREA5 Y**

Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta5 1 pixel

**IEP2 RO OSD AREA6 X**

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end6 1 pixel
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:0	RO	0x000	ro_x_sta6 1 pixel

**IEP2 RO OSD AREA6 Y**

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end6 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta6 1 pixel

**IEP2 RO OSD AREA7 X**

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta7 1 pixel

**IEP2 RO OSD AREA7 Y**

Address: Operational Base + offset (0x047C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta7 1 pixel

**IEP2 RO MV HIST BIN0**

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist01 Mv_histogram01
15:0	RO	0x0000	ro_mv_hist00 Mv_histogram00

**IEP2 RO MV HIST BIN1**

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist03 Mv_histogram03
15:0	RO	0x0000	ro_mv_hist02 Mv_histogram02

**IEP2 RO MV HIST BIN2**

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist05 Mv_histogram05

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ro_mv_hist04 Mv_histogram04

**IEP2 RO MV HIST BIN3**

Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist07 Mv_histogram07
15:0	RO	0x0000	ro_mv_hist06 Mv_histogram06

**IEP2 RO MV HIST BIN4**

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist09 Mv_histogram09
15:0	RO	0x0000	ro_mv_hist08 Mv_histogram08

**IEP2 RO MV HIST BIN5**

Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist11 Mv_histogram11
15:0	RO	0x0000	ro_mv_hist10 Mv_histogram10

**IEP2 RO MV HIST BIN6**

Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist13 Mv_histogram13
15:0	RO	0x0000	ro_mv_hist12 Mv_histogram12

**IEP2 RO MV HIST BIN7**

Address: Operational Base + offset (0x049C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist15 Mv_histogram15
15:0	RO	0x0000	ro_mv_hist14 Mv_histogram14

**IEP2 RO MV HIST BIN8**

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist17 Mv_histogram17
15:0	RO	0x0000	ro_mv_hist16 Mv_histogram16

**IEP2 RO MV HIST BIN9**

Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist19 Mv_histogram19
15:0	RO	0x0000	ro_mv_hist18 Mv_histogram18

**IEP2 RO MV HIST BIN10**

Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist21 Mv_histogram21
15:0	RO	0x0000	ro_mv_hist20 Mv_histogram20

**IEP2 RO MV HIST BIN11**

Address: Operational Base + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist23 Mv_histogram23
15:0	RO	0x0000	ro_mv_hist22 Mv_histogram22

**IEP2 RO MV HIST BIN12**

Address: Operational Base + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist25 Mv_histogram25
15:0	RO	0x0000	ro_mv_hist24 Mv_histogram24

**IEP2 RO MV HIST BIN13**

Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist27 Mv_histogram27
15:0	RO	0x0000	ro_mv_hist26 Mv_histogram26

**IEP2 RO MV HIST BIN14**

Address: Operational Base + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist29 Mv_histogram29
15:0	RO	0x0000	ro_mv_hist28 Mv_histogram28

**IEP2 RO MV HIST BIN15**

Address: Operational Base + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist31 Mv_histogram31
15:0	RO	0x0000	ro_mv_hist30 Mv_histogram30

**IEP2 RO MV HIST BIN16**

Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist33 Mv_histogram33
15:0	RO	0x0000	ro_mv_hist32 Mv_histogram32

**IEP2 RO MV HIST BIN17**

Address: Operational Base + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist35 Mv_histogram35
15:0	RO	0x0000	ro_mv_hist34 Mv_histogram34

**IEP2 RO MV HIST BIN18**

Address: Operational Base + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist37 Mv_histogram37
15:0	RO	0x0000	ro_mv_hist36 Mv_histogram36

**IEP2 RO MV HIST BIN19**

Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist39 Mv_histogram39
15:0	RO	0x0000	ro_mv_hist38 Mv_histogram38

**IEP2 RO MV HIST BIN20**

Address: Operational Base + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist41 Mv_histogram41
15:0	RO	0x0000	ro_mv_hist40 Mv_histogram40

**IEP2 RO MV HIST BIN21**

Address: Operational Base + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist43 Mv_histogram43
15:0	RO	0x0000	ro_mv_hist42 Mv_histogram42

**IEP2 RO MV HIST BIN22**

Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist45 Mv_histogram45
15:0	RO	0x0000	ro_mv_hist44 Mv_histogram44

**IEP2 RO MV HIST BIN23**

Address: Operational Base + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist47 Mv_histogram47
15:0	RO	0x0000	ro_mv_hist46 Mv_histogram46

**IEP2 RO MV HIST BIN24**

Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist49 Mv_histogram49
15:0	RO	0x0000	ro_mv_hist48 Mv_histogram48

**IEP2 RO MV HIST BIN25**

Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist51 Mv_histogram51
15:0	RO	0x0000	ro_mv_hist50 Mv_histogram50

**IEP2 RO MV HIST BIN26**

Address: Operational Base + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist53 Mv_histogram54
15:0	RO	0x0000	ro_mv_hist52 Mv_histogram53

**IEP2 RO MV HIST BIN27**

Address: Operational Base + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist55 Mv_histogram55
15:0	RO	0x0000	ro_mv_hist54 Mv_histogram54

**IEP2 PERF LATENCY CTRL0**

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr sw_rd_latency_thr
7:4	RW	0x1	sw_rd_latency_id sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type
2	RW	0x0	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end



Bit	Attr	Reset Value	Description
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enable
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

**IEP2 PERF LATENCY CTRL1**

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x1	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type
1:0	RW	0x1	sw_addr_align_type sw_addr_align_type

**IEP2 PERF RD MAX LATENCY NUM0**

Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 rd_max_latency_num_ch0

**IEP2 PERF RD LATENCY SAMP NUM**

Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 rd_latency_thr_num_ch0

**IEP2 PERF RD LATENCY ACC SUM**

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum rd_latency_acc_sum

**IEP2 PERF WR AXI TOTAL BYTE**

Address: Operational Base + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

**IEP2 PERF WORKING CNT**

Address: Operational Base + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt

**IEP2 PERF RD AXI TOTAL BYTE**

Address: Operational Base + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

**IEP2 MMU DTE ADDR**

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU dte addr

**IEP2 MMU STATUS**

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x1	mmu_idle The MMU is idle when accesses are being translated and there is no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: The MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.
0	RW	0x0	mmu_paging_enabled MMU page enable

**IEP2 MMU CMD**

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled. 3'b000: Enable paging 3'b001: Disable paging 3'b010: Turn on stall mode 3'b011: Turn off stall mode 3'b100: Zap the entire page table cache 3'b101: Leave page fault mode 3'b110: Reset the MMU

**IEP2 MMU PAGE FAULT ADDR**

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr mmu_page_fault_addr

**IEP2 MMU ZAP ONE LINE**

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_zap_one_line Address to be invalidated from the page table cache

**IEP2 MMU INT RAWSTAT**

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

**IEP2 MMU INT CLEAR**

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_clear Read bus error interrupt clear. Write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear Page fault interrupt clear. Write 1 to this register can clear page fault interrupt.

**IEP2 MMU INT MASK**

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_int_en MMU read bus error int enable
0	RW	0x0	page_fault_int_en PAGE fault int enable

**IEP2 MMU INT STATUS**

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

**IEP2 MMU AUTO GATING**

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating When it is 1, the MMU will auto gating itself

**IEP2 MMU ID**

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	mmu_axi_id
3:1	RO	0x0	reserved
0	RW	0x0	reg_load_mmu_en

## Application Notes

**Input source definition constant**

The input source definition must be 16x4 aligned, which means the image width 16 aligned and image height 4 aligned.

**Normal configuration flow**

- Set IEP2 related signals based on current video source information and deinterlace mode (must open frame done interruption by asserting the sw\_iep\_frm\_done\_en signal )
- Set frame start by letting sw\_iep\_frm\_en = 1
- Wait for IEP frame done interruption
- Read back many kinds of Detection data and MVHIST, analyze these data, get the global MV, OSD information etc
- Configure the MV, OSD information back
- Set frame start for deinterlace loop

## Chapter 13 Multi-format Video Encoder and Decoder

### 13.1 Overview

VPU\_Combo is composed by the VDPU345 and VPU121(JPEG only) and VEPU54X to realize the high quality video decoding and encoding. VDPU345 can support such as H265 and H264 decoder. VEPU54X can support H265 and H264 encoder. VPU121 can support JPEG decoder and encoder.

VEPU54X is a high-performance HEVC/H.264 video encoder with the resolution up to 4096x4096. In addition to high objective video quality, its intelligent encoding algorithm can significantly improve subjective quality, especially at low bitrate conditions. VEPU also provides rich application interfaces such as ROI, OSD, link-table which meets different user requirements.

#### 13.1.1 Feature

The features of VDPU345 are listed as follows:

- MMU embedded with MMU interrupt support
- Supports H265 decoding
  - Main Profile up to Level 5.0 High Tier: 4096x2304@30 fps
  - Supports frame timeout interrupt, frame finish interrupt, bus error interrupt and bitstream error interrupt
  - Supports maximum stream bitrate high up to 800MBPS
  - Supports error-mode decoding and error info output
- Supports H264 decoding
  - The following profiles up to Level 5.1: 4096x2304 @30fps
    - ◆ Baseline Profile
    - ◆ Main Profile
    - ◆ High Profile
    - ◆ High 4:2:2 Profile(the 4:2:2 MBAFF feature is not supported)
  - Supports frame timeout interrupt, frame finish interrupt and bitstream error interrupt, buffer empty interrupt
  - Supports slice by slice or random size stream decoding
  - Supports error-mode decoding and error info output

The features of VPU121 are listed as follows:

- Supports JPEG decoding
  - 48x48 to 8176x8176(66.8 Mpixels), Step size 8 pixels
  - Baseline interleaved, and supports ROI (region of image) decode
- Supports JPEG encoding
  - JPEG: Baseline (DCT sequential)
  - JFIF file format 1.02
  - Non-progressive JPEG
  - Support image size from 96x32 to 8192x8192, step size 4 pixels
  - Up to 90 million pixels per second

The primary features of VEPU54X are listed below:

- HEVC main profile encoding, up to level 5.0
- H.264 high profile encoding, up to level 5.1
- Resolution up to 4096x4096
- Intelligent encoding to improve subjective quality
- Block level bitrate control
- Slice split
- Block based ROI configuration
- 8-area OSD
- Support link table mode
- YUV/RGB video source with rotation and mirror
- Frame buffer compression
- MMU inside

### 13.2 VDPU345 and VPU121 Block Diagram

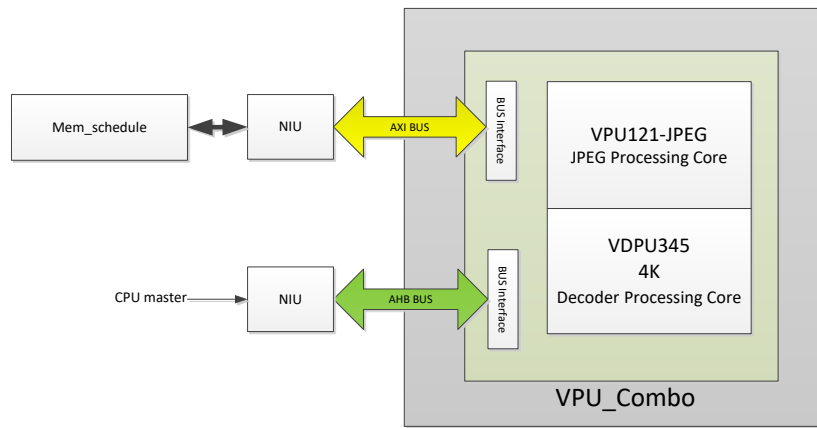


Fig. 13-1 VPU Combo Block Diagram

As shown in the figures above, CPU accesses to the decoder register bank through AHB bus. Bitstream and other necessary data are fed into processing core through AXI read channel, and after several steps of decoding process, decoded pictures and other information data are transferred to designated location in the DDR through AXI write channel.

VPU121 1080P processing core: Support JPEG decoder and encoder.

VDP345 4K decoder processing core: can support h.265/h.264 video standard decoder, max solution size is 4096x2304.

Please note that VPU121 and VDP345 is two IP cores, so such two processing core can be work together.

### 13.3 VEP54X Block Diagram

VEPU54X comprises with:

- TCTRL: top control module
- PRE\_PROC: video source pre-process
- PRE\_ME: coarse motion estimation
- REF\_LDR: reference frame loader
- ME: motion estimation
- INTRA: intra prediction
- MDS: mode decision
- LPF: loop filter
- VLC: variable length coding
- MMU: memory management unit

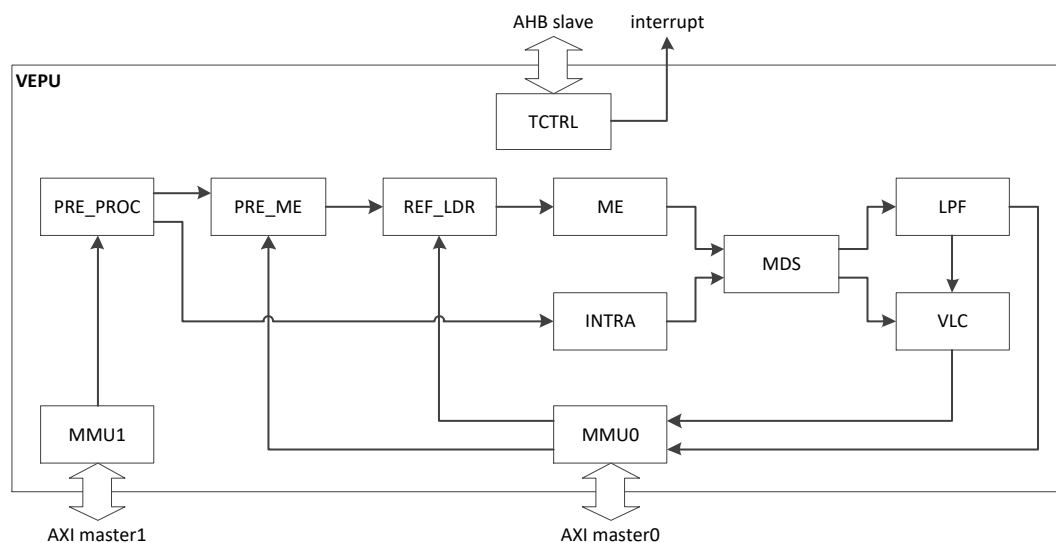


Fig. 13-2 VEP54x Block Diagram

### 13.4 Video frame format

This chapter describes different input and output video frame formats supported by

VCODEC. Each function module has its own supported video frame formats, and this chapter describes all the video frame formats.

### 13.4.1 YCbCr 4:2:0 Planar Format

In the planar format, each video sample component forms one memory plane. Within one plane, the data has to be stored linearly and contiguously in the memory as shown in fellows. The luminance samples are stored in raster-scan order (Y0Y1 Y2Y3 Y4....). The chrominance samples are stored in two planes also in raster scan order (Cb0Cb1 Cb2Cb3 Cb4.... and Cr0Cr1 Cr2Cr3 Cr4....). In this format each pixel takes 12 bits of memory.

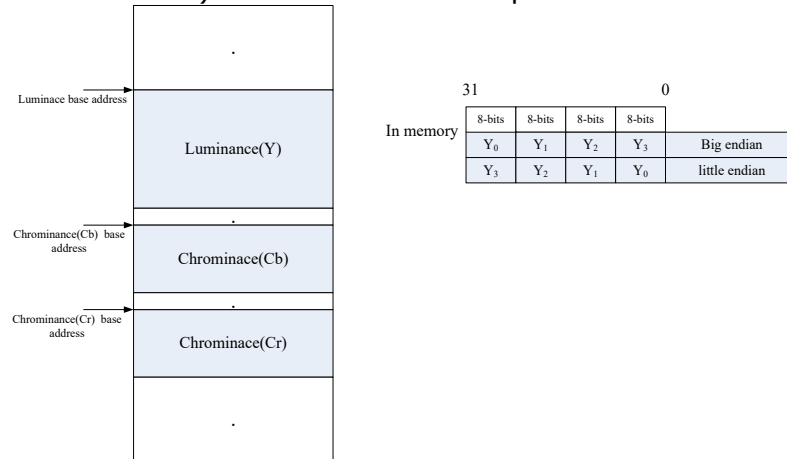


Fig. 13-3 VCODEC YCbCr 4:2:0 planar format

### 13.4.2 YCbCr 4:2:0 Semi-Planar format

In semi-planar YcbCr4:2:0 format the luminance samples from one plane in memory, and chrominance samples from another. Within one plane, the data has to be stored linearly and contiguously in the memory. The luminance pixels are stored in raster-scan order (Y0Y1 Y2Y3 Y4....). The interleaved chrominance CbCr samples are stored in raster-scan order in memory as Cb0Cr0 Cb1Cr1 Cb2 Cr2 Cb3Cr3 Cb4 Cr4....

Semi-Planar format supports both progressive and interlaced format as presented in Fig. 13-4. The interlaced format may be alternative line or each line.

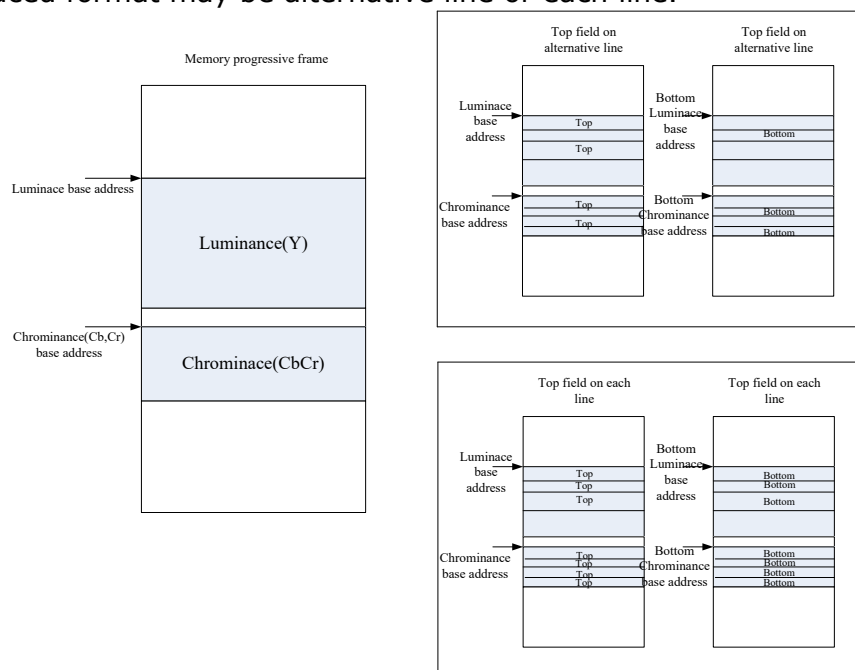


Fig. 13-4 VCODEC YCbCr 4:2:0 Semi-planar format

### 13.4.3 YCbCr 4:2:0 Tiled Semi-Planar Format

Like the YCbCr 4:2:0 semi-planar format, the tiled semi-planar format is also organized in the memory on two separate planes. The difference between these formats is that in tiled format the pixel samples are not anymore in raster-scan order but are stored macroblock (16x16 pixels) by macroblock. The samples of each macroblock are stored in consecutive

addresses and the macroblocks are ordered from left to right and from top to down as Fig. 13-5. When this format used as input data format, it causes the lowest bus load to the system as there is minimal amount of non-sequential memory addressing required when reading the input data to the post-processor.

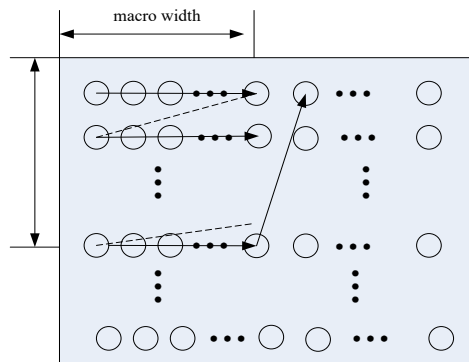


Fig. 13-5 VCODEC Tile scan mode

#### 13.4.4 YCbCr 4:2:2 Interleaved Format

In the interleaved YCbCr 4:2:2 format the pixel samples from a single plane in which the data has to be stored linearly and contiguously as shown in Fig. 13-6. The pixel data is in raster scan order and the chrominance samples are interleaved between the luminance samples as Y0Cb0 Y1Cr0 Y2 Cb1 Y3Cr1 Y4 Cb2.... YCrCb, CbYCrY and CrYCbY component orders are supported also. In this format, each pixel takes 16 bits in the memory.

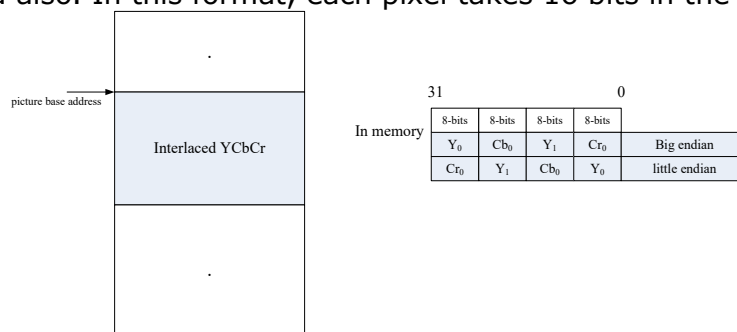


Fig. 13-6 VCODEC YCbCr4:2:2 Interleaved format

#### 13.4.5 AYCbCr 4:4:4 Interleaved Format

In the interleaved YcbCr 4:2:2 format, the pixel samples from a single plane in which the data has to be stored linearly and contiguously as show in Fig. 13-7. The pixel data is in raster scan order and the chrominance and alpha channel samples are interleaved between the luminance samples as A0Y0 Cb0Cr0 A1 Y1 Cb1Cr1....

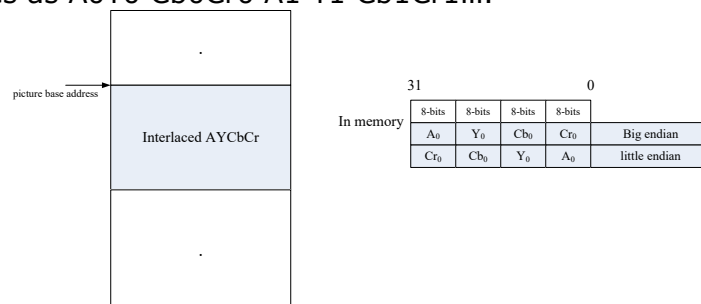


Fig. 13-7 VCODEC AYCbCr 4:4:4 Interleaved format

#### 13.4.6 RGB 16bpp Format

In this format each pixel is represented by 16 or less bits containing the red, blue and green samples. There are several 16bpp formats which use different number of bits for each sample. For example the RGB 5-5-5 format uses 5 bits for each sample and 1 bit is left unused or can represent a transparency flag, where RGB 5-6-5 uses 6 bits for the G sample and 5 bits for R and B samples. Common for all 16bpp types is that two pixels fit into one 32-bit space.



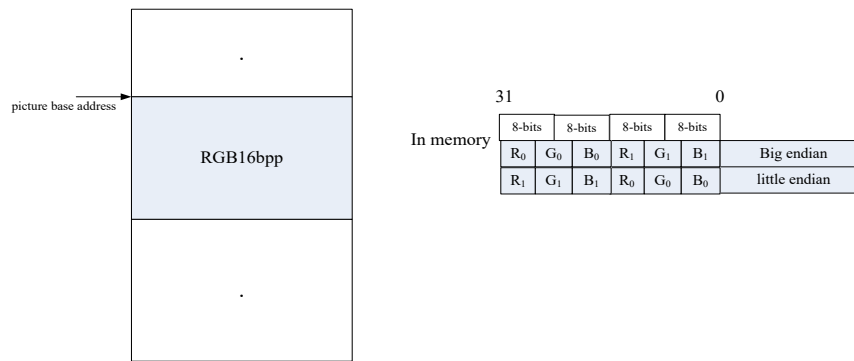


Fig. 13-8 VCODEC RGB 16bpp format

### 13.4.7 RGB 32bpp Format

Any RGB format that has its pixels represented by more than 16bits each is considered to be of 32bpp type. Typically in this format each pixel is represented by three bytes containing a red, blue and green sample and a 4th byte which can be empty or hold an alpha blending value. Common for all 32bpp types is that only one pixel fit into one 32-bit space. The data has to be stored linearly and contiguously in the memory.

## 13.5 Function Description

### 13.5.1 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

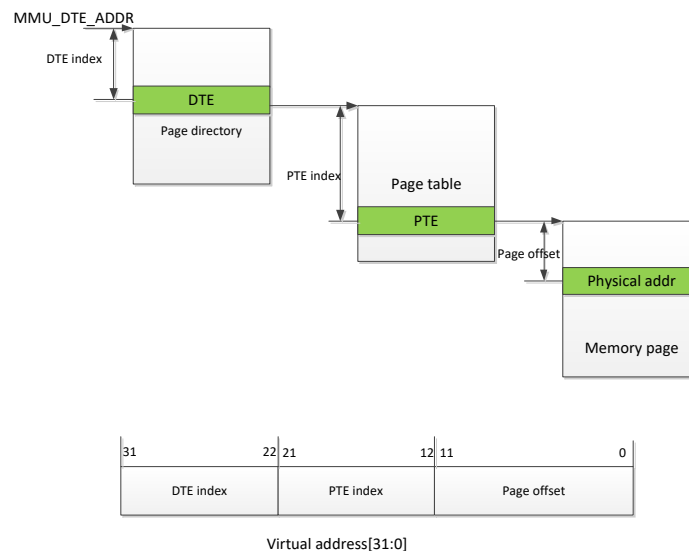


Fig. 13-9 structure of two-level page table

### 13.5.2 VEPU121 feature supported

#### 1. JPEG encoder

The JPEG features supported by encoder are shown as follows.

Table 13-1 Video Jpeg encoder feature

Feature	Encoder support
Input data format	YCbCr formats: YCbCr 4:2:0 planar YCbCr 4:2:0 semi-planar YCbYCr 4:2:2①

Feature	Encoder support
	CbYCrY 4:2:2 Interleaved <sup>①</sup> RGB formats:① RGB444 to BGR444 RGB555 to BGR555 RGB565 to BGR565 RGB888 to BRG888 RGB101010 and BRG 101010
Output data format	JFIF FILE format 1.02 Non-progressive JPEG
Supported image size	96x96 to 8192x8192(64 million pixels) Step size 4 pixels
Maximum Data rate	Up to 90 million pixels per second

①Internally encoder handles image only in 4:2:0 format

### 13.5.3 VDPUI21 feature supported

#### 1. JPEG Decoder

JPEG features supported by decoder are as shown in fellows:

Table 13-2 Video Jpeg decoder feature

Feature	Decoder support
Input data format	JFIF file format 1.02 YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Decoding scheme	Input: Buffer by buffer, from 5Kb to 8MB at a time <sup>①</sup> Output: from 1 MB row to 16 Mpixels at a time <sup>②</sup>
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Supported image size	48x48 to 8176x8176(66.8 Mpixels) Step size 8 pixels <sup>③</sup>
Maximum frame rate	Up to 76 million pixels pre second
Maximum bit rate	As specified by the specification
Thumbnail decoding	JPEG compressed thumbnails supported
Error detection	Supported

### 13.5.4 VDPUI345 feature supported

#### 1. H265/MVC

Table 13-3 Video H.265 decoder features

Feature	Decoder support
Input data format	H265 byte unit stream/MVC stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 Semi-Planar
Supported image size	64x64 to 4096x2304 step size 16pixels
Profile/level	Main level 5.0
Maximum frame rate	YCbCr 4:2:0 30fps @4096x2304
Maximum bit rate	800MBPS
Error detection And concealment	Supported

#### 2. H264/MVC

Table 13-4 Video H.264 decoder features

Feature	Decoder support
Input data format	H264byte or NAL unit stream/SVC stream/MVC stream

Feature	Decoder support
Decoding scheme	Frame by frame(or field by field) Slice by slice
Output data format	YCbCr 4:0:0 (monochrome) YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:2 semi-planar raster-scan
Supported image size	16x16 to 4096x2304 step size 16 pixels
Profile and Level	Main level 5.1
Maximum frame rate	30fps @4096x2304
Maximum bit rate	-
Error detection And concealment	Supported

### 13.5.5 VDPU345 Config Register Linked List Pointer mode(LLP mode)

VDPU345 Video decoder support link table mode to improve decoder continuity and reduce CPU participate and interrupt response time. In this mode, the register which used for config will be prepare into DDR, after that user enable link table mode, and then our decoder will fetch the register config information through AXI bus frame by frame. On link table mode, the decoder will auto finish all the frame decoder which be prepared in DDR, and not need CPU participate.

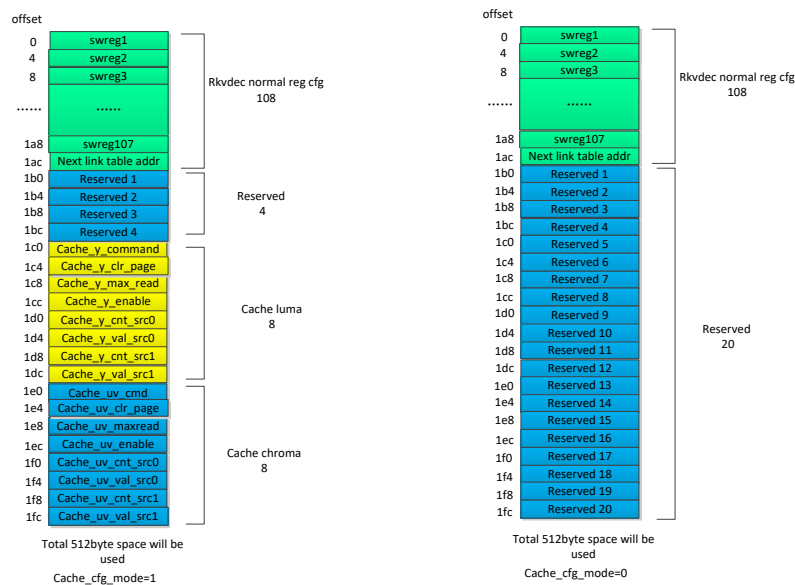


Fig. 13-10 Link table register prepare in DDR format

As show in the above Fig, Link table register prepare in DDR format, each frame config information need 512bytes in DDR. We have two cache config mode, you can use link\_table\_swreg0[1] to select, if cache\_cfg\_mode=1,user should prepare cache config information to DDR, otherwise, user can doesn't care cache config, hardware will auto select the best to config.

After hardware decoder one frame, will write back some information to DDR where the write back base address is current config storage addr base. All the write back information are listed in the follows table.

Table 13-5 Link table write back register

offset	Description
0x0	{1'b0, sw_colmv_compress_en, sw_allow_16x8_cp_flag, sw_fbc_e,

offset	Description
	1'b1, pps_no_ref_bframe_dec, sw_allow_not_wr_unref_bframe, sw_scl_down_en, sw_wr_ddr_align_en, sw_softreset_rdy, sw_force_softreset_valid, sw_softrst_en_p, sw_h264orvp9_error_mode, sw_cabu_end_sta, sw_colmv_ref_error_sta, sw_buf_empty_sta, sw_dec_timeout_sta, sw_dec_error_sta, sw_dec_bus_sta, sw_dec_rdy_sta, sw_dec_commonirq_mode, 1'b0, sw_dec_irq_raw, sw_dec_irq, sw_strmerror_waitdecfifo_empty, sw_buf_empty_en, sw_dec_timeout_e, sw_dec_irq_dis, sw_timeout_mode, sw_dec_e_strmd_clkgate_dis, sw_dec_clkgate_e, 1'b0}
0x4	{sw_colmv_ref_pidx[3:0],sw_cabac_error_status[27:0]}
0x8	{7'b0,sw_vp9_reg_error_ctu0_en,1'b0,sw_streamfifo_space2full[6:0],sw_cabac_error_ctu_offset[15:0]}
0xc	{sw_strm_rlc_base,4'b0}
0x10	{payload_total_bytes[31:0]}
0x14	{swreg100_axi_perf_ctrl[19:1],swreg101_axi_perf_ctrl[12:0]}
0x18	{16'h0,perf_rd_max_latency_num[15:0]}
0x1c	perf_rd_latency_samp_num[31:0]
0x20	perf_rd_latency_acc_sum[31:0]
0x24	perf_rd_axi_total_byte[31:0]
0x28	perf_wr_axi_total_byte[31:0]
0x2c	perf_working_cnt[31:0]
0x30	error_infomation_0
0x34	error_infomation_1
0x38	{inter_sw_mv_x_pu_cnt_sum[14:0],dec_sw_ctu_num[16:0]}
0x3c	inter_sw_reflst_idx_use[31:0]
0x40	{inter_sw_mv_y_pu_cnt_sum[6:0], inter_sw_mv_x_pu_cnt_sum[19:15], inter_sw_pu_cnt_sum[19:0]}
0x44	{min_of_mv_y[15:0],min_of_mv_x[15:0]}
0x48	{max_of_mv_y[15:0],max_of_mv_x[15:0]}
0x4c	{sum_of_mv_x[31:0]}
0x50	{sum_of_mv_y[31:0]}
0x54	{sum_of_abs_mv_x[31:0]}
0x58	{sum_of_abs_mv_y[31:0]}
0x5c	{sum_of_abs_mv_y[39:32], sum_of_abs_mv_x[39:32],

offset	Description
	sum_of_mv_y[39:32], sum_of_mv_x[39:32]}
0x60	{3'd0,inter_sw_mv_y_pu_cnt_sum[19:7],cu8x8_skip_num[15:0]}
0x64	the tu skip number
0x68	{8'b0,cr_qp_max[7:0],cb_qp_max[7:0],luma_qp_max[7:0]}
0x6c	{8'b0,cr_qp_min[7:0],cb_qp_min[7:0],luma_qp_min[7:0]}
0x70	the sum of luma qp
0x74	the sum of cb qp
0x78	the sum of cr qp
0x7c	{last_correct_ctu_yoffset[15:0],last_correct_ctu_xoffset[15:0]}

The base address of config link table mode is RKVDEC\_BASE+0x300.

### 13.5.6 VDP345 Qos mode

In VDP345 hardware, we support QOS mode, in this mode, we can request high priority to fetch data, you can control QOS work by config swreg99 and swreg108. For more detail, you can see the register description.

User should accord to the soc system to select appropriate level.

### 13.5.7 VDP345 Error Processing

#### 1. Error types

Table 13-6 VDP345 Error Types

Error type	Description
timeout error	The VDP345 IP will monitor if it was always be hold on idle state, and if it stay on IDLE too much long times, will give timeout error.
bus error	It will detect the axi data read and write, if there have any error happened, if it done, it will give bus error.
refer frame error	If the reference frame required by the decoder which is invalid, the hardware will give reference frame error.
stream error	If the stream meet some error, such as stream packet loss, some syntax elements value are irrationality, it will give an stream error.
mmu page fault	If the mmu page is not ready, but used by decoder, the decoder will give an mmu page fault interrupt, and after that, the software should go to prepare the missing mmu page on DDR and config hardware continue to decoder.
LLP work error	If any error happened when LLP work mode be activated, the decoder will stop next frame decoding, and then give an error interrupt, wait soft to process.

The decoder should need to be reset no matter what error types be detected. For decoder reset, it have two reset mode, you can let hardware reset itself if any error happened, or you also can select use software to config cru reset, you can config swreg2[23] to select the mode.

### 13.5.8 VDP345 Decoder Output Frame Buffer Size Requested

We define variables  $\text{ceil}(M(N))$  as follows:

$$\text{ceil}(M,N)=\text{ceil}M(N)=((N+M-1)/M)*M$$

#### 1) . LLP register buffer size

For LLP work mode, LLP register buffer will be required. Every frame will require 512 byte DDR space. Then, buffer size calculate formula be defined as follows:

$$\text{LLP\_register\_buffer\_size} = \text{frame\_num} * 512 \text{byte}$$

There frame\_num is the number of frame will be prepare in DDR when work on LLP mode.

#### 2). Output frame decoder buffer size

If output select YCbCr 4:2:0 semi-planar raster-scan format, you can use follows formula to calculate the decoder frame buffer size.

$$\text{luma\_frame\_buffer\_size} = y\_vir\_hor\_stride * pic\_h * bit\_depth\_y / 8$$

$$\text{chroma\_frame\_buffer\_size} = uv\_vir\_hor\_stride * (pic\_h / 2) * bit\_depth\_c / 8$$

$$frame\_buffer\_size = luma\_frame\_buffer\_size + chroma\_frame\_buffer\_size$$

There:

- `y_vir_hor_stride`: The virtual stride of luma, it must should more bigger than picture width
- `uv_vir_hor_stride`: The virtual stride of chroma, it must should more big than picture width for YCbCr 4:2:0
- `bit_depth_y/c`: Main10 or main, its value will be 10 or 8

3). Output frame colmv buffer size

If colmv compress be disabled, you can use follows formula to calculate the decoder frame buffer size.

Table 13-7 Colmv uncompress info

Format	Colmv_size	Colmv space(bytes unit)
h264	4x4	8
hevc	16x16	16
vp9	8x8	16
avs2	16x16	8

So, the colmv uncompress size is:

$$colmv\_buffer\_size0 = (ceil64(pic\_w) * ceil64(pic\_h) / (colmv\_size * colmv\_size)) * colmv\_bytes$$

The buffer size unit is byte unit.

4). Tile column buffer size

If the video stream include TILE split, this buffer buffer will be required, and we can use the follows formula to calculate the TILE column buffer size.

$$tile\_col\_buffer\_size = (ceil64(pic\_h) + 64) * 60$$

The buffer size unit is byte unit.

5). Error info buffer size

If error infomation be enable write to DDR, the error info buffer size will be required, and we can use the follows formula to calculate the error info buffer size.

$$error\_info\_buffer\_size = ceil2(slice\_num) * 8$$

only h264 and h265 support error info output.

### 13.5.9 VEPUS4X H.264 or HEVC Encoding

VEPU can perform one frame H.264 or HEVC encoding by register configuration. User should allocate DDR buffer, configure VEPU through AHB slave port, and then wait for frame finish interrupt.

VEPU also have batch processing mode (the so called link-table mode). User should configure the link table node in DDR, start VEPU, and then wait for frame or sequence finish. User can also add new frames to be encoded while VEPU is processing the previous one.

### 13.5.10 VEPUS4X Video Source Pre-process

VEPU can read video source of different color formats such as ARGB, RGB, YUV422/420 P/SP, and Arm AFBC YUV422/420. It also supports image clipping, rotation, mirror and OSD insertion.

### 13.5.11 VEPUS4X ROI Configuration

User can configure QP and I/P selection for each 16x16 block through VEPU ROI configuration.

## 13.6 Register Description

### 13.6.1 Internal Address Mapping

This section describes the control/status registers of the codec.

If VDPUS45 decoder is chosen to work, the register base address is VDPUS45\_base.

If VDPUS121 decoder is chosen to work, the register base address is VDPUS121\_base.

If VEPUS121 encoder is chosen to work, the register base address is VDPUS121\_base.

All the register config base are listed as follows:

Table 13-8 Base address of config

Config Register	Base addr
VDPUS45 function config base	VDPUS45_base
VDPUS45 mmu config base	VDPUS45_base+0x480 for read channel

Config Register	Base addr
	VDPU345_base+0x4c0 for write channel
VDPU345 cache config base	VDPU345_base+0x400 for luma channel VDPU345_base+0x440 for chroma channel
VDPU345 link table config base	VDPU345_base+0x300
VDPU121 function config base	VDPU121_base
VDPU121 mmu config base	VDPU121_base+0x400
VEPU121 function config base	VEPU121_base
VEPU121 mmu config base	VEPU121_base+0x800

Table 13-9 Base address value

Base addr	value
VDPU345_base	0xFFB8_0000
VDPU121_base	0xFFB9_0400
VEPU121_base	0xFFB9_0000

Because of that VEPU54X has lots of configuration registers, they are divided into two layers: LAYER1 and LAYER2. The registers in LAYER1 can be accessed directly, while LAYER2's registers are accessed through the registers of L2CFG\_ADDR(0x03f0), L2CFG\_WDATA(0x03f4) and L2CFG\_RDATA(0x03f8) in LAYER1, just like secondary addressing.

Note that layer2's registers are address separately.

### 13.6.2 VEPU121 Registers Summary

Name	Offset	Size	Reset Value	Description
<u>VEPU_swreg_0</u>	0x0000	W	0x00000000	1st quantization for jpeg lumen table
<u>VEPU_swreg_1</u>	0x0004	W	0x00000000	2st quantization for jpeg lumen table
<u>VEPU_swreg_2</u>	0x0008	W	0x00000000	3st quantization for jpeg lumen table
<u>VEPU_swreg_3</u>	0x000c	W	0x00000000	4st quantization for jpeg lumen table
<u>VEPU_swreg_4</u>	0x0010	W	0x00000000	5st quantization for jpeg lumen table
<u>VEPU_swreg_5</u>	0x0014	W	0x00000000	6st quantization for jpeg lumen table/part 1 for qp round
<u>VEPU_swreg_6</u>	0x0018	W	0x00000000	7st quantization for jpeg lumen table
<u>VEPU_swreg_7</u>	0x001c	W	0x00000000	8st quantization for jpeg lumen table
<u>VEPU_swreg_8</u>	0x0020	W	0x00000000	9st quantization for jpeg lumen table
<u>VEPU_swreg_9</u>	0x0024	W	0x00000000	10st quantization for jpeg lumen table
<u>VEPU_swreg_10</u>	0x0028	W	0x00000000	11st quantization for jpeg lumen table
<u>VEPU_swreg_11</u>	0x002c	W	0x00000000	12st quantization for jpeg lumen table
<u>VEPU_swreg_12</u>	0x0030	W	0x00000000	13st quantization for jpeg lumen table
<u>VEPU_swreg_13</u>	0x0034	W	0x00000000	14st quantization for jpeg lumen table
<u>VEPU_swreg_14</u>	0x0038	W	0x00000000	15st quantization for jpeg lumen table
<u>VEPU_swreg_15</u>	0x003c	W	0x00000000	16st quantization for jpeg lumen table

Name	Offset	Size	Reset Value	Description
<u>VEPU swreg 16</u>	0x0040	W	0x00000000	1st quantization for jpeg chroma table
<u>VEPU swreg 17</u>	0x0044	W	0x00000000	2st quantization for jpeg chroma table
<u>VEPU swreg 18</u>	0x0048	W	0x00000000	3st quantization for jpeg chroma table
<u>VEPU swreg 19</u>	0x004c	W	0x00000000	4st quantization for jpeg chroma table
<u>VEPU swreg 20</u>	0x0050	W	0x00000000	5st quantization for jpeg chroma table
<u>VEPU swreg 21</u>	0x0054	W	0x00000000	6st quantization for jpeg chroma table
<u>VEPU swreg 22</u>	0x0058	W	0x00000000	7st quantization for jpeg chroma table
<u>VEPU swreg 23</u>	0x005c	W	0x00000000	8st quantization for jpeg chroma table/part 3 for qp round
<u>VEPU swreg 24</u>	0x0060	W	0x00000000	9st quantization for jpeg chroma table
<u>VEPU swreg 25</u>	0x0064	W	0x00000000	10st quantization for jpeg chroma table
<u>VEPU swreg 26</u>	0x0068	W	0x00000000	11st quantization for jpeg chroma table
<u>VEPU swreg 27</u>	0x006c	W	0x00000000	12st quantization for jpeg chroma
<u>VEPU swreg 28</u>	0x0070	W	0x00000000	13st quantization for jpeg chroma
<u>VEPU swreg 29</u>	0x0074	W	0x00000000	14st quantization for jpeg chroma
<u>VEPU swreg 30</u>	0x0078	W	0x00000000	15st quantization for jpeg chroma
<u>VEPU swreg 31</u>	0x007c	W	0x00000000	16st quantization for jpeg chroma
<u>VEPU swreg 44</u>	0x00b0	W	0x00000000	Intra slice bitmap
<u>VEPU swreg 45</u>	0x00b4	W	0x00000000	Intra slice bitmap1
<u>VEPU swreg 46</u>	0x00b8	W	0x00000000	Intra macro block select register
<u>VEPU swreg 47</u>	0x00bc	W	0x00000000	CIR intra control register
<u>VEPU swreg 48</u>	0x00c0	W	0x00000000	Base addr for input luma
<u>VEPU swreg 49</u>	0x00c4	W	0x00000000	Base address for input cb
<u>VEPU swreg 50</u>	0x00c8	W	0x00000000	Input cr start address
<u>VEPU swreg 51</u>	0x00cc	W	0x00000000	Stream header bits left register
<u>VEPU swreg 52</u>	0x00d0	W	0x00000000	Stream header bits left register
<u>VEPU swreg 53</u>	0x00d4	W	0x00000000	Stream buffer register
<u>VEPU swreg 54</u>	0x00d8	W	0x01010000	Axi control register
<u>VEPU swreg 55</u>	0x00dc	W	0x00000000	Qp related
<u>VEPU swreg 56</u>	0x00e0	W	0x00000000	The luma reference frame start address
<u>VEPU swreg 57</u>	0x00e4	W	0x00000000	The chroma reference frame start address
<u>VEPU swreg 58</u>	0x00e8	W	0x00000000	The result of qp sum div2
<u>VEPU swreg 59</u>	0x00ec	W	0x00000000	H264 slice ctrl
<u>VEPU swreg 60</u>	0x00f0	W	0x00000000	Spill ctrl
<u>VEPU swreg 61</u>	0x00f4	W	0x00000000	Input luminance information
<u>VEPU swreg 62</u>	0x00f8	W	0x00000000	Rlc_sum
<u>VEPU swreg 63</u>	0x00fc	W	0x00000000	The reconstructed luma start address
<u>VEPU swreg 64</u>	0x0100	W	0x00000000	The reconstructed chroma start address
<u>VEPU swreg 65 reuse</u>	0x0104	W	0x00000000	Checkpoint 1 and 2



Name	Offset	Size	Reset Value	Description
VEPU swreg 66 reuse	0x0108	W	0x00000000	Checkpoint 3 and 4
VEPU swreg 67 reuse	0x010c	W	0x00000000	Checkpoint 5 and 6
VEPU swreg 68 reuse	0x0110	W	0x00000000	Checkpoint 7 and 8
VEPU swreg 69 reuse	0x0114	W	0x00000000	Checkpoint 9 and 10
VEPU swreg 70 reuse	0x0118	W	0x00000000	Checkpoint word error 1 and 2
VEPU swreg 71 reuse	0x011c	W	0x00000000	Checkpoint word error 1 and 2
VEPU swreg 72 reuse	0x0120	W	0x00000000	Checkpoint word error 1 and 2
VEPU swreg 73 reuse	0x0124	W	0x00000000	Checkpoint delta QP register
VEPU swreg 74	0x0128	W	0x00000000	Input image format
VEPU swreg 75	0x012c	W	0x00000000	Intra/inter mode
VEPU swreg 76 reuse	0x0130	W	0x00000000	Encoder control register 0
VEPU swreg 77	0x0134	W	0x00000000	Output stream start address
VEPU swreg 78	0x0138	W	0x00000000	Output control start address
VEPU swreg 79	0x013c	W	0x00000000	Next picture luminance start address
VEPU swreg 80	0x0140	W	0x00000000	Base address for MV output
VEPU swreg 81	0x0144	W	0x00000000	The cabac table start address
VEPU swreg 82	0x0148	W	0x00000000	ROI area register
VEPU swreg 83	0x014c	W	0x00000000	The second of ROI area register
VEPU swreg 84	0x0150	W	0x00000000	Stabilization matrix1
VEPU swreg 85	0x0154	W	0x00000000	Stabilization matrix2
VEPU swreg 86	0x0158	W	0x00000000	Stabilization matrix3
VEPU swreg 87	0x015c	W	0x00000000	Stabilization matrix4
VEPU swreg 88	0x0160	W	0x00000000	Stabilization matrix5
VEPU swreg 89	0x0164	W	0x00000000	Stabilization matrix6
VEPU swreg 90	0x0168	W	0x00000000	Stabilization matrix7
VEPU swreg 91	0x016c	W	0x00000000	Stabilization matrix8
VEPU swreg 92	0x0170	W	0x00000000	Stabilization matrix9
VEPU swreg 93	0x0174	W	0x00000000	The output of Stabilization motion sum
VEPU swreg 94	0x0178	W	0x00000000	Output of Stabilization
VEPU swreg 95	0x017c	W	0x00000000	RGB to YUV conversion coefficient register
VEPU swreg 96	0x0180	W	0x00000000	RGB to YUV conversion coefficient register
VEPU swreg 97	0x0184	W	0x00000000	RGB to YUV conversion coefficient register
VEPU swreg 98	0x0188	W	0x00000000	RGA MASK
VEPU swreg 99	0x018c	W	0x00000000	Mv related
VEPU swreg 100 reuse	0x0190	W	0x00000000	QP register
VEPU swreg 101 read	0x0194	W	0x1f522780	Hw config reg
VEPU swreg 102	0x0198	W	0x00000000	Mvc related
VEPU swreg 103	0x019c	W	0x00000000	Encoder start
VEPU swreg 104	0x01a0	W	0x00000000	Mb control register
VEPU swreg 105	0x01a4	W	0x00000000	Swap ctrl register
VEPU swreg 106 reuse	0x01a8	W	0x00000000	Encoder control register 1
VEPU swreg 107 reuse	0x01ac	W	0x00000000	JPEG control register
VEPU swreg 108 reuse	0x01b0	W	0x00000000	Intra slice bmp2
VEPU swreg 109	0x01b4	W	0x00001000	Encoder status
VEPU swreg 110 read	0x01b8	W	0x48311220	Product ID

Name	Offset	Size	Reset Value	Description
VEPU swreg 120 183	0x01e0	W	0x00000000	Addr range: 0x01e0~0x02dc Swreg120: DMV 4p/1p penalty table values Swreg121: DMV 4p/1p penalty table values Swreg122: DMV 4p/1p penalty table values Swreg123: DMV 4p/1p penalty table values ..... Swreg183: DMV 4p/1p penalty table values

Notes: **Size: B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.3 VEPU121 Detail Registers Description

#### VEPU swreg 0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant1 Jpeg luma quantization 1

#### VEPU swreg 1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant2 Jpeg luma quantization 2

#### VEPU swreg 2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant3 Jpeg luma quantization 3

#### VEPU swreg 3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant4 Jpeg luma quantization 4

#### VEPU swreg 4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant5 Jpeg luma quantization 5

#### VEPU swreg 5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant6 Jpeg luma quantization 6

#### VEPU swreg 6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant7 Jpeg luma quantization 7

**VEPU swreg 7**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant8 Jpeg luma quantization 8

**VEPU swreg 8**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant9 Jpeg luma quantization 9

**VEPU swreg 9**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant10 Jpeg luma quantization 10

**VEPU swreg 10**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant11 Jpeg luma quantization 11

**VEPU swreg 11**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant12 Jpeg luma quantization 12

**VEPU swreg 12**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant13 Jpeg luma quantization 13

**VEPU swreg 13**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant14 Jpeg luma quantization 14

**VEPU swreg 14**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant15 Jpeg luma quantization 15

**VEPU swreg 15**

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	Reserved
7:0	RW	0x00	Sw_jpeg_luma_quant16 Jpeg luma quantization 16

**VEPU swreg 16**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant1 Jpeg chroma quantization 1

**VEPU swreg 17**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant2 Jpeg chroma quantization 2

**VEPU swreg 18**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant3 Jpeg chroma quantization 3

**VEPU swreg 19**

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant4 Jpeg chroma quantization 4

**VEPU swreg 20**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant5 Jpeg chroma quantization 5

**VEPU swreg 21**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant6 Jpeg chroma quantization 6

**VEPU swreg 22**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant7 Jpeg chroma quantization 7

**VEPU swreg 23**

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant8 Jpeg chroma quantization 8

**VEPU swreg 24**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant9 Jpeg chroma quantization 9

**VEPU swreg 25**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant10 Jpeg chroma quantization 10

**VEPU swreg 26**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	Reserved
8:0	RW	0x000	Sw_jpeg_chroma_quant11 Jpeg chroma quantization 11

**VEPU swreg 27**

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant12 Jpeg chroma quantization 12

**VEPU swreg 28**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	Reserved
11:0	RW	0x000	Sw_jpeg_chroma_quant13 Jpeg chroma quantization 13

**VEPU swreg 29**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant14 Jpeg chroma quantization 14

**VEPU swreg 30**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	Reserved
11:0	RW	0x000	Sw_jpeg_chroma_quant15 Jpeg chroma quantization 15

**VEPU swreg 31**

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant16 Jpeg chroma quantization 16

**VEPU swreg 44**

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Intra_slice_bmp0 Bit0 : Slices0 Bit1 : Slices1 Bit2 : Slices2 ..... Bit31 : Slices31

**VEPU swreg 45**

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Intra_slice_bmp1 Bit0 : Slices32 Bit1 : Slices33 Bit2 : Slices34 ..... Bit31 : Slices63

**VEPU swreg 46**

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Intra_up_mb_area The top intra macro block's area used in row.
23:16	RW	0x00	Intra_down_mb_area The bottom intra macro block's area used in row.
15:8	RW	0x00	Intra_left_mb_area The left intra macro block's area used in column.
7:0	RW	0x00	Intra_right_mb_area The right intra macro block's area used in column.

**VEPU swreg 47**

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Cir_first_intra 16'd0: Disable Other: Enable and be set
15:0	RW	0x0000	Cir_intra_mb_itvl 16'd0: Disable Other: Enable and be set

**VEPU swreg 48**

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Luma_in_st_adr Input luma start address

**VEPU swreg 49**

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Cb_in_st_adr Input cb start address

**VEPU swreg 50**

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Cr_in_st_adr Input cr start address

**VEPU swreg 51**

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Strm_header_left_hbits The high 32 bit of stram header be left.

**VEPU swreg 52**

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Strm_header_left_lbits The low 32 bit of stram header be left.

**VEPU swreg 53**

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Strm_bufsize_lmt The limit size of steam buffer.

**VEPU swreg 54**

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	Axi_rd_id If config 0,it will be modify as 1 by HW auto
23:16	RW	0x01	Axi_wr_id If config 0,it will be modify as 1 by HW auto
15:14	RO	0x0	Reserved
13:8	RW	0x00	Burst_len Burst length
7:3	RO	0x00	Reserved
2	RW	0x0	Burst_incr_mod_sel 1'b0: Single burst selected 1'b1: Incr burst selected
1	RW	0x0	Burst_discard 1'b0: Disable, off 1'b1: Enable, on
0	RW	0x0	Burst_disable 1'b0: Enable 1'b1: Disable

**VEPU swreg 55**

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15:12	RW	0x0	Roi_dlt_qp1 1st for delta qp for roi
11:8	RW	0x0	Roi_dlt_qp2 2st for delta qp for roi
7:4	RO	0x0	Reserved
3:0	RW	0x0	Qp_adjst Signed register; Range from -8 to 7

**VEPU swreg 56**

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Luma_ref_st_adr The luma reference frame start address

**VEPU swreg 57**

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Chroma_ref_st_adr The chroma reference frame start address

**VEPU swreg 58**

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:11	RW	0x0000000	Qp_sum_div2 The result of (qp sum)/2

**VEPU swreg 59**

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Reserved
28	RW	0x0	H264_qurt_pixmv_dis 1'b1: Disable 1'b0: Default, enable
27:26	RO	0x0	Reserved
25:24	RW	0x0	Dblkingflt_mode 2'd0: Enabled 2'd1: Disabled 2'd2: Disabled on slice
23	RO	0x0	Reserved
22:21	RW	0x0	H264_cabac_idc 2'd0,2'd1,2'd2: Used 2'd3: No use
20	RW	0x0	Entry_code_fmt H.264: 1'b0: Cavlc 1'b1: Cabac
19:18	RO	0x0	Reserved
17	RW	0x0	H264_trfmod_8x8 On-off for 8x8 transform used in h264
16	RW	0x0	H264_res_intermod_4x4 The restriction inter mode selected in 4x4 block
15	RW	0x0	H264_strm_mod_sel 1'b0: NAL unit 1'b1: BYTE
14:8	RW	0x00	H264_slice_num 0: One slice in current picture 1: Two slice in current picture .....

**VEPU swreg 60**

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved



Bit	Attr	Reset Value	Description
21:16	RW	0x00	Strm_st_offset
15:8	RW	0x00	Skip_mb_mode H264: SKIP macroblock mode
7:6	RO	0x0	Reserved
5:4	RW	0x0	Right_spill Div4 value Range: 0~3
3:0	RW	0x0	Bot_spill The bottom edge of image for spill pixels

**VEPU swreg 61**

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22:20	RW	0x0	Offset_in_chroma Byte unit
19	RO	0x0	Reserved
18:16	RW	0x0	Offset_in_luma Byte unit
15:14	RO	0x0	Reserved
13:0	RW	0x0000	Row_len_in_luma

**VEPU swreg 62**

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved
21:0	RW	0x0000000	Rlc_sum Rlc_sum

**VEPU swreg 63**

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Recon_luma_st_adr The reconstructed luma start address

**VEPU swreg 64**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Recon_chroma_st_adr The reconstructed chroma start address

**VEPU swreg 65 reuse**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_1 1st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_2 2st word used for check point used in h.264

**VEPU swreg 66 reuse**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_3 3st word used for check point used in h.264

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	H264_chkpt_4 4st word used for check point used in h.264

**VEPU swreg 67 reuse**

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_5 5st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_6 6st word used for check point used in h.264

**VEPU swreg 68 reuse**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_7 7st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_8 8st word used for check point used in h.264

**VEPU swreg 69 reuse**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_9 9st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_10 10st word used for check point used in h.264

**VEPU swreg 70 reuse**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_errchkpt_1 1st word error check point used in h.264
15:0	RW	0x0000	H264_errchkpt_2 2st word error check point used in h.264

**VEPU swreg 71 reuse**

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_errchkpt_3 3st word error check point used in h.264
15:0	RW	0x0000	H264_errchkpt_4 4st word error check point used in h.264

**VEPU swreg 72 reuse**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_errchkpt_5 5st word error check point used in h.264
15:0	RW	0x0000	H264_errchkpt_6 6st word error check point used in h.264

**VEPU swreg 73 reuse**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:24	RW	0x0	Chkqp_1 1st for delta qp check point
23:20	RW	0x0	Chkqp_2 2st for delta qp check point
19:16	RW	0x0	Chkqp_3 3st for delta qp check point
15:12	RW	0x0	Chkqp_4 4st for delta qp check point
11:8	RW	0x0	Chkqp_5 5st for delta qp check point
7:4	RW	0x0	Chkqp_6 6st for delta qp check point
3:0	RW	0x0	Chkqp_7 7st for delta qp check point

**VEPU swreg 74**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:24	RW	0x00	Mad_thsld Value = (MAD threshold)/256
23:16	RW	0x00	Encoded_slices The number of encoder slices which used in h.264
15:8	RO	0x00	Reserved
7:4	RW	0x0	Img_fmt_in YUV420P YUV420SP YUV422 UYVY422 RGB565 RGB444 RGB888 RGB101010
3:2	RW	0x0	Img_in_rot 2'd0: No rotation 2'd1: Rotate right 90 degress 2'd2: Rotate left 90 degress
1	RO	0x0	Reserved
0	RW	0x0	Nal_mode The output of NAL size to base control

**VEPU swreg 75**

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Intramod_16x16
15:0	RW	0x0000	Intermod The intra/inter selection for inter macro block mode favor.

**VEPU swreg 76 reuse**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Pps_init_qp Pps init qp in picture used in h264. Range: 0~51
25:22	RW	0x0	Sliceflt_alpha Offset div2 Range: -6~6
21:18	RW	0x0	Sliceflt_beta Config value = (real value)/2 Signed register Range: -6 ~6
17:13	RW	0x00	Qp_offset_ch Signed register Range: -12~12
12:9	RO	0x0	Reserved
8	RW	0x0	Sw_qpass
7:5	RO	0x0	Reserved
4:1	RW	0x0	Idr_picid IDR pic ID
0	RW	0x0	Constr_intra_pred Constrained intra prediction

**VEPU swreg 77**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Output_strm_st_adr Output stream start address

**VEPU swreg 78**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Output_ctrl_st_adr Output control start address

**VEPU swreg 79**

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Next_luma_st_adr Next picture luminance start address

**VEPU swreg 80**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mv_out_st_adr Mv wr start address

**VEPU swreg 81**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Cabac_table_st_adr H264: Cabac table

**VEPU swreg 82**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	First_roi_tmb (Inside area)
23:16	RW	0x00	First_roi_bmb (Outside area)
15:8	RW	0x00	First_roi_lmb $Qp = qp + roi1\_Delta\_Qp$ (Inside area)
7:0	RW	0x00	First_roi_rmb $Qp = qp - roi1\_Delta\_Qp$ (Outside area)

**VEPU swreg 83**

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Second_roi_rmb (Inside area)
23:16	RW	0x00	Second_roi_bmb (Outside area)
15:8	RW	0x00	Second_roi_lmb $Qp = qp + roi1\_Delta\_Qp$ (Inside area)
7:0	RW	0x00	Second_roi_tmb $Qp = qp - roi1\_Delta\_Qp$ (Outside area)

**VEPU swreg 84**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix1 (Position@ up-left)

**VEPU swreg 85**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix2 (Position @ up)

**VEPU swreg 86**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix3 (Position @up-right)

**VEPU swreg 87**

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix4 (Position @ left)

**VEPU swreg 88**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix5 (Position @GMV )

**VEPU swreg 89**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix6 (Position@right )

**VEPU swreg 90**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix7 (Position@down-left)

**VEPU swreg 91**

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix8 (Position@down )

**VEPU swreg 92**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Stab_gmv_vrtl Signed register Range: -16~16
25:24	RO	0x0	Reserved
23:0	RW	0x000000	Stab_matrix9 (Position@down- right )

**VEPU swreg 93**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Stab_motion_sum Read value = (real value)/8 Range: 0~1089*253*255*53/8

**VEPU swreg 94**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Stab_min_value Range: 0~255*253*253
7:6	RW	0x0	Stab_mod_sel 2'd0: Disabled 2'd1: Stab only 2'd2: Stab+encode

Bit	Attr	Reset Value	Description
5:0	RW	0x00	Stab_hor_gmv Signed register Range: -16~16

**VEPU swreg 95**

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Rgb2yuv_coe2 The 2st conversion coefficient for RGB to YUV
15:0	RW	0x0000	Rgb2yuv_coe1 The 1st conversion coefficient for RGB to YUV

**VEPU swreg 96**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Rgb2yuv_coe5 The 5st conversion coefficient for RGB to YUV
15:0	RW	0x0000	Rgb2yuv_coe3 The 3st conversion coefficient for RGB to YUV

**VEPU swreg 97**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15:0	RW	0x0000	Rgb2yuv_coe6 The 6st conversion coefficient for RGB to YUV

**VEPU swreg 98**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	Reserved
20:16	RW	0x00	Bcmpt_mask_postition Range: 0~31
15:13	RO	0x0	Reserved
12:8	RW	0x00	Gcmpt_mask_postition Range: 0~31
7:5	RO	0x0	Reserved
4:0	RW	0x00	Rcmpt_mask_postition Range: 0~31

**VEPU swreg 99**

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved
30:21	RW	0x000	Mv_1p_ply Differential MV penalty for 1p
20:11	RW	0x000	Mv_1p_4p_ply ME. DMVPenaltyQp
10:1	RW	0x000	Mv_4p_ply 4p of differential MV penalty
0	RW	0x0	Mutimv_en On-off flag for using exceed one mv every mb.

**VEPU swreg 100 reuse**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	H264_init_luma_qp Range: 0~51
25:20	RW	0x00	H264_max_qp Range: 0~51
19:14	RW	0x00	H264_min_qp Range: 0~51
13	RO	0x0	Reserved
12:0	RW	0x0000	H264_chkpt_distance Checkpoint distance for macro block

### **VEPU swreg 101 read**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:12	RO	0x1f522	HW_CONFIG Field0000 Description
11:0	RO	0x780	MAX_VID_WIDTH Field0000 Description

### **VEPU swreg 102**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:20	RW	0x0	Mv_favor_16x16 Value = (real value)/2.
19:11	RW	0x000	Mv_ply_4x4 4x4 Mv Penalty
10:8	RW	0x0	Mvc_view_id MVC view id
7	RW	0x0	Mvc_anchor_pic_flag To specifie picture is one part of anchor access unit
6:4	RW	0x0	Mvc_priority_id MVC priority id
3:1	RW	0x0	Mvc_temporal_id MVC temporal id
0	RW	0x0	Mvc_inter_view_flag MVC inter_view_flag.

### **VEPU swreg 103**

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Reserved
28:20	RW	0x000	Enc_height Lum height (macroblock unit) H264: [6..255] JPEG: [6..511]
19:17	RO	0x0	Reserved
16:8	RW	0x000	Enc_width Lum width (macroblock unit) H264: Range: 9~255 JPEG: Range: 6~511



Bit	Attr	Reset Value	Description
7:6	RW	0x0	Enc_frame_type 0: INTER 1: INTRA(IDR) 2: MVC-INTER
5:4	RW	0x0	Enc_fmt 2: JPEG 3: H264
3:1	RO	0x0	Reserved
0	RW	0x0	Enc_en Encoder enable

**VEPU swreg 104**

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Mb_count_out Mb_count_out
15:0	RW	0x0000	Mb_cnt Macroblock_count

**VEPU swreg 105**

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31	RW	0x0	Swap8_in 1'b0: No swap 1'b1: Swap 8bit
30	RW	0x0	Swap16_in 1'b0: No swap 1'b1: Swap 16bit
29	RW	0x0	Swap32_in 1'b0: No swap 1'b1: Swap 32bit
28	RW	0x0	Swap8_out 1'b0: No swap 1'b1: Swap 8bit
27	RW	0x0	Swap16_out 1'b0: No swap 1'b1: Swap 16bit
26	RW	0x0	Swap32_out 1'b0: No swap 1'b1: Swap 32bit
25	RO	0x0	Reserved
24	RW	0x0	Test_irq Test irq
23:20	RW	0x0	Test_counter Test counter
19	RW	0x0	Coher_test_reg Test register coherency
18	RW	0x0	Coher_test_mem Test memory coherency
17:0	RW	0x00000	Test_len Test data length

**VEPU swreg 106 reuse**

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Pic_para_id H.264 picture parameter id set
23:16	RW	0x00	Intra_pred_mode H.264 intra prediction previous 4x4 mode favor
15:0	RW	0x0000	Frame_num H.264 frame number

**VEPU swreg 107 reuse**

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:20	RW	0x000	Mv_ply_16x8_8x16 Penalty for using 16x8 or 8x16 MV
19:10	RW	0x000	Mv_ply_8x8 Penalty for using 8x8 MV
9:0	RW	0x000	Mv_ply_8x4_4x8 Penalty for using 8x4 or 4x8 MV.

**VEPU swreg 108 reuse**

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Intra_slice_bmp2 Bit0: Slices64 Bit1: Slices65 Bit2: Slices66 ..... Bit31: Slices95

**VEPU swreg 109**

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	Mv_sad_wren The each MB MV and SAD be writed to mv_wr_st_adr enable
23:21	RO	0x0	Reserved
20	RW	0x0	Rocon_write_dis Write reconstructed image disable flag
19:17	RO	0x0	Reserved
16	RW	0x0	Slice_rdyint_en Enable slice ready interrupt
15:13	RO	0x0	Reserved
12	RW	0x1	Clk_gating_en Default clk_gating_en = 1'b1
11	RO	0x0	Reserved
10	RW	0x0	Int_timeout_en Enable interrupt for timeout
9	RW	0x0	Irq_clr Irq clear
8	RW	0x0	Irq_dis Irq disable
7	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	Irq_timeout HW wait timeout flag
5	RW	0x0	Irq_buffer_full Buffer full flag
4	RW	0x0	Irq_bus_error Bus error irq
3	RW	0x0	Fuse_int Fuse irq
2	RW	0x0	Irq_slice_ready Slice ready flag
1	RW	0x0	Irq_frame_rdy One frame encoder success flag
0	RW	0x0	Enc_irq Enc interrupt

**VEPU swreg 110 read**

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:16	RO	0x4831	Prod_id Product ID
15:12	RO	0x1	Major_num Major number
11:4	RO	0x22	Minor_num Minor number
3:0	RO	0x0	Synthesis {ASCII_ID_E,BUILDNUMBER}

**VEPU swreg 120 183**

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	Dmv_ply_table Addr range: 0x01e0~0x02dc Swreg120: DMV 4p/1p penalty table values Swreg121: DMV 4p/1p penalty table values Swreg122: DMV 4p/1p penalty table values Swreg123: DMV 4p/1p penalty table values ..... Swreg183: DMV 4p/1p penalty table values

**13.6.4 VDP121 Registers Summary**

Name	Offset	Size	Reset Value	Description
VDP121_Swreg0	0x00000	W	0x00010100	Axi control
VDP121_Swreg1	0x00004	W	0x00000000	Color coeff register0
VDP121_Swreg2	0x00008	W	0x00000000	Color coeff register1
VDP121_Swreg3	0x0000c	W	0x00000000	Color coeff register2
VDP121_Swreg4	0x00010	W	0x00000000	Scl ctrl register0
VDP121_Swreg5	0x00014	W	0x00000000	Scl ctrl register1
VDP121_Swreg6	0x00018	W	0x00000000	Scl ctrl register2
VDP121_Swreg7	0x0001c	W	0x00000000	Amount of pixels beyond border0.
VDP121_Swreg8	0x00020	W	0x00000000	Amount of pixels beyond border1.
VDP121_Swreg9	0x00024	W	0x00000000	Rmask register

Name	Offset	Size	Reset Value	Description
VDPU_Swreg10	0x00028	W	0x00000000	Gmask register
VDPU_Swreg11	0x0002c	W	0x00000000	Bmask register
VDPU_Swreg12	0x00030	W	0x00000000	PP input picture base address for Y bottom field.
VDPU_Swreg13	0x00034	W	0x00000000	PP input picture base for Ch bottom field.
VDPU_Swreg14	0x00038	W	0x00000000	Coordinate used in macroblock crop.
VDPU_Swreg15	0x0003c	W	0x00000000	Range map register
VDPU_Swreg16	0x00040	W	0x00000000	Total num of padded for RGB
VDPU_Swreg17	0x00044	W	0x00000000	Hw support informan, read only
VDPU_Swreg18	0x00048	W	0x00000000	Base address for reading post-processing input picture luminance.
VDPU_Swreg19	0x0004c	W	0x00000000	Base address for reading post-processing input picture Cb/Ch.
VDPU_Swreg20	0x00050	W	0x00000000	Input cr component address
VDPU_Swreg21	0x00054	W	0x00000000	Base address for writing post-processed picture luminance/RGB.
VDPU_Swreg22	0x00058	W	0x00000000	Base address for writing post-processed picture Ch.
VDPU_Swreg23	0x0005c	W	0x00000000	Display width and PP input size extension register.
VDPU_Swreg24	0x00060	W	0x00000000	Alpha blending base address.
VDPU_Swreg25	0x00064	W	0x00000000	Ablend of pixels scanline
VDPU_Swreg26	0x00068	W	0x00000000	X-coordinate of mask area 1 for horizontal start pixel.
VDPU_Swreg27	0x0006c	W	0x00000000	Y-coordinate of mask area 1 for Horizontal start pixel.
VDPU_Swreg28	0x00070	W	0x00000000	X-coordinate of mask area 2 for Horizontal start pixel.
VDPU_Swreg29	0x00074	W	0x00000000	Y-coordinate of mask area 2 for Horizontal start pixel
VDPU_Swreg30	0x00078	W	0x00000000	Register for deinterlace ctrl
VDPU_Swreg31	0x0007c	W	0x00000000	Contrast adjust threshold
VDPU_Swreg32	0x00080	W	0x00000000	Contrast adjust offset
VDPU_Swreg33	0x00084	W	0xfc874780	Synthesis configuration register post-processor (read only).
VDPU_Swreg34	0x00088	W	0x00000000	PP input pic size register.
VDPU_Swreg35	0x0008c	W	0x00000000	PP output pic size register
VDPU_Swreg36	0x00090	W	0x00000000	The dither mode for RGB
VDPU_Swreg37	0x00094	W	0x00000000	PP input/output data format
VDPU_Swreg38	0x00098	W	0x00000000	PP input/output data format.
VDPU_Swreg39	0x0009c	W	0x00000000	The display width ctrl
VDPU_Swreg40	0x000a0	W	0x00000000	Pp int register
VDPU_Swreg41	0x000a4	W	0x00000008	Enable ctrl flag

Name	Offset	Size	Reset Value	Description
VDPU_Swreg50	0x000c8	W	0x00000000	video decoder ctrl register
VDPU_Swreg51	0x000cc	W	0x00000000	The stream length
VDPU_Swreg52	0x000d0	W	0x00000000	Error concealment case related.
VDPU_Swreg53	0x000d4	W	0x00000000	Decoder format
VDPU_Swreg54	0x000d8	W	0x00000000	Endian for input/output data
VDPU_Swreg55	0x000dc	W	0x00000000	Decoder int register
VDPU_Swreg56	0x000e0	W	0x00200101	Axi ctrl for decoder
VDPU_Swreg57	0x000e4	W	0x00000010	Enable flag for decoder
VDPU_Swreg58	0x000e8	W	0x00000000	Soft reset register
VDPU_Swreg59	0x000ec	W	0x00000000	H264, MPEG4, VC1, VP6 Prediction filter tap.
VDPU_Swreg60	0x000f0	W	0x00000000	Additional chrominance address
VDPU_Swreg61	0x000f4	W	0x00000000	Standard dependent tables start address.
VDPU_Swreg62	0x000f8	W	0x00000000	Direct mode motion vector write/read start address.
VDPU_Swreg63	0x000fc	W	0x00000000	Write decoder output picture or field start address.
VDPU_Swreg64	0x00100	W	0x00000000	Rlc or vlc mode input data start addr.
VDPU_Swreg65	0x00104	W	0x00000000	Refbufferd related
VDPU_Swreg66	0x00108	W	0x67312688	ID register
VDPU_Swreg67	0x0010c	W	0xc1520000	Synthesis configuration register decoder 1(read only).
VDPU_Swreg68	0x00110	W	0x00000000	Sum of partitions(read only)
VDPU_Swreg69	0x00114	W	0x00000000	Sum information (read only)
VDPU_Swreg70	0x00118	W	0x00000000	Sum of the decoded motion vector y-components(read only).
VDPU_Swreg71	0x0011c	W	0xfb356780	Information for read only register.
VDPU_Swreg72	0x00120	W	0x00000000	Debug0
VDPU_Swreg73	0x00124	W	0x00000000	Debug registers
VDPU_Swreg74	0x00128	W	0x00000000	MV address for h264.
VDPU_Swreg75	0x0012c	W	0x00000000	H.264 Intra prediction 4x4 mode start address.
VDPU_Swreg76	0x00130	W	0x00000000	The number of reference pic0~1
VDPU_Swreg77	0x00134	W	0x00000000	The number of reference pic2~3
VDPU_Swreg78	0x00138	W	0x00000000	The number of reference pic4~5
VDPU_Swreg79	0x0013c	W	0x00000000	The number of reference pic6~7
VDPU_Swreg80	0x00140	W	0x00000000	The number of reference pic8~9
VDPU_Swreg81	0x00144	W	0x00000000	The number of reference pic10~11
VDPU_Swreg82	0x00148	W	0x00000000	The number of reference pic12~13
VDPU_Swreg83	0x0014c	W	0x00000000	The number of reference pic14~15
VDPU_Swreg84	0x00150	W	0x00000000	reference frame0 address for h264.
VDPU_Swreg85	0x00154	W	0x00000000	reference frame1 address for h264.
VDPU_Swreg86	0x00158	W	0x00000000	reference frame2 address for h264.

Name	Offset	Size	Reset Value	Description
VDPU_Swreg87	0x0015c	W	0x00000000	reference frame3 address for h264.
VDPU_Swreg88	0x00160	W	0x00000000	reference frame4 address for h264.
VDPU_Swreg89	0x00164	W	0x00000000	reference frame5 address for h264.
VDPU_Swreg90	0x00168	W	0x00000000	reference frame6 address for h264.
VDPU_Swreg91	0x0016c	W	0x00000000	reference frame7 address for h264.
VDPU_Swreg92	0x00170	W	0x00000000	reference frame8 address for h264.
VDPU_Swreg93	0x00174	W	0x00000000	reference frame9 address for h264.
VDPU_Swreg94	0x00178	W	0x00000000	reference frame10 address for h264.
VDPU_Swreg95	0x0017c	W	0x00000000	reference frame11 address for h264.
VDPU_Swreg96	0x00180	W	0x00000000	reference frame12 address for h264.
VDPU_Swreg97	0x00184	W	0x00000000	reference frame13 address for h264.
VDPU_Swreg98	0x00188	W	0x00000000	reference frame14 address for h264.
VDPU_Swreg99	0x0018c	W	0x00000000	reference frame15 address for h264.
VDPU_Swreg100	0x00190	W	0x00000000	Initial reference picture list related0.
VDPU_Swreg101	0x00194	W	0x00000000	Initial reference picture list related1.
VDPU_Swreg102	0x00198	W	0x00000000	Initial reference picture list related2.
VDPU_Swreg103	0x0019c	W	0x00000000	Initial reference picture list related3.
VDPU_Swreg104	0x001a0	W	0x00000000	Initial reference picture list related4.
VDPU_Swreg105	0x001a4	W	0x00000000	Initial reference picture list related5.
VDPU_Swreg106	0x001a8	W	0x00000000	Initial reference picture list related6.
VDPU_Swreg107	0x001ac	W	0x00000000	Long term flag for reference picture index.
VDPU_Swreg108	0x001b0	W	0x00000000	Valid flag for reference picture index.
VDPU_Swreg109	0x001b4	W	0x00000000	The stream start word for decoder.
VDPU_Swreg110	0x001b8	W	0x00000000	H264 pic mb size
VDPU_Swreg111	0x001bc	W	0x00000000	H264 ctrl related
VDPU_Swreg112	0x001c0	W	0x00000000	Current frame related
VDPU_Swreg113	0x001c4	W	0x00000000	Reference picture related
VDPU_Swreg114	0x001c8	W	0x00000000	Maximum reference
VDPU_Swreg115	0x001cc	W	0x00000000	Enable flag
VDPU_Swreg120	0x001e0	W	0x00000000	Multi format reuse register0
VDPU_Swreg121	0x001e4	W	0x00000000	Multi format reuse register1
VDPU_Swreg122	0x001e8	W	0x00000000	Multi format reuse register2
VDPU_Swreg123	0x001ec	W	0x00000000	Multi format reuse register3
VDPU_Swreg124	0x001f0	W	0x00000000	Multi format reuse register4
VDPU_Swreg125	0x001f4	W	0x00000000	Multi format reuse register5
VDPU_Swreg126	0x001f8	W	0x00000000	Multi format reuse register6
VDPU_Swreg127	0x001fc	W	0x00000000	Multi format reuse register7
VDPU_Swreg128	0x00200	W	0x00000000	Multi format reuse register8
VDPU_Swreg129	0x00204	W	0x00000000	Multi format reuse register9
VDPU_Swreg130	0x00208	W	0x00000000	Multi format reuse register10
VDPU_Swreg131	0x0020c	W	0x00000000	Multi format reuse register11
VDPU_Swreg132	0x00210	W	0x00000000	Multi format reuse register12

Name	Offset	Size	Reset Value	Description
VDPU_Swreg133	0x00214	W	0x00000000	Multi format reuse register13
VDPU_Swreg134	0x00218	W	0x00000000	Multi format reuse register14
VDPU_Swreg135	0x0021c	W	0x00000000	Multi format reuse register15
VDPU_Swreg136	0x00220	W	0x00000000	Multi format reuse register16
VDPU_Swreg137	0x00224	W	0x00000000	Multi format reuse register17
VDPU_Swreg138	0x00228	W	0x00000000	Multi format reuse register18
VDPU_Swreg139	0x0022c	W	0x00000000	Multi format reuse register19
VDPU_Swreg140	0x00230	W	0x00000000	Multi format reuse register20
VDPU_Swreg141	0x00234	W	0x00000000	Multi format reuse register21
VDPU_Swreg142	0x00238	W	0x00000000	Multi format reuse register22
VDPU_Swreg143	0x0023c	W	0x00000000	Multi format reuse register23
VDPU_Swreg144	0x00240	W	0x00000000	Multi format reuse register24
VDPU_Swreg145	0x00244	W	0x00000000	Multi format reuse register25
VDPU_Swreg146	0x00248	W	0x00000000	Multi format reuse register26
VDPU_Swreg147	0x0024c	W	0x00000000	Multi format reuse register27
VDPU_Swreg148	0x00250	W	0x00000000	Multi format reuse register28
VDPU_Swreg149	0x00254	W	0x00000000	Multi format reuse register29
VDPU_Swreg150	0x00258	W	0x00000000	Multi format reuse register30
VDPU_Swreg151	0x0025c	W	0x00000000	Multi format reuse register31
VDPU_Swreg152	0x00260	W	0x00000000	Multi format reuse register32
VDPU_Swreg153	0x00264	W	0x00000000	Multi format reuse register33
VDPU_Swreg154	0x00268	W	0x00000000	Multi format reuse register34
VDPU_Swreg155	0x0026c	W	0x00000000	Multi format reuse register35
VDPU_Swreg156	0x00270	W	0x00000000	Multi format reuse register36
VDPU_Swreg157	0x00274	W	0x00000000	Multi format reuse register37
VDPU_Swreg158	0x00278	W	0x00000000	Multi format reuse register38
VDPU_Swreg164_perf_latency_ctrl0	0x00290	W	0x00000000	Axi performance latency module ctrl register0.
VDPU_Swreg165_perf_latency_ctrl1	0x00294	W	0x00000000	Axi performance latency module ctrl register1.
VDPU_Swreg166_perf_rd_max_latency_num0	0x00298	W	0x00000000	Read max latency number
VDPU_Swreg167_perf_rd_latency_sample_num	0x0029c	W	0x00000000	The number of bigger than configed threshold value.
VDPU_Swreg168_perf_rd_latency_acc_num	0x002a0	W	0x00000000	Total sample number
VDPU_Swreg169_perf_rd_axi_total_byte	0x002a4	W	0x00000000	Perf_rd_axi_total_byte

Name	Offset	Size	Reset Value	Description
VDPU_Swreg170_perf_wr_axi_total_byte	0x002a8	W	0x00000000	Perf_wr_axi_total_byte
VDPU_Swreg171_perf_working_cnt	0x002ac	W	0x00000000	Perf_working_cnt

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.5 VDPU121 Detail Registers Description

#### VDPU\_Swreg0

Address: Operational Base + offset (0x00000)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x01	Sw_axi_id_wr If you config 0, will modify as 1 by hw.
15:8	RW	0x01	Sw_axi_id_rd If you config 0, will modify as 1 by hw.
7:6	RO	0x0	reserved
5	RW	0x0	Sw_scmd_off On-off for AXI Single Command Multiple Data. 1'b0: On 1'b1: Off
4:0	RW	0x00	Sw_max_burst_len The max burst length can be used by axi bus. Range: 1-16

#### VDPU\_Swreg1

Address: Operational Base + offset (0x00004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	Sw_coe_2st Used for red color components calculate, used together with cr pix.
19:10	RW	0x000	Sw_coe_1st_1 Used for all color components calculate, used together with y pix.
9:0	RW	0x000	Sw_coe_1st_0 Used for all color components calculate, used together with y pix.

#### VDPU\_Swreg2

Address: Operational Base + offset (0x00008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved



Bit	Attr	Reset Value	Description
29:20	RW	0x000	Sw_coe_5st Used for blue components calculate, used together with cb pix.
19:10	RW	0x000	Sw_coe_4st Used for green color components calculate, used together with cb pix.
9:0	RW	0x000	Sw_coe_3st Used for green color components calculate, used together with cr pix.

**VDPU\_Swreg3**

Address: Operational Base + offset (0x0000c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Sw_coe_6st Used for burightness adjust, sed together with y pix.

**VDPU\_Swreg4**

Address: Operational Base + offset (0x00010)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:22	RW	0x0	Sw_scl_mode_vrt 2'd0: No scl 2'd1: Up scl 2'd2: Down scl
21:20	RW	0x0	Sw_scl_mode_hrz To select scaling mode for Horizontal. 2'd0: No scl 2'd1: Up scl 2'd2: Down scl
19:18	RO	0x0	reserved
17:0	RW	0x00000	Sw_scl_fct_w Scaling factor of width. Value = (output_width-1)/(input_width-1).

**VDPU\_Swreg5**

Address: Operational Base + offset (0x00014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:0	RW	0x00000	Sw_scl_fct_h Scaling factor of height. Value = (output_width-1)/(input_width-1).

**VDPU\_Swreg6**

Address: Operational Base + offset (0x00018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_scl_fct_h_inv Scaling factor of height and cv. Value =(inputw-1) / (outputw-1).
15:0	RW	0x0000	Sw_scl_fct_w_inv Scaling factor of width and ch. Value =(inputw-1) / (outputw-1).

**VDPU\_Swreg7**

Address: Operational Base + offset (0x0001c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	Sw_pixnum_down_byd The Amount of vertical pixels beyond the down border. Range: 0~dst_height.
15:11	RO	0x0	reserved
10:0	RW	0x000	Sw_pixnum_up_byd The Amount of vertical pixels beyond the up border. Range: 0~dst_height.

**VDPU\_Swreg8**

Address: Operational Base + offset (0x00020)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	Sw_pixnum_right_byd The Amount of vertical pixels beyond the right border. Range: 0~dst_width.
15:11	RO	0x0	reserved
10:0	RW	0x000	Sw_pixnum_left_byd The Amount of vertical pixels beyond the left border. Range: 0~dst_width.

**VDPU\_Swreg9**

Address: Operational Base + offset (0x00024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_mask_r Color R/(alpha channel) component 's bit mask.

**VDPU\_Swreg10**

Address: Operational Base + offset (0x00028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_mask_g Color G/(alpha channel) component 's bit mask.

**VDPU\_Swreg11**

Address: Operational Base + offset (0x0002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_mask_b Color B/(alpha channel) component 's bit mask.

**VDPU\_Swreg12**

Address: Operational Base + offset (0x00030)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_botfld_y_st_adr Input bottom field pp start address for y component.
1:0	RO	0x0	reserved

**VDPU\_Swreg13**

Address: Operational Base + offset (0x00034)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_botfld_c_st_adr Input bottom field pp start address for c component.
1:0	RO	0x0	reserved

**VDPU\_Swreg14**

Address: Operational Base + offset (0x00038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	Sw_mrmb_8pix_flag 829PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the unrotated input picture is used for PP input.
28	RW	0x0	Sw_mdmb_8pix_flag The most down unrotated MB of input picture just 8 rows pix data.
27	RO	0x0	reserved
26:24	RW	0x0	Sw_mbcrop_crdty_ext In order to support jpeg to extend coordinate y bits.
23:16	RW	0x00	Sw_mbcrop_crdty Coordinate y used in macroblock crop.
15:12	RO	0x0	reserved
11:9	RW	0x0	Sw_mbcrop_crdtx_ext In order to support jpeg to extend bits.
8:0	RW	0x000	Sw_mbcrop_crdtx Coordinate x used in macroblock crop.

**VDPU\_Swreg15**

Address: Operational Base + offset (0x0003c)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	Sw_rangemap_coef_c The value of chrominance component range map. VC- 1: C range map value + 9.
7:6	RO	0x0	reserved
5	RW	0x0	Sw_yuv_conv_range To declaration the range of YCbCr when RGB conversion. Y: 1'b0: 16~235 1'b1: 0~255 C: 1'b0: 16~240 1'b1: 0~255
4:0	RW	0x00	Sw_rangemap_y The value of Y component range map. VC- 1: Y range map value + 9.

**VDPU\_Swreg16**

Address: Operational Base + offset (0x00040)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	Sw_padd_b The total num of padded in front of B componet.
15:13	RO	0x0	reserved
12:8	RW	0x00	Sw_padd_g The total num of padded in front of G componet.
7:5	RO	0x0	reserved
4:0	RW	0x00	Sw_padd_r The total num of padded in front of R componet.

**VDPU\_Swreg17**

Address: Operational Base + offset (0x00044)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	Pp_deinterl_en On-off for pp deinterlance. 1'b0: Off 1'b1: On
29	RO	0x0	Pp_abled_en On-off for pp Alpha Blending. 1'b0: Off 1'b1: On

Bit	Attr	Reset Value	Description
28	RO	0x0	Pp_work_en Pp work allow flag. 1'b0: Off 1'b1: On
27:4	RO	0x0	reserved
3	RO	0x0	Pp_outw_1920_en On-off for pp output width up to 1920, 1st priority used.
2	RO	0x0	Pp_outw_1280_en On-off for pp output width up to 1280, 2st priority used.
1	RO	0x0	Pp_outw_720_en On-off for pp output width up to 720, 3st priority used.
0	RO	0x0	Pp_outw_352_en On-off for pp output width up to 352, 4st priority used.

**VDPU\_Swreg18**

Address: Operational Base + offset (0x00048)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_y_in_st_adr Input y component start address. The start address of topfield of the picture when data come from fields, external mode support only.
1:0	RO	0x0	reserved

**VDPU\_Swreg19**

Address: Operational Base + offset (0x0004c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_cb_in_st_adr Input cb component start address. The start address of topfield of the picture when data come from fields, external mode support only.
1:0	RO	0x0	reserved

**VDPU\_Swreg20**

Address: Operational Base + offset (0x00050)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_cr_in_st_adr Input cr component start address. The start address of topfield of the picture when data come from fields, external mode support only.
1:0	RO	0x0	reserved

**VDPU\_Swreg21**

Address: Operational Base + offset (0x00054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_y_out_st_adr Output y component start address, also the start address of YUYV and RGB.

**VDPU\_Swreg22**

Address: Operational Base + offset (0x00058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_c_out_st_adr Output chrominance component start address. Format is uvuvuv....

**VDPU\_Swreg23**

Address: Operational Base + offset (0x0005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_abled_st_adr_1st 1st alpha blending start address. 1. Valid when mask1 is used in alpha blending mode. 2. Format of data the same as in PP input. 3. Amount of data is related to mask 1 size or ablend1_scanline informed with mask 1 size or with ablend1_scanline if ablend when crop flag valid.

**VDPU\_Swreg24**

Address: Operational Base + offset (0x00060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_abled_st_adr_2st 2st alpha blending start address. 1. Valid when mask2 is used in alpha blending mode. 2. Format of data the same as in PP input. 3. Amount of data is related to mask 2 size or ablend1_scanline informed with mask 1 size or with ablend1_scanline if ablend when crop flag valid.

**VDPU\_Swreg25**

Address: Operational Base + offset (0x00064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	Sw_scanl_abld2 Ablend 2 of pixels scanline. Corresponding function should be enabled.
15:13	RO	0x0	reserved
12:0	RW	0x0000	Sw_scanl_abld1 Ablend 1 of pixels scanline. Corresponding function should be enabled.

**VDPU\_Swreg26**

Address: Operational Base + offset (0x00068)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:12	RW	0x000	Sw_end_coordx_ma1 The end x-coordinate of mask area 1 of horizontal start pixel. Range: Sw_st_coordx_ma1~dst width.
11	RO	0x0	reserved
10:0	RW	0x000	Sw_st_coordx_ma1 The start x-coordinate of mask area 1 of horizontal start pixel.

**VDPU\_Swreg27**

Address: Operational Base + offset (0x0006c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:12	RW	0x000	Sw_end_coordy_ma1 The start y-coordinate of mask area 1 of Vertical start pixel. Range: Sw_st_coordy_ma1~dst width.
11	RO	0x0	reserved
10:0	RW	0x000	Sw_st_coordy_ma1 The start y-coordinate of mask area 1 of Vertical start pixel.

**VDPU\_Swreg28**

Address: Operational Base + offset (0x00070)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:11	RW	0x000	Sw_end_coordx_ma2 The end x-coordinate of mask area 2 of Horizontal start pixel. Range: Sw_st_coordx_ma2~dst width.
10:0	RW	0x000	Sw_st_coordx_ma2 The start x-coordinate of mask area 2 of Horizontal start pixel.

**VDPU\_Swreg29**

Address: Operational Base + offset (0x00074)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:11	RW	0x000	Sw_end_coordy_ma2 The start y-coordinate of mask area 2 of Vertical start pixel. Range: Sw_st_coordy_ma2~dst width.
10:0	RW	0x000	Sw_st_coordy_ma2 The start y-coordinate of mask area 2 of Vertical start pixel.

**VDPU\_Swreg30**

Address: Operational Base + offset (0x00078)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	Sw_deinterl_edge Edge detect value used for deinterlacing.
15:14	RO	0x0	reserved
13:0	RW	0x0000	Sw_deinterl_thr The threshold value of deinterlace.

**VDPU\_Swreg31**

Address: Operational Base + offset (0x0007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	Sw_cont_thr1 The threshold value 1 for contrast adjust.
7:0	RW	0x00	Sw_cont_thr0 The threshold value 0 for contrast adjust.

**VDPU\_Swreg32**

Address: Operational Base + offset (0x00080)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	Sw_cont_offset1 The offset value 1 for contrast adjust.
15:10	RO	0x0	reserved
9:0	RW	0x000	Sw_cont_offset0 The offset value 0 for contrast adjust.

**VDPU\_Swreg33**

Address: Operational Base + offset (0x00084)

Bit	Attr	Reset Value	Description
31	RO	0x1	Abld_crop_flag 1'b0: Unsupport crop, the exact image of the area being alpha blended should exist in the external memory. 1'b1: Supprot crop, one picture in external memory which come from blended area can be cropped.
30	RO	0x1	Accut_out_exist_flag Pixel Accurate PP output mode exists flag. PIP: 1'b0: Use 8 pixels (width) or 2 pixels (height) steps to adjust Scaling and masks. 1'b1: Use 1 pixel for RGB and 2 pixels for subsampled chroma formats to adjust Scaling and masks.



Bit	Attr	Reset Value	Description
29	RO	0x1	Tile_exist_flag The output of yuv422 tiled exist flag. 1'b0: No exist 1'b1: Exist
28	RO	0x1	Dither_exist_flag Dithering exists flag. 1'b0: No exist 1'b1: Exist
27:26	RO	0x3	Scl_perf_sel Scaling performance sel. 2'd0: Without scaling. 2'd1: Low performance scaling. 2'd2: High performance scaling. 2'd3: High and fast performance scaling.
25	RO	0x0	Deinterl_exist_flag Deinterlacing exists flag. 1'b0: No exist 1'b1: Exist
24	RO	0x0	Abld_exist_flag Alpha blending exists flag. 1'b0: No exist 1'b1: Exist
23	RO	0x1	Pp_in_buf_sel PP input buffering select. 1'b0: Output buffering is 1 MB. 1'b1: Output buffering is 4 MB.
22:19	RO	0x0	reserved
18	RO	0x1	Pp_endian_mode PP output endian mode select. 1'b0: Endian mode supported except RGB. 1'b1: Endian mode supported for all format.
17	RO	0x1	Pp_out_buf_sel PP output buffering select. 1'b0: Output buffering is 1 unit. 1'b1: Output buffering is 4 unit.
16	RO	0x1	Ppd_exist_flag 1'b0: No exist 1'b1: Exist
15:14	RO	0x1	Pp_tile_in_mode PD input tiled mode. 2'd0: Unsupport. 2'd1: 8x4 tile be used.
13:11	RO	0x0	reserved
10:0	RO	0x780	Ppd_max_outw The max pixels width allow for pp output.

**VDPU\_Swreg34**

Address: Operational Base + offset (0x00088)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Sw_pp_inh_ext PP input extended height. In order to support jpeg.
28:21	RW	0x00	Sw_pp_inh The picture height of PP input with in macro blocks which can be cropped from a bigger picture when in the condtion of external mode.
20:12	RW	0x000	Sw_org_inw_ext The orginal width of pp input pic in MBS.
11:9	RW	0x0	Sw_pp_inw_ext PP input extended width. In order to support jpeg.
8:0	RW	0x000	Sw_pp_inw The picture width of PP input with in macro blocks which can be cropped from a bigger picture when in the condtion of external mode.

**VDPU\_Swreg35**

Address: Operational Base + offset (0x0008c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_pp_outh_ext The extension height of pp output.
26:16	RW	0x000	Sw_pp_outh (output width = 2*n (n=1,2,.....)    output width =(configured Pixel Accurate PP output configuration)*n ) && (pp output width < 1920    pp output width< 3*(sw_pp_inh-8)).
15:12	RO	0x0	reserved
11	RW	0x0	Sw_pp_outw_ext The extension width of pp output.
10:0	RW	0x000	Sw_pp_outw The pp output width. (output width = 8*n (n=1,2,.....)    output width =(configured Pixel Accurate PP output configuration)*n ) && (pp output width < 1920    pp output width< 3*(sw_pp_inw-8)).

**VDPU\_Swreg36**

Address: Operational Base + offset (0x00090)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	Sw_dither_mode_b The dither mode for B-component. 2'd0: No use dithering. 2'd1: 4-bits dither matrix be used. 2'd2: 5-bits dither matrix be used. 2'd3: 6-bits dither matrix be used.
3:2	RW	0x0	Sw_dither_mode_g The dither mode for G-component. 2'd0: No use dithering. 2'd1: 4-bits dither matrix be used. 2'd2: 5-bits dither matrix be used. 2'd3: 6-bits dither matrix be used.
1:0	RW	0x0	Sw_dither_mode_r The dither mode for R-component. 2'd0: No use dithering. 2'd1: 4-bits dither matrix be used. 2'd2: 5-bits dither matrix be used. 2'd3: 6-bits dither matrix be used.

**VDPU\_Swreg37**

Address: Operational Base + offset (0x00094)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:24	RW	0x0	Sw_pp_in_data_strc The data structure of pp input picture. 3'd0: Top field. 3'd1: Bottom field. 3'd2: Interlaced field. 3'd3: Interlaced frame. 3'd4: Ripped top field. 3'd5: Ripped bottom field. If value=0/1/2, then should read every line from the base address, if value=3/4/5, then should read every second line from the base address.
23:20	RO	0x0	reserved
19	RW	0x0	Sw_pp_out_crbf_en Output yuv422 or yuv420, cr before cb. 1'b0: Y0CbY0Cr / CbY0CrY0. 1'b1: Y0CrY0Cb / CrY0CbY0.

Bit	Attr	Reset Value	Description
18	RW	0x0	Sw_pp_in_crbf_en In yuv422 or yuv420, cr before cb. Yuv422: 1'b0: Y0CbY0Cr / CbY0CrY0. 1'b1: Y0CrY0Cb / CrY0CbY0. Yuv420 semiplanar chrominance: 1'b0: CbCrCbCr 1'b1: CrCbCrCb
17	RW	0x0	Sw_pp_out_yuv_order The output yuv order. 1'b0: Y0CbY0Cr / Y0CrY0Cb. 1'b1: CbY0CrY0 / CrY0CbY0.
16	RW	0x0	Sw_pp_in_yuv_order The input yuv order. 1'b0: Y0CbY0Cr / Y0CrY0Cb. 1'b1: CbY0CrY0 / CrY0CbY0.
15:12	RO	0x0	reserved
11	RW	0x0	Sw_pp_out_wordsp The 32bit data swap for pp output data. It will be used in 64 bit environment. 1'b0: No swapping. 1'b1: Swapping high and low 32bit data.
10	RW	0x0	Sw_pp_out_hfwordsp The half word swap inside of word. 1'b0: No swap 1'b1: Swap Also be used as change pixel orders for 16 bit RGB, support all output format require pp_endian_mode=1.
9	RW	0x0	Sw_pp_abld1_in_wordsp The 32bit data swap for the input 32bit data swap of Alpha blend. For Alpha blend source 1. 1'b0: No swapping. 1'b1: Swapping high and low 32bit data.
8	RW	0x0	Sw_pp_in_wordsp The 32bit data swap for pp input data. It will be used in 64 bit environment. 1'b0: No swapping. 1'b1: Swapping high and low 32bit data.
7:5	RO	0x0	reserved
4	RW	0x0	Sw_rgb_pix_bits Rga bits used sel. 1'b0: Every word have only one rga pixel. 1'b1: Every word have two rga pixel.

Bit	Attr	Reset Value	Description
3	RW	0x0	Sw_pp_out_endian The endian mode of pp output. For all yuv output endian mode or any data when pp_endian_mode=1. 1'b0: Big endian 1'b1: Little endian If pp_endian_mode=0: 16 bit RGB: This bit used as pixel swapping bit. 32 bit RGB: No used.
2	RW	0x0	Sw_pp_abld2_in_endian The endian select for input data of Alpha blend source 2. 1'b0: Same with sw_pp_in_endian. 1'b1: Same with sw_pp_abld1_in_endian. 1'b0: Use PP in endian/swap definitions (sw_pp_in_endian, sw_pp_in_swap). 1'b1: Use Ablend source 1 endian/swap definitions.
1	RW	0x0	Sw_pp_abld1_in_endian The endian mode of input data for Alpha blend source 1 1'b0: Big endian (0-1-2-3). 1'b1: Little endian (3-2-1-0).
0	RW	0x0	Sw_pp_in_endian The endian mode of pp input picture when PP in standalone. This bit will no to be used when PP is running pipelined with the decoder. 1'b0: Big endian (0-1-2-3). 1'b1: Little endian (3-2-1-0).

**VDPU\_Swreg38**

Address: Operational Base + offset (0x00098)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:20	RW	0x0	Sw_pp_in_tilmod The tiled mode of pp input data. Only support yuv420 input data,can be as pipeline or external mode. 2'd0: Tiled mode not be activated. 2'd1: 8x4 sized tiles be used. 2'd2,2'd3: reserved.
19	RO	0x0	reserved
18:16	RW	0x0	Sw_pp_in_fmt_ecp Escape PP in format Be activated when sw_pp_in_fmt = 3'b111. 3'd0: YCbCr 4:4:4. 3'd1: YCbCr 4:1:1.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:11	RW	0x0	Sw_pp_out_fmt 3'd0: RGB 3'd1: YCbCr 4:2:0, Planar (Not supported). 3'd2: YCbCr 4:2:2, Planar (Not supported). 3'd3: YUYV 4:2:2, Interleaved. 3'd4: YCbCr 4:4:4, Planar (Not supported). 3'd5: YCh 4:2:0, Chrominance interleaved. 3'd6: YCh 4:2:2, (Not supported). 3'd7: YCh 4:4:4 (Not supported).
10:8	RW	0x0	Sw_pp_in_fmt The input format of pp input data. 3'd0: YUYV 4:2:2, Interleaved and it only supported in external mode. 3'd1: YCbCr 4:2:0, The format of Semi-planar in linear raster-scan. 3'd2: YCbCr 4:2:0, Planar and it only supported in external mode. 3'd3: YCbCr 4:0:0, It only supported in pipelined mode. 3'd4: YCbCr 4:2:2, Semi-planar and it only supported only in pipelined mode. 3'd5: YCbCr 4:2:0, Semi-planar in tiled format and it only supported in external mode. 3'd6: YCbCr 4:4:0, Semi-planar and it only supported for jpeg in pipelined mode. 3'd7: Same as sw_pp_in_fmt_ecp.
7:3	RO	0x0	reserved
2:0	RW	0x0	Sw_rot_mode Rotation mode 3'd0: Rotation disabled. 3'd1: Rotate + 90. 3'd2: Rotate - 90. 3'd3: Horizontal flip (mirror). 3'd4: Vertical flip. 3'd5: Rotate 180.

**VDPU\_Swreg39**

Address: Operational Base + offset (0x0009c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	Sw_display_w The display width Max support 1920.

**VDPU\_Swreg40**

Address: Operational Base + offset (0x000a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Sw_pp_bus_sts The Interrupt status bit for tell sw bus have some error.
2	RW	0x0	Sw_pp_rdy_sts The Interrupt status bit for tell sw processed a picture.
1	RW	0x0	Sw_pp_irq_dis The pp finish interrupt request diable flag. 1'b1: Use polling to see the interrupt. 1'b0: Use sw_pp_irq.
0	RW	0x0	Sw_pp_irq The pp finish interrupt request. After sw query this interrupt,shoud write 0 to reset. This bit will no used in pipeline mode.

**VDPU\_Swreg41**

Address: Operational Base + offset (0x000a4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	Sw_pp_ahb_hlock_en The enable flag for AHB master HLOCK. The service is locked to pp as long as it needs the bus.
27	RW	0x0	Sw_rightwd_cross_en The enable flag for Right side overcross. 1'b0: Disable 1'b1: Enable
26	RW	0x0	Sw_leftsd_cross_en The enable flag for Left side overcross. 1'b0: Disable 1'b1: Enable
25	RW	0x0	Sw_downwd_cross_en The enable flag for Downward overcross. 1'b0: Disable 1'b1: Enable
24	RW	0x0	Sw_upwd_cross_en The enable flag for Upward overcross. 1'b0: Disable 1'b1: Enable
23	RW	0x0	Sw_mask2_abld_en The enable flag for Mask 2 alpha blending. Alpha blending for the output picture, only be supported when data format is RGB/YUYV422. Alpha blending read data from alpha blend 2 base address.

Bit	Attr	Reset Value	Description
22	RW	0x0	Sw_mask1_abld_en The enable flag for Mask 1 alpha blending. Alpha blending for the output picture, only be supported when data format is RGB/YUYV422. Alpha blending read data from alpha blend 1 base address.
21	RW	0x0	Sw_mask2_en The enable flag for mask 2. 1'b0: Disable 1'b1: Enable
20	RW	0x0	Sw_mask1_en The enable flag for mask 1. 1'b0: Disable 1'b1: Enable
19:17	RO	0x0	reserved
16	RW	0x0	Sw_pp_discd_en The enable flag for PP data discard. The burst length will be fix after sw_pp_discd_en=1, and extra read data will auto be discarded by HW.
15:12	RO	0x0	reserved
11	RW	0x0	Sw_pp_out_tiled_en The enable flag for pp output tiled mode. Only used in YCbYCr format. Tile size: 4x4 pixels.
10	RW	0x0	Sw_pp_fdscl_en The enable flag for fast downscaling. 1'b0: Disable 1'b1: Rnabled. it will inprove the performance but will decrease the quality of the pic.
9	RW	0x0	Sw_rangemap_c_en The enable flag for C component Range map.
8	RW	0x0	Sw_rangemap_y_en The enable flag for Y component Range map. VC1: Used as range expansion enable.
7:5	RO	0x0	reserved
4	RW	0x0	Sw_pp_pipl_en Pp pipeline width Decoder enable. 1'b0: Disable, external mode. 1'b1: Enable, pipeline mode, Post-processing pipeline with decoder.



Bit	Attr	Reset Value	Description
3	RW	0x1	Sw_pp_clkgate_en Pp auto clock gating: Default is 1 1'b0: Don't auto gating. 1'b1: Audo gating. PP dynamic clock gating enable: 1'b1: Clock is gated from PP structures that are not used. 1'b0: Clock is running for all PP structures. [Note]: Clock gating value can be changed only when PP is not enabled.
2	RW	0x0	Sw_deint_en Deinterlace enable flag. The input data should be interlaced format.
1	RW	0x0	Sw_deint_bld_en On-off Blend for deinterlacing.
0	RW	0x0	Sw_pp_dec_st Post-processing start flag. After config other register, write 1 to start post-processing operation, and hw will reset to 0 after it decoded a picture, should be under External mode.

**VDPUs\_Swreg50**

Address: Operational Base + offset (0x000c8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	Sw_refbuf_pid The pic id for reference buffer. The used reference picture ID for reference buffer usage.
24:13	RW	0x000	Sw_refbuf_thrd Reference buffer threshold value. Used shut down buffer.
12	RW	0x0	Sw_dec_tiled_lsb The enable for lsb tiled mode. 1'b0: Tiled mode disable. 1'b1: Tiled mode enabled for 8x4 tile size.
11	RW	0x0	Sw_adv_pref_dis Disable for Advanced PREFETCH mode.
10	RW	0x0	Sw_dec_ascmd0_dis The disable for AXI Single Command Multiple Data0.
9	RW	0x0	Sw_skip_sel AVS format: 1'b0: Skip mbs use special MB type. 1'b1: Avs skip mbs have the same skip run syntax element as h264.

Bit	Attr	Reset Value	Description
8	RW	0x0	Sw_dblkflt_dis The disable for current pic deblock filtering. 1'b0: Disable 1'b1: Enable
7	RW	0x0	Sw_dec_fixed_quant H.264: This bit is for the enable of multi view coding. Other format(VC1): 1'b0: It can be different inside pic for Quantization parameter. 1'b1: It is fixed for Quantization parameter.
6:1	RW	0x00	Sw_adtion_latency The additional latency for decoder master interface. Can be used to slow down 8*sw_dec_latency cycles of IDLE between services, so if sw_dec_latency =0, that is no latency.
0	RW	0x0	Sw_dec_tiled_msb The enable for msb tiled mode. 1'b0: Tiled mode disable. 1'b1: Tiled mode enabled for 8x4 tile size.

**VDPU\_Swreg51**

Address: Operational Base + offset (0x000cc)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RW	0x00	Sw_qp_init_val The qp(quantization parameter)'s Initial value.
24	RW	0x0	Sw_strm_len_ext The extension bit of sw_strm_len.
23:0	RW	0x000000	Sw_strm_len The stream data bytes number in input buffer. If the buffer size be given small than it required, hw will give an interrupt, and then you should config again, and the stream start address should be config also. VC1: One picture/slice of the picture's should be included in the input buffer. H264/H263/MPEG*: One slice of the picture's should be included in the input buffer. JPEG: 256bytes or onepicture should be included in the input buffer.

**VDPU\_Swreg52**

Address: Operational Base + offset (0x000d0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:17	RW	0x0000	Sw_adv_pref_thrd The threshold value for advanced prefetch. When current MB num > this threshold value, then advanced mode will be closed.
16:8	RW	0x000	Sw_xdim_mbst The X dimension value for Start MB from SW. It may be used in error concealment case.
7:0	RW	0x00	Sw_ydim_mbst The Y dimension value for Start MB from SW. It may be used in error concealment case.

**VDPU\_Swreg53**

Address: Operational Base + offset (0x000d4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	Sw_dec_fmt_sel The dec format select. 4'd0: H.264 4'd1: MPEG-4 4'd2: H.263 4'd3: JPEG 4'd4: VC-1 4'd5: MPEG-2 4'd6: MPEG-1 4'd9: VP7 4'd11: AVS Others: Reserved

**VDPU\_Swreg54**

Address: Operational Base + offset (0x000d8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	Sw_dec_strendian_e The endian mode of stream data. 1'b0: Big endian (0-1-2-3 order). 1'b1: Little endian (3-2-1-0 order).
4	RW	0x0	Sw_dec_strm_wordsp The 32bit data swap for stream data. It will be used in 64 bit environment. 1'b0: No swapping. 1'b1: Swapping high and low 32bit data.

Bit	Attr	Reset Value	Description
3	RW	0x0	Sw_dec_out_wordsp The 32bit data swap for dec output data. It will be used in 64 bit environment. 1'b0: No swapping. 1'b1: Swapping high and low 32bit data.
2	RW	0x0	Sw_dec_in_wordsp The 32bit data swap for dec input data. It will be used in 64 bit environment. 1'b0: No swapping. 1'b1: Swapping high and low 32bit data. [Note]: It no used for stream data.
1	RW	0x0	Sw_dec_out_endian The endian mode of dec output. Decoder output endian mode: 1'b0: Big endian (0-1-2-3 order). 1'b1: Little endian (3-2-1-0 order).
0	RW	0x0	Sw_dec_in_endian The endian mode of dec input. 1'b0: Big endian (0-1-2-3 order). 1'b1: Little endian (3-2-1-0 order). [Note]: It no used for stream data.

**VDPU\_Swreg55**

Address: Operational Base + offset (0x000dc)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	Sw_timeout_det_sts The Interrupt status bit for tell us timeout detected. AXI in IDLE status too long.
12	RW	0x0	Sw_error_det_sts The Interrupt status bit for tell us error detected. Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset. (1,2,3,6,48,55,57).
11	RO	0x0	reserved
10	RW	0x0	Sw_bslicet_det_sts The Interrupt status bit for tell us B slice be detected. DIVX3: The value extension header flag.
9	RW	0x0	Sw_slice_det_sts The Interrupt status bit for tell us slice be decoded.
8	RW	0x0	Sw_aso_det_sts The Interrupt status bit for tell us ASO detectet. ASO: Arbitrary Slice Ordering.
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	Sw_buf_emt_sts The Interrupt status bit for tell input buffer empty.
5	RW	0x0	Sw_pp_bus_sts The Interrupt status bit for tell sw bus have some error.
4	RW	0x0	Sw_dec_rdy_sts The Interrupt status bit for tell sw processed a picture.
3:2	RO	0x0	reserved
1	RW	0x0	Sw_dec_irq_dis The decoder finish interrupt request diable flag. 1'b1: Use polling to see the interrupt. 1'b0: Use sw_pp_irq.
0	RW	0x0	Sw_dec_irq The decoder finish interrupt request. After sw query this interrupt, shoud write 0 to reset.

**VDPU\_Swreg56**

Address: Operational Base + offset (0x000e0)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	Sw_axi_sel Axi signals selected for encoder or decoder. 1'b0: Auto sel for encoder or decoder. 1'b1: Sel decoder (only used in the middle decoder frame to set bus_dec_en to 0).
22	RW	0x0	Sw_dec_data_discd_en Enable for Data discard. The fixed burst length will be used, and the more read datas will be auto discarded by hw.
21	RW	0x1	Sw_bus_pos_sel The parallel or serial mode for axi read and write. 1'b0: Serial 1'b1: Parallel
20:16	RW	0x00	Sw_dec_max_burlen The max burst length can be used by axi bus. Range: 1-16
15:8	RW	0x01	Sw_dec_axi_id_wr AXI Write ID If you config 0, will modify as 1 by hw.
7:0	RW	0x01	Sw_dec_axi_id_rd AXI Read ID If you config 0/5, will modify as 1 by hw.

**VDPU\_Swreg57**

Address: Operational Base + offset (0x000e4)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_dec_timeout_mode Dec timeout mode selset When 1'b0, timeout cycle is 181'b1. When 1'b1, timeout cycle is 221'b1.
30	RO	0x0	reserved
29	RW	0x0	Sw_cache_en 1'b1: Cache enable 1'b0: Cache disable When sw_cache_en is 1'b1, sw_pref_sigchan should also be 1'b1.
28	RW	0x0	Sw_pref_sigchan 1'b1: Prefetch single channel enable.
27	RW	0x0	Sw_intra_dbl3t In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block.
26	RW	0x0	Sw_intra_dbldspeed Intra double speed enable.
25	RW	0x0	Sw_inter_dbldspeed Inter double speed enable.
24:23	RO	0x0	reserved
22	RW	0x0	Sw_st_code_exist Existence flag for stream start code. 1'b0: Not exist 1'b1: Exist
21	RW	0x0	Sw_addit_ch_fmt_wen Enable for additional chrominance data format writing. Tiled mode should be disable, when this bit be used. Decoder writes chrominance: Group of 8 pixels of Cb then corresponding 8 pixels of Cr. Data is written to sw_dec_ch8pix_st_adr.
20	RW	0x0	Sw_rlc_mode_en Enable for RLC mode. 1'b0: Decoder data come from bit stream(VLC mode), side information (bitplane data in VC-1). 1'b1: Decoder data come from RLC input data, only h.264 and MPEG4 sp be valid.
19	RW	0x0	Sw_divx3_en Enable for divx3. Used sw_dec_fmt_sle= MPEG4. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
18	RW	0x0	Sw_prog_jpeg_en Enable flag for Progressive JPEG. 1'b0: Baseline JPEG. 1'b1: Progressive JPEG.
17	RW	0x0	Sw_curpic_code_sel The current picture coding mode select. 1'b0: Progressive 1'b1: Interlaced
16	RW	0x0	Sw_curpic_stru_sel The current picture Structure selected. 1'b0: Frame structure, (that isMBAFF structured picture is interlaced). 1'b1: Field structure.
15	RW	0x0	Sw_pic_type_sel1 Pic type sel1 flag. 1'b0: Desided by sw_pic_type_sel0. 1'b1: Picture type is BI/D/B. [Note]: BI is for vc1. D is for mpeg1. B is for h264.
14	RW	0x0	Sw_pic_type_sel0 Pic type sel0 flag. Should need sw_pic_type_sel1=0. 1'b0: Intra type (I). 1'b1: Inter type (P).
13	RW	0x0	Sw_pic_decfield_sel Select which field will be decoded. 1'b0: Bottom field 1'b1: Top field
12	RW	0x0	Sw_fwd_refpic_mode_sel Progressive and interlaced for coding mode. Used for forward reference picture. 1'b0: Progressive 1'b1: Interlaced The backward reference picture is the same as current picture.
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	Sw_dmmv_wr_en Enable flag for Direct mode motion vector write current picture. 1'b0: Disable 1'b1: Enable This bit used in MPEG2 is for the purpose error concealment case. This bit used in h264 is for the purpose write DPB case with the corresponding reference picture. This bit used in other decoder format is for the purpose writing to external memory starting from mv start address.
9	RW	0x0	Sw_reftop_en Enable flag for reference top field. Sw_dec_fmt_sel = VC-1 and sw_ref_frm = 0. 1'b0: Bottom field 1'b1: Top field
8	RW	0x0	Sw_first_reftop_en Enable flag for FWD reference top field have been decoded first. 1'b0: Fwd reference bottom field. 1'b1: Fwd reference top field.
7	RW	0x0	Sw_sequ_mbaff_en The enable flag for Sequence includes MBAFF coded pictures. 1'b0: Disable 1'b1: Enable
6	RW	0x0	Sw_rd_cnt_tab_en The enable flag for reading Picture order count table. Read data from memory used. 1'b0: Disable 1'b1: Enable (hw will read pic order counts).
5	RW	0x0	Sw_timeout_sts_en The enable flag for Timeout interrupt. 1'b0: Disable 1'b1: Enable (if hw can be working status too long, you will get an timeout interrupt).
4	RW	0x1	Sw_dec_clkgate_en The enable flag for Decoder auto clock gating. Default hw will reset to 1. 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	Sw_dec_wr_extmem_dis Disable flag for writing decoder output data to external memory. 1'b0: Enable 1'b1: Disable(no write to external memory).



Bit	Attr	Reset Value	Description
1	RW	0x0	Sw_refpic_buf2_en Enable flag for Refer picture buffer 2. 1'b0: Disable 1'b1: Enable (should : pic size > QVGA).
0	RW	0x0	Sw_dec_st_work Enable flag for decoder to start working. Hw will auto reset this be after a frame be decoded no matter it right or have some error.

**VDPU\_Swreg58**

Address: Operational Base + offset (0x000e8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Sw_soft_rst The soft reset for decoder or pp or encoder. Write 1 to reset, and it will auto reset to 0 after one cycle.

**VDPU\_Swreg59**

Address: Operational Base + offset (0x000ec)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Sw_pflt_set0_tap0 Prediction filter Set 0, tap 0
21:12	RW	0x000	Sw_pflt_set0_tap1 Prediction filter Set 0, tap 1
11:2	RW	0x000	Sw_pflt_set0_tap2 Prediction filter Set 0, tap 2
1:0	RO	0x0	reserved

**VDPU\_Swreg60**

Address: Operational Base + offset (0x000f0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_addit_ch_st_adr The start address for additional chrominance data format. The usage is enabled by sw_addit_ch_fmt_wen.
1:0	RO	0x0	reserved

**VDPU\_Swreg61**

Address: Operational Base + offset (0x000f4)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_qtable_st_adr Standard dependent tables start address JPEG: AC,DC, QP tables. MPEG4/2: QP table. H.264: Various tables. VP7: Stream decoding tables.
1:0	RO	0x0	reserved

**VDPU\_Swreg62**

Address: Operational Base + offset (0x000f8)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_dmmv_st_adr Direct mode motion vector write/read start address. H264: Direct mode motion vector write/read start address. Progressive JPEG: The start address for ACDC coefficient read/write. If current round is for DC components: This start address is pointing to luminance. AC component rounds: This start address is used for current type.
1:0	RO	0x0	reserved

**VDPU\_Swreg63**

Address: Operational Base + offset (0x000fc)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_dec_out_st_adr Write decoder output picture or field start address. Video: Write decoder output picture or field start address. JPEG snapshot: Wiret decoder output luminance picture start address.
1:0	RO	0x0	reserved

**VDPU\_Swreg64**

Address: Operational Base + offset (0x00100)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_rlc_vlc_st_adr Rlc or vlc mode input data start addr. RLC mode: RLC data start address. VLC mode: Stream start address. HW return value of last_byte_address by this register to tell where stream has been read when you get some abnormality interrupt, may be used for debug. VP7: DCT stream for MB rows 0, 2n start address.
1:0	RO	0x0	reserved

**VDPU\_Swreg65**

Address: Operational Base + offset (0x00104)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_refbu_e 1'b0: Disable 1'b1: Enable
30:19	RW	0x000	Sw_refbu_thr_level Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed).
18:14	RW	0x00	Sw_refbuf_picid The picture id for reference buffer.
13	RW	0x0	Sw_refbuf_idcal_e Enable for HW internal reference ID calculation. If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture.
12	RW	0x0	Sw_refbuf_fildpar_mod_e The mode enable for Field parity mode enable. 1'b0: The result field of the evaluation be used. 1'b1: The parity mode field be used.
11:9	RO	0x0	reserved
8:0	RW	0x000	Sw_refbuf_y_offset The y offset for rebufferd. If hw should compensate the global motion of the video for better buffer hit rate will use this coordinate.

**VDPU\_Swreg66**

Address: Operational Base + offset (0x00108)

Bit	Attr	Reset Value	Description
31:16	RO	0x6731	Prod_id Product number

Bit	Attr	Reset Value	Description
15:12	RO	0x2	Major_num Major_num
11:4	RO	0x68	Minor_num Minor_num
3	RO	0x1	Ascii_id_en Enable for ASCII product ID.
2:0	RO	0x0	Build_ver Build_ver

**VDPU\_Swreg67**

Address: Operational Base + offset (0x0010c)

Bit	Attr	Reset Value	Description
31	RO	0x1	Jpeg_allow_flag JPEG sampling support 16Mpixel~67Mpixel be sampled and supported by 411 and 444.
30	RO	0x1	Refbuf_allow_flag Ref buffer support 1'b0: No support 1'b1: Support
29	RO	0x0	reserved
28	RO	0x0	Refbuf2_allow_flag Refbuffer2 support
27:26	RO	0x0	reserved
25	RO	0x0	Rom_imp_type Rom implementation type. 1'b0: From actual ROM units. 1'b1: From RTL.
24	RO	0x1	Vp7_allow_flag Vp7 support
23	RO	0x0	reserved
22	RO	0x1	Avs_allow_flag Avs support
21:20	RO	0x1	Mvc_allow_flag Mvc support
19	RO	0x0	reserved
18:17	RO	0x1	Tile_mode_sel Tile mode support 2'd0: No support 2'd1: 8x4 support 2'd2,2'd3: No used
16:0	RO	0x0	reserved

**VDPU\_Swreg68**

Address: Operational Base + offset (0x00110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Sw_refbuf_sum_top Sum of the top partitions.
15:0	RO	0x0000	Sw_refbuf_sum_bot Sum of the bottom partitions.

**VDPU\_Swreg69**

Address: Operational Base + offset (0x00114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Sw_refbuf_sum_hit Sum of the rebuffered hits of the picture.
15:0	RO	0x0000	Sw_luma_sum_intra Sum of the luminance 8x8 intra partitions of the picture.

**VDPU\_Swreg70**

Address: Operational Base + offset (0x00118)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RO	0x000000	Sw_ycomp_mv_sum Sum of the decoded motion vector y-components.

**VDPU\_Swreg71**

Address: Operational Base + offset (0x0011c)

Bit	Attr	Reset Value	Description
31	RO	0x1	Dec_mpeg2_allow Decoding format support, for MPEG-2 / MPEG-1. 1'b0: Not supported 1'b1: Support
30:29	RO	0x3	Dec_vc1_allow Decoding format support, VC-1. 2'd0: Not supported. 2'd1: Simple profile be supported. 2'd2: Main profile be supported. 2'd3: Advanced profile be supported.
28	RO	0x1	Dec_jpeg_allow Decoding format support for JPEG. 1'b0: Not supported 1'b1: Support
27:26	RO	0x2	Dec_mpeg4_allow Decoding format support for MPEG-4 / H.263. 2'd0: Not supported. 2'd1: Simple profile be supported. 2'd2: Advanced simple profile be supported.

Bit	Attr	Reset Value	Description
25:24	RO	0x3	Dec_h264_allow H264 be support 2'd0: No support. 2'd1: Baseline profile be supported. 2'd2: High profile be supported.
23	RO	0x0	reserved
22	RO	0x0	Dec_prog_jpeg_allow Support for progressive jpeg 1'b0: Not supported 1'b1: Support
21	RO	0x1	Outbuf_sel Output buffer selected 1'b0: 1MB buffer be used. 1'b1: 4MB buffer be used.
20	RO	0x1	Refbuf_exist Reference buffer support 1'b0: Not supported 1'b1: Support
19:16	RO	0x5	Dec_std_bus 4'd0: Error 4'd1: AHB master, AHB slave. 4'd2: OCP master, OCP slave. 4'd3: AXI master, AXI slave. 4'd4: AXI master, APB slave. 4'd5: AXI master, AHB slave.
15:14	RO	0x1	Rtl_lan_sel 2'd0: No used 2'd1: Vhdl 2'd2: Verilog
13:12	RO	0x2	Bus_w 2'd0: Error 2'd1: Word bus 2'd2: Double word bus 2'd3: Quadruple word bus
11	RO	0x0	reserved
10:0	RO	0x780	Sw_dec_max_allow_w The max width can be decoder.

**VDPU\_Swreg72**

Address: Operational Base + offset (0x00120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	Debug_service Debug_service signals This value[6:0]=service_wr[2:0], service_rd[3:0].

Bit	Attr	Reset Value	Description
23:0	RO	0x0	reserved

**VDPU\_Swreg73**

Address: Operational Base + offset (0x00124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	Debug_mv_req Mvst_mv_req signal value.
29	RO	0x0	Debug_rlc_req Prtr_res_y_req signal value.
28	RO	0x0	Debug_res_y_req Prtr_res_y_req signal value.
27	RO	0x0	Debug_res_c_req Debug_res_c_req
26	RO	0x0	Debug_strm_da_e Debug_strm_da_e
25	RO	0x0	Debug_frm_rdy Debug_frm_rdy
24	RO	0x0	Debugflt_req Debugflt_req
23	RO	0x0	Debug_ref0_req Debug_ref0_req
22	RO	0x0	Debug_ref1_req Debug_ref1_req
21	RO	0x0	reserved
20:0	RO	0x000000	Debug_mb_cnt Debug_mb_cnt

**VDPU\_Swreg74**

Address: Operational Base + offset (0x00128)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_diff_mv_st_adr The Differential motion vector start address. Differential motion vector base address used for h264 only. It also reuse used as: [29:25]: 9st forward picid of inital reference pic list. [24:20]: 8st forward picid of inital reference pic list. [19:15]: 7st forward picid of inital reference pic list. [14:10]: 6st forward picid of inital reference pic list. [9:5]: 5st forward picid of inital reference pic list. [4:0]: 4st forward picid of inital reference pic list.
1:0	RO	0x0	reserved

**VDPU\_Swreg75**

Address: Operational Base + offset (0x0012c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_pred4x4_st_adr H.264 Intra prediction 4x4 mode start address. Also be used as: [29:25]: 15st forward picid of initial reference pic list. [24:20]: 14st forward picid of initial reference pic list. [19:15]: 13st forward picid of initial reference pic list. [14:10]: 12st forward picid of initial reference pic list. [9:5]: 11st forward picid of initial reference pic list. [4:0]: 10st forward picid of initial reference pic list.
1:0	RO	0x0	reserved

**VDPU\_Swreg76**

Address: Operational Base + offset (0x00130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx1 The number of reference pic index1.
15:0	RW	0x0000	H264_num_ref_idx0 The number of reference pic index0.

**VDPU\_Swreg77**

Address: Operational Base + offset (0x00134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx3 The number of reference pic index3.
15:0	RW	0x0000	H264_num_ref_idx2 The number of reference pic index2.

**VDPU\_Swreg78**

Address: Operational Base + offset (0x00138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx5 The number of reference pic index5.
15:0	RW	0x0000	H264_num_ref_idx4 The number of reference pic index4.

**VDPU\_Swreg79**

Address: Operational Base + offset (0x0013c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx7 The number of reference pic index7.



Bit	Attr	Reset Value	Description
15:0	RW	0x0000	H264_num_ref_idx6 The number of reference pic index6.

**VDPU\_Swreg80**

Address: Operational Base + offset (0x00140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx9 The number of reference pic index9.
15:0	RW	0x0000	H264_num_ref_idx8 The number of reference pic index8.

**VDPU\_Swreg81**

Address: Operational Base + offset (0x00144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx11 The number of reference pic index11.
15:0	RW	0x0000	H264_num_ref_idx10 The number of reference pic index10.

**VDPU\_Swreg82**

Address: Operational Base + offset (0x00148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx13 The number of reference pic index13.
15:0	RW	0x0000	H264_num_ref_idx12 The number of reference pic index12.

**VDPU\_Swreg83**

Address: Operational Base + offset (0x0014c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_num_ref_idx15 The number of reference pic index15.
15:0	RW	0x0000	H264_num_ref_idx14 The number of reference pic index14.

**VDPU\_Swreg84**

Address: Operational Base + offset (0x00150)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref0_st_addr The start address of reference frame0.

Bit	Attr	Reset Value	Description
1	RW	0x0	H264_ref0_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref0_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg85**

Address: Operational Base + offset (0x00154)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref1_st_addr The start address of reference frame1.
1	RW	0x0	H264_ref1_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref1_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg86**

Address: Operational Base + offset (0x00158)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref2_st_addr The start address of reference frame2.
1	RW	0x0	H264_ref2_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref2_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg87**

Address: Operational Base + offset (0x0015c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref3_st_addr The start address of reference frame3.

Bit	Attr	Reset Value	Description
1	RW	0x0	H264_ref3_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref3_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPUSwreg88**

Address: Operational Base + offset (0x00160)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref4_st_addr The start address of reference frame4.
1	RW	0x0	H264_ref4_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref4_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPUSwreg89**

Address: Operational Base + offset (0x00164)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref5_st_addr The start address of reference frame5.
1	RW	0x0	H264_ref5_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref5_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPUSwreg90**

Address: Operational Base + offset (0x00168)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref6_st_addr The start address of reference frame6.

Bit	Attr	Reset Value	Description
1	RW	0x0	H264_ref6_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref6_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg91**

Address: Operational Base + offset (0x0016c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref7_st_addr The start address of reference frame7.
1	RW	0x0	H264_ref7_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref7_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg92**

Address: Operational Base + offset (0x00170)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref8_st_addr The start address of reference frame8.
1	RW	0x0	H264_ref8_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref8_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg93**

Address: Operational Base + offset (0x00174)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref9_st_addr The start address of reference frame9.

Bit	Attr	Reset Value	Description
1	RW	0x0	H264_ref9_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref9_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg94**

Address: Operational Base + offset (0x00178)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref10_st_addr The start address of reference frame10.
1	RW	0x0	H264_ref10_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref10_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg95**

Address: Operational Base + offset (0x0017c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref11_st_addr The start address of reference frame11.
1	RW	0x0	H264_ref11_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref11_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg96**

Address: Operational Base + offset (0x00180)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref12_st_addr The start address of reference frame12.

Bit	Attr	Reset Value	Description
1	RW	0x0	H264_ref12_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref12_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg97**

Address: Operational Base + offset (0x00184)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref13_st_addr The start address of reference frame13.
1	RW	0x0	H264_ref13_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref13_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg98**

Address: Operational Base + offset (0x00188)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref14_st_addr The start address of reference frame14.
1	RW	0x0	H264_ref14_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref14_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg99**

Address: Operational Base + offset (0x0018c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	H264_ref15_st_addr The start address of reference frame15.

Bit	Attr	Reset Value	Description
1	RW	0x0	H264_ref15_field_en The type Refer picture consist of. 1'b0: Frame 1'b1: Field
0	RW	0x0	H264_ref15_closer_sel Which field is more closer to current picture. 1'b0: Bottom field be selected. 1'b1: Top field be selected.

**VDPU\_Swreg100**

Address: Operational Base + offset (0x00190)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	H264_init_reflist_df5 5st initial reference picture list for direct forward picid. Used for h264
24:20	RW	0x00	H264_init_reflist_df4 4st initial reference picture list for direct forward picid. Used for h264
19:15	RW	0x00	H264_init_reflist_df3 3st initial reference picture list for direct forward picid. Used for h264
14:10	RW	0x00	H264_init_reflist_df2 2st initial reference picture list for direct forward picid. Used for h264
9:5	RW	0x00	H264_init_reflist_df1 1st initial reference picture list for direct forward picid. Used for h264
4:0	RW	0x00	H264_init_reflist_df0 0st initial reference picture list for direct forward picid. Used for h264

**VDPU\_Swreg101**

Address: Operational Base + offset (0x00194)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	H264_init_reflist_df11 11st initial reference picture list for direct forward picid. Used for h264
24:20	RW	0x00	H264_init_reflist_df10 10st initial reference picture list for direct forward picid. Used for h264

Bit	Attr	Reset Value	Description
19:15	RW	0x00	H264_init_reflist_df9 9st initial reference picture list for direct forward picid. Used for h264
14:10	RW	0x00	H264_init_reflist_df8 8st initial reference picture list for direct forward picid. Used for h264
9:5	RW	0x00	H264_init_reflist_df7 7st initial reference picture list for direct forward picid. Used for h264
4:0	RW	0x00	H264_init_reflist_df6 6st initial reference picture list for direct forward picid. Used for h264

**VDPU\_Swreg102**

Address: Operational Base + offset (0x00198)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	H264_init_reflist_df15 15st initial reference picture list for direct forward picid. Used for h264
14:10	RW	0x00	H264_init_reflist_df14 14st initial reference picture list for direct forward picid. Used for h264
9:5	RW	0x00	H264_init_reflist_df13 13st initial reference picture list for direct forward picid. Used for h264
4:0	RW	0x00	H264_init_reflist_df12 12st initial reference picture list for direct forward picid. Used for h264

**VDPU\_Swreg103**

Address: Operational Base + offset (0x0019c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	H264_init_reflist_db5 5st initial reference picture list for direct backward picid. Used for h264
24:20	RW	0x00	H264_init_reflist_db4 4st initial reference picture list for direct backward picid. Used for h264
19:15	RW	0x00	H264_init_reflist_db3 3st initial reference picture list for direct backward picid. Used for h264



Bit	Attr	Reset Value	Description
14:10	RW	0x00	H264_init_reflist_db2 2st initial reference picture list for direct backward picid. Used for h264
9:5	RW	0x00	H264_init_reflist_db1 1st initial reference picture list for direct backward picid. Used for h264
4:0	RW	0x00	H264_init_reflist_db0 0st initial reference picture list for direct backward picid. Used for h264

**VDPU\_Swreg104**

Address: Operational Base + offset (0x001a0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	H264_init_reflist_db11 11st initial reference picture list for direct backward picid. Used for h264
24:20	RW	0x00	H264_init_reflist_db10 10st initial reference picture list for direct backward picid. Used for h264
19:15	RW	0x00	H264_init_reflist_db9 9st initial reference picture list for direct backward picid. Used for h264
14:10	RW	0x00	H264_init_reflist_db8 8st initial reference picture list for direct backward picid. Used for h264
9:5	RW	0x00	H264_init_reflist_db7 7st initial reference picture list for direct backward picid. Used for h264
4:0	RW	0x00	H264_init_reflist_db6 6st initial reference picture list for direct backward picid. Used for h264

**VDPU\_Swreg105**

Address: Operational Base + offset (0x001a4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	H264_init_reflist_db15 15st initial reference picture list for direct backward picid. Used for h264
14:10	RW	0x00	H264_init_reflist_db14 14st initial reference picture list for direct backward picid. Used for h264

Bit	Attr	Reset Value	Description
9:5	RW	0x00	H264_init_reflist_db13 13st initial reference picture list for direct backward picid. Used for h264
4:0	RW	0x00	H264_init_reflist_db12 12st initial reference picture list for direct backward picid. Used for h264

**VDPU\_Swreg106**

Address: Operational Base + offset (0x001a8)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	H264_init_reflist_pf3 3st initial reference picture list for P forward picid. Initial reference picture list for P forward picid 3.
14:10	RW	0x00	H264_init_reflist_pf2 2st initial reference picture list for P forward picid. Initial reference picture list for P forward picid 2.
9:5	RW	0x00	H264_init_reflist_pf1 1st initial reference picture list for P forward picid. Initial reference picture list for P forward picid 1.
4:0	RW	0x00	H264_init_reflist_pf0 0st initial reference picture list for P forward picid. Used for h264

**VDPU\_Swreg107**

Address: Operational Base + offset (0x001ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	H264_refpic_term_flag Long term flag for reference picture index.

**VDPU\_Swreg108**

Address: Operational Base + offset (0x001b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	H264_refpic_valid_flag Valid flag for reference picture index.

**VDPU\_Swreg109**

Address: Operational Base + offset (0x001b4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	H264_strm_start_bit The stream start word for decoder. Associates with sw_rlc_vlc_st_adr.

**VDPU\_Swreg110**

Address: Operational Base + offset (0x001b8)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:22	RW	0x00	H264_flt_offset_cr_qp Filter offset of cr qp.
21:17	RW	0x00	H264_flt_offset_cb_qp Filter offset of cb qp.
16:9	RW	0x00	H264_pic_mb_h Picture height in macroblocks. Value = ((pixel height+15)/16). Used for frame or single field size being decoded.
8:0	RW	0x000	H264_pic_mb_w Picture width in macroblocks. Value = ((pixel width + 15) /16).

**VDPU\_Swreg111**

Address: Operational Base + offset (0x001bc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x0	H264_wp_bslicel_sel Wp(weighted prediction) specification for B slice. 2'd0: Default wp be used. 2'd1: Explicit wp be used. 2'd2: Implicit wp be used.
15:5	RO	0x0	reserved
4:0	RW	0x00	H264_max_refnum Short and long term reference frames's maximum number. This value is for decoded picture buffer.

**VDPU\_Swreg112**

Address: Operational Base + offset (0x001c0)

Bit	Attr	Reset Value	Description
31	RW	0x0	H264_dblk_ctrl_flag The control present flag of deblocking filter. To indicates if the slice header will have the deblocking filter's extra variables controlling characteristics.
30	RW	0x0	H264_rpcp_flag Redundant picture count present flag. To specifies whether redundant picture count syntax elements.
29:21	RO	0x0	reserved
20:16	RW	0x00	H264_curfrm_len The bit length of input data stream's frame num. H.264: Bit length of frame_num in data stream.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	H264_curfrm_num The current frame number for h264. It may be use for reference picture reordering and identify short-term reference frames.

**VDPU\_Swreg113**

Address: Operational Base + offset (0x001c4)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	H264_mk_len The length of marking bits. Use for decoded reference picture.
15:0	RW	0x0000	H264_idrp_id Instantaneous decoding refresh picture id.

**VDPU\_Swreg114**

Address: Operational Base + offset (0x001c8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	H264_pps_id The id for picture parameter set. It identifies the slice header will have the id of picture parameter set.
23:19	RW	0x00	H264_max_refidx1 The maximum reference index 1. It will be used in decoding inter predicted macro blocks.
18:14	RW	0x00	H264_max_refidx0 The maximum reference index 0. It will be used in decoding inter predicted macro blocks.
13:8	RO	0x0	reserved
7:0	RW	0x00	H264_pocf_len The length of picture order count field in stream The length of picture order count field in stream.

**VDPU\_Swreg115**

Address: Operational Base + offset (0x001cc)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	H264_idr_pic_flag Instantaneous decoding refresh picture flag.
7	RW	0x0	H264_dlmv_method_en The method to use to derive luma motion vectors. With B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag.

Bit	Attr	Reset Value	Description
6	RW	0x0	H264_monochr_en Monochromatic enable. Sampling format. 1'b0: 4:2:0 1'b1: 4:0:0
5	RW	0x0	H264_cabac_en Enable for cabac.
4	RW	0x0	H264_pslice_wp_en Enable flag of Weighted prediction for P slices.
3	RW	0x0	H264_nimb_intra_en If intra prediction uses only neighbouring intra macroblocks. 1'b0: Neighbouring inter macroblocks are used in intra prediction process. 1'b1: Neighbouring intra macroblocks are used.
2	RW	0x0	H264_tranf_flag_en_8x8 8x8 transform flag enable for stream decoding.
1	RW	0x0	H264_scl_matrix_en Scaling matrix enable. 1'b0: Normal transform. 1'b1: Use scaling matrix for transform.
0	RW	0x0	H264_fieldpic_flag_exist Flag for streamd that field_pic_flag exists in stream.

**VDPU\_Swreg120**

Address: Operational Base + offset (0x001e0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg0 Multi format reuse register0 except h264. MPEG4/JPEG/VC-1/MPEG2/VP6/VP7/VP: [31:2] RLC mode: Base address for RLC data. VLC mode: Stream start address. VP7: [31:2] This base address is used as sw_dct_strm0_base including DCT stream for MB rows 0,2n.

**VDPU\_Swreg121**

Address: Operational Base + offset (0x001e4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg1 Multi format reuse register1 except h264. Vc-1: [31]: Bitplane mode enable for corresponding element0. [30]: Bitplane mode enable for corresponding element1. [29]: Bitplane mode enable for corresponding element2. [28:24]: Alemnative PQUANT. [23:20]: Weather dq_profile will be set to picture edges. [19]: TTMB or TTFRM sel. [18:14]: Qpindex value. [12]: Enable for bilinear motion compensation ena. [11]: Enable for iform quantizer e. [10]: Enable for HALFQP. [9:8]: Frame level transform type sel. [7]: The 2st byte of the stream emulation byte. [6]: Enable for antization parameter change inside frame. [5]: Enable for VC-1 advanced profile. JPEG: [26:0]: Progressive JPEG. MPEG2: [12]: Enable for bilinear motion compensation. VP7: [31:26]: DCT stream partition index 1 of start bit. [25:20]: DCT stream partition index 2 of start bit. [13]: Rominance motion vector resolution for VP7/8. [12]: Enable for bilinear motion compensation. [11:9]: 0st count for DC prediction mach. [8:6]: 1st count for DC prediction mach.</p>

**VDPUs\_Swreg122**

Address: Operational Base + offset (0x001e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg2</p> <p>Multi format reuse register2 except h264.</p> <p>MPEG4:</p> <p>[31:26]: Exact bit of stream start word.</p> <p>[25]: Enable for sync markers.</p> <p>[24]: Enable for Type 1 quantization.</p> <p>[23:19]: The offset of Qp filter.</p> <p>[18:14]: The offset of Qp filter for cr.</p> <p>[0]: Filed_pic_flag exists in stream.</p> <p>JPEG:</p> <p>[31:26]: Exact bit of stream start word.</p> <p>[25]: Enable for sync markers.</p> <p>[12:11]: Total of Quantization tables.</p> <p>[10:8]: The sampling format for input pic.</p> <p>[7]: JPEG width.</p> <p>[6]: Weather current strem buffer contain the end of a JPEG image.</p> <p>[5:0]: Vlc table.</p> <p>VC-1:</p> <p>[31:26]: Exact bit of stream start word.</p> <p>[25]: Enable for sync markers.</p> <p>[24]: Quantisation profile.</p> <p>[23]: Each mb take on quantization step size or not.</p> <p>[22]: Range reduced.</p> <p>[20]: Chrominance interpolation accuracy information.</p> <p>[17:13]: Select tables which be used to dec.</p> <p>[12:10]: Select mode syntax element table.</p> <p>[9:7]: Select mv table.</p> <p>[6:4]: Select CPBCY table.</p> <p>[3:0]: Block pattern table select.</p> <p>Vp6:</p> <p>[23:18]: Start bit for ctrl stream (vp7).</p> <p>[17]: Enable for huffman decoding.</p> <p>[16]: Enable for muti stream (vp7).</p> <p>[15:8]: Boolean dec init value(vp7).</p> <p>[7:0]: Boolean dec init range.</p>

**VDPU\_Swreg123**

Address: Operational Base + offset (0x001ec)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg3</p> <p>Multi format reuse register3 except h264.</p> <p>JPEG:</p> <p>[15:0]: Start marker frequency.</p> <p>Vc-1:</p> <p>[31:24]: B picture scl factor.</p> <p>[23:19]: Fwd direction reference distance.</p> <p>[18:14]: Bwd direction reference distance.</p> <p>Vp6:</p> <p>[17:14]: Loop filter limit value.</p> <p>[13]: Enable for variance test.</p> <p>[12:10]: Filter MV size threshold.</p> <p>[9:0]: Filter variance threshold.</p> <p>VP7/VP:</p> <p>[31:16]: Value 0 for inital dc predictor.</p> <p>[15:0]: Value 1 for inital dc predictor.</p>

**VDPU\_Swreg124**

Address: Operational Base + offset (0x001f0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg4</p> <p>Multi format reuse register4 except h264.</p> <p>MPEG4:</p> <p>[31:2]: MB ctrl start address.</p> <p>VC-1:</p> <p>[24]: Enable for 0st intensity compensation.</p> <p>[23:16]: Iscale value.</p> <p>[15:0]: Ishift value.</p> <p>VP6:</p> <p>[23:0]: Total of CTRL stream data.</p> <p>VP7/VP:</p> <p>[27:24]: Coefficient partitions number.</p> <p>[23:0]: Total of CTRL stream data.</p>

**VDPU\_Swreg125**

Address: Operational Base + offset (0x001f4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg5</p> <p>Multi format reuse register5 except h264.</p> <p>JPEG:</p> <p>[31:2]: Cb ACDC coeff start address.</p> <p>VP6/VP7/vp:</p> <p>[31:22]: Prediction filter with set 5 and tap 1.</p> <p>[21:12]: Prediction filter with set 5 and tap 2.</p> <p>[11:2]: Prediction filter with set 5 and tap 3.</p>



**VDPU\_Swreg126**

Address: Operational Base + offset (0x001f8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg6 Multi format reuse register6 except h264. JPEG: [31:2]: Cr ACDC coeff start address. VP6/VP7/vp: [31:22]: Prediction filter with set 6 and tap 0. [21:12]: Prediction filter with set 6 and tap 1. [11:2]: Prediction filter with set 6 and tap 2.

**VDPU\_Swreg127**

Address: Operational Base + offset (0x001fc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg7 Multi format reuse register7 except h264. VP6/VP7/vp: [31:22]: Prediction filter with set 6 and tap 3. [21:12]: Prediction filter with set 7 and tap 0. [11:2]: Prediction filter with set 7 and tap 1.

**VDPU\_Swreg128**

Address: Operational Base + offset (0x00200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg8 Multi format reuse register8 except h264. VP6: [31:22]: Prediction filter with set 7 and tap 2. [21:12]: Prediction filter with set 7 and tap 3. VP7/VP: [31:22]: Prediction filter with set 7 and tap 2. [21:12]: Prediction filter with set 7 and tap 3. [11:10]: Extra prediction filter with set 2 and tap -1. [9:8]: Extra prediction filter with set 2 and tap 4. [7:6]: Extra prediction filter with set 4 and tap -1. [5:4]: Extra prediction filter with set 4 and tap 4. [3:2]: Extra prediction filter with set 6 and tap -1. [1:0]: Extra prediction filter with set 6 and tap 4.

**VDPU\_Swreg129**

Address: Operational Base + offset (0x00204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg9 Multi format reuse register9 except h264. VP6: [29:24]: 56st coef of scan read index. [23:18]: 57st coef of scan read index. [17:12]: 58st coef of scan read index. [11:6]: 59st coef of scan read index. [5:0]: 60st coef of scan read index.

**VDPU\_Swreg130**

Address: Operational Base + offset (0x00208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg10 Multi format reuse register10 except h264. VP6: [29:24]: 61st coef of scan read index. [23:18]: 62st coef of scan read index. [17:12]: 63st coef of scan read index. VP7: [21:11]: QP0 for VP7. [10:0]: QP1 for VP7.

**VDPU\_Swreg131**

Address: Operational Base + offset (0x0020c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg11 Multi format reuse register11 except h264. MPEG4/H263/VC-1/VP6/VP7: [31:2]: Reference pic0 start address. JPEG: [31:2]: The ch decoder output start address.

**VDPU\_Swreg132**

Address: Operational Base + offset (0x00210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg12 Multi format reuse register12 except h264. VP7: [31]: Type of loop filter. [27:21]: MB type0 adjustment of filter level. [20:14]: MB type1 adjustment of filter level. [13:7]: MB type2 adjustment of filter level. [6:0]: MB type3 adjustment of filter level.

**VDPU\_Swreg133**

Address: Operational Base + offset (0x00214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg13 Multi format reuse register13 except h264.</p> <p>VP6: [29:24]: 51st coef of scan read index. [23:18]: 52st coef of scan read index. [17:12]: 53st coef of scan read index. [11:6]: 54st coef of scan read index. [5:0]: 55st coef of scan read index.</p> <p>VP7: [27:21]: Reference frame type0 adjustment of filter level. [20:14]: Reference frame type1 adjustment of filter level. [13:7]: Reference frame type2 adjustment of filter level. [6:0]: Reference frame type3 adjustment of filter level.</p>

**VDPU\_Swreg134**

Address: Operational Base + offset (0x00218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg14 Multi format reuse register14 except h264.</p> <p>MPEG4/vc1/MEPG2: [31:2]: Reference pic2 start address.</p> <p>JPEG: [30:24]: Code words of length 6. [21:16]: Code words of length 5. [15:11]: Code words of length 4. [10:7]: Code words of length 3. [5:3]: Code words of length 2. [1:0]: Code words of length 1.</p>

**VDPU\_Swreg135**

Address: Operational Base + offset (0x0021c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg15 Multi format reuse register15 except h264.</p> <p>MPEG4/vc1/MEPG2: [31:2]: Reference pic3 start address.</p> <p>JPEG: [30:24]: Code words of length 10. [23:16]: Code words of length 9. [15:8]: Code words of length 8. [7:0]: Code words of length 7.</p>

**VDPU\_Swreg136**

Address: Operational Base + offset (0x00220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg16 Multi format reuse register16 except h264. VP6/VP7: [31:2]: Golden reference pic start address(PIC_ID 4). [0]: Golden reference pic siggn bias(VP7/VP8). VC-1: [31:16]: Length of picture header. [13]: 1/4 MV/MB sel. [11]: Enable for ref pic range reduce. [10:9]: Max different mv length. [7:6]: Select range for mv. [5]: Enable for overlap smoothing. [4:3]: MB overlap smoothing method. MPEG4/MPEG2: [19]: Alternalte scan flag. [18:15]: HRZ AXI's bit amount for representing FWD MV. [14:11]: VRZ AXI's bit amount for representing FWD MV. [10:7]: HRZ AXI's bit amount for representing BWD MV. [6:3]: VRZ AXI's bit amount for representing BWD MV. [2]: FWD MV Y resolution. [1]: The ctrl bit for rounding(MPEG4), BWD MV Y resolution(MPEG2). [0]: Pic type of previous anchor(MPEG4). JPEG: [30:24]: Code words of length 14. [23:16]: Code words of length 13. [15:8]: Code words of length 12. [7:0]: Code words of length 11.</p>

**VDPU\_Swreg137**

Address: Operational Base + offset (0x00224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg17 Multi format reuse register17 except h264. MPEG4: [26:0]: Reference distance syntax for delta value0 be used. JPEG: [31:27]: Tab2 code words of length 4. [26:23]: Tab2 code words of length 3. [21:19]: Tab2 code words of length 2. [17:16]: Tab2 code words of length 1. [15:8]: Tab1 code words of length 16. [7:0]: Tab1 code words of length 15. VC-1: [24] : Enable for intensity compensation 3. [23:16]: Intensity compensation's iscale value. [15:0]: Intensity compensation's ishift value. VP6/VP7: [29:24]: 1st coef of scan read index. [23:18]: 2st coef of scan read index. [17:12]: 3st coef of scan read index. [11:6]: 4st coef of scan read index. [5:0]: 5st coef of scan read index.</p>

**VDPU\_Swreg138**

Address: Operational Base + offset (0x00228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg18 Multi format reuse register18 except h264. MPEG4: [26:0]: Reference distance syntax for delta value -1 be used. JPEG: [31:24]: Tab2 code words of length 8. [23:16]: Tab2 code words of length 7. [14:8]: Tab2 code words of length 6. [5:0]: Tab2 code words of length 5. VC-1: [24]: Enable for intensity compensation 4. [23:16]: Intensity compensation's iscale value. [15:0]: Intensity compensation's shift value. VP6/VP7: [29:24]: 6st coef of scan read index. [23:18]: 7st coef of scan read index. [17:12]: 8st coef of scan read index. [11:6]: 9st coef of scan read index. [5:0]: 10st coef of scan read index.</p>

**VDPU\_Swreg139**

Address: Operational Base + offset (0x0022c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg19 Multi format reuse register19 except h264. MPEG4: [26:0]: Reference distance syntax for delta value1 be used. JPEG: [31:24]: Tab2 code words of length 12. [23:16]: Tab2 code words of length 11. [15:8]: Tab2 code words of length 10. [7:0]: Tab2 code words of length 9. VP6/VP7: [29:24]: 11st coef of scan read index. [23:18]: 12st coef of scan read index. [17:12]: 13st coef of scan read index. [11:6]: 14st coef of scan read index. [5:0]: 15st coef of scan read index.</p>

**VDPU\_Swreg140**

Address: Operational Base + offset (0x00230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg20 Multi format reuse register20 except h264. JPEG: [31:24]: Tab2 code words of length 16. [23:16]: Tab2 code words of length 15. [15:8]: Tab2 code words of length 14. [7:0]: Tab2 code words of length 13. VP6: [29:24]: 16st coef of scan read index. [23:18]: 17st coef of scan read index. [17:12]: 18st coef of scan read index. [11:6]: 19st coef of scan read index. [5:0]: 20st coef of scan read index. VP7: [31:2]: DCT stream MB row 2, 2n+1 start address.</p>

**VDPU\_Swreg141**

Address: Operational Base + offset (0x00234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg21</p> <p>Multi format reuse register21 except h264.</p> <p>JPEG:</p> <p>[31:28]: Tab1 code words of length 8.</p> <p>[27:24]: Tab1 code words of length 7.</p> <p>[23:20]: Tab1 code words of length 6.</p> <p>[19:16]: Tab1 code words of length 5.</p> <p>[15:12]: Tab1 code words of length 4.</p> <p>[11:8]: Tab1 code words of length 3.</p> <p>[6:4]: Tab1 code words of length 2.</p> <p>[1:0]: Tab1 code words of length 1.</p> <p>VP6:</p> <p>[29:24]: 21st coef of scan read index.</p> <p>[23:18]: 22st coef of scan read index.</p> <p>[17:12]: 23st coef of scan read index.</p> <p>[11:6]: 24st coef of scan read index.</p> <p>[5:0]: 25st coef of scan read index.</p> <p>VP7:</p> <p>[31:2]: DCT stream MB row 2, 2n+2 start address.</p>

**VDPU\_Swreg142**

Address: Operational Base + offset (0x00238)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg22</p> <p>Multi format reuse register22 except h264.</p> <p>JPEG:</p> <p>[31:28]: Tab1 code words of length 16.</p> <p>[27:24]: Tab1 code words of length 15.</p> <p>[23:20]: Tab1 code words of length 14.</p> <p>[19:16]: Tab1 code words of length 13.</p> <p>[15:12]: Tab1 code words of length 12.</p> <p>[11:8]: Tab1 code words of length 11.</p> <p>[6:4]: Tab1 code words of length 10.</p> <p>[1:0]: Tab1 code words of length 9.</p> <p>VP6:</p> <p>[29:24]: 26st coef of scan read index.</p> <p>[23:18]: 27st coef of scan read index.</p> <p>[17:12]: 28st coef of scan read index.</p> <p>[11:6]: 29st coef of scan read index.</p> <p>[5:0]: 30st coef of scan read index.</p> <p>VP7:</p> <p>[31:2]: DCT stream MB row 2, 2n+3 start address.</p>

**VDPU\_Swreg143**

Address: Operational Base + offset (0x0023c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg23</p> <p>Multi format reuse register23 except h264.</p> <p>JPEG:</p> <p>[31:28]: Tab2 code words of length 8.</p> <p>[27:24]: Tab2 code words of length 7.</p> <p>[23:20]: Tab2 code words of length 6.</p> <p>[19:16]: Tab2 code words of length 5.</p> <p>[15:12]: Tab2 code words of length 4.</p> <p>[11:8]: Tab2 code words of length 3.</p> <p>[6:4]: Tab2 code words of length 2.</p> <p>[1:0]: Tab2 code words of length 1.</p> <p>VP6:</p> <p>[29:24]: 31st coef of scan read index.</p> <p>[23:18]: 32st coef of scan read index.</p> <p>[17:12]: 33st coef of scan read index.</p> <p>[11:6]: 34st coef of scan read index.</p> <p>[5:0]: 35st coef of scan read index.</p> <p>VP7:</p> <p>[31:2]: DCT stream MB row 2, 2n+4 start address.</p>

**VDPU\_Swreg144**

Address: Operational Base + offset (0x00240)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>Mfr_reg24</p> <p>Multi format reuse register24 except h264.</p> <p>JPEG:</p> <p>[31:28]: Tab2 code words of length 16.</p> <p>[27:24]: Tab2 code words of length 15.</p> <p>[23:20]: Tab2 code words of length 14.</p> <p>[19:16]: Tab2 code words of length 13.</p> <p>[15:12]: Tab2 code words of length 12.</p> <p>[11:8]: Tab2 code words of length 11.</p> <p>[6:4]: Tab2 code words of length 10.</p> <p>[1:0]: Tab2 code words of length 9.</p> <p>VP6:</p> <p>[29:24]: 36st coef of scan read index.</p> <p>[23:18]: 37st coef of scan read index.</p> <p>[17:12]: 38st coef of scan read index.</p> <p>[11:6]: 39st coef of scan read index.</p> <p>[5:0]: 40st coef of scan read index.</p> <p>VP7:</p> <p>[31:2]: DCT stream MB row 2, 2n+5 start address.</p>

**VDPU\_Swreg145**

Address: Operational Base + offset (0x00244)



Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg25 Multi format reuse register25 except h264. JPEG: [31:28]: Tab3 code words of length 8. [27:24]: Tab3 code words of length 7. [23:20]: Tab3 code words of length 6. [19:16]: Tab3 code words of length 5. [15:12]: Tab3 code words of length 4. [11:8]: Tab3 code words of length 3. [6:4]: Tab3 code words of length 2. [1:0]: Tab3 code words of length 1. VC-1: [31:2]: Bitplane mb ctrl start address. VP6/VP7: [31:2]: Ctrl data stream start address.

**VDPU\_Swreg146**

Address: Operational Base + offset (0x00248)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg26 Multi format reuse register26 except h264. JPEG: [31:28]: Tab3 code words of length 16. [27:24]: Tab3 code words of length 15. [23:20]: Tab3 code words of length 14. [19:16]: Tab3 code words of length 13. [15:12]: Tab3 code words of length 12. [11:8]: Tab3 code words of length 11. [6:4]: Tab3 code words of length 10. [1:0]: Tab3 code words of length 9. VP6: [29:24]: 41st coef of scan read index. [23:18]: 42st coef of scan read index. [17:12]: 43st coef of scan read index [11:6]: 44st coef of scan read index. [5:0]: 45st coef of scan read index. VP7: [31:2]: DCT stream MB row 2, 2n+6 start address.

**VDPU\_Swreg147**

Address: Operational Base + offset (0x0024c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg27 Multi format reuse register27 except h264. VP6: [29:24]: 46st coef of scan read index. [23:18]: 47st coef of scan read index. [17:12]: 48st coef of scan read index. [11:6]: 49st coef of scan read index. [5:0]: 50st coef of scan read index. VP7: [31:2]: DCT stream MB row 2, 2n+7 start address.

**VDPU\_Swreg148**

Address: Operational Base + offset (0x00250)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg28 Multi format reuse register28 except h264. MPEG4/VC-1/MPEG2/VP7: [31:2]: Ref pic index 1 start address. JPEG: [7:0]: Snapshot.

**VDPU\_Swreg149**

Address: Operational Base + offset (0x00254)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg29 Multi format reuse register29 except h264. VC-1: [24]: Enable for intensity compensation 1. [23:16]: Intensity compensation iscale value. [15:0]: Intensity compensation ishift value. VP7: [31:2]: The segmentation map value start address. [1]: Enable for segmentation map update. [0]: Enable for segmentation.

**VDPU\_Swreg150**

Address: Operational Base + offset (0x00258)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg30 Multi format reuse register30 except h264. VC-1: [24]: Enable for intensity compensation 2. [23:16]: Intensity compensation iscale value. [15:0]: Intensity compensation ishift value. VP7: [29:24]: DCT stream partition index 3 of start bit. [23:18]: DCT stream partition index 4 of start bit. [17:12]: DCT stream partition index 5 of start bit. [11:6]: DCT stream partition index 6 of start bit. [5:0]: DCT stream partition index 7 of start bit.

**VDPU\_Swreg151**

Address: Operational Base + offset (0x0025c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg31 Multi format reuse register31 except h264. VP7: [21:11]: QP2 for VP7. [10:0]: QP3 for VP7.

**VDPU\_Swreg152**

Address: Operational Base + offset (0x00260)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg32 Multi format reuse register32 except h264. VP7: [21:11]: QP4 for VP7. [10:0]: QP5 for VP7.

**VDPU\_Swreg153**

Address: Operational Base + offset (0x00264)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg33 Multi format reuse register33 except h264. VC-1/VP6/VP7: [31:22]: Prediction filter with set 0, tap3 (also for mpeg4). [21:12]: Prediction filter with set 1, tap0. [11:2]: Prediction filter with set 1, tap1.

**VDPU\_Swreg154**

Address: Operational Base + offset (0x00268)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg34 Multi format reuse register34 except h264. VC-1/VP6/VP7: [31:22]: Prediction filter with set 1, tap2. [21:12]: Prediction filter with set 1, tap3. [11:2]: Prediction filter with set 2, tap0(no for vc-1).

**VDPU\_Swreg155**

Address: Operational Base + offset (0x0026c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg35 Multi format reuse register35 except h264. VC-1/VP6/VP7: [31:22]: Prediction filter with set 2, tap1. [21:12]: Prediction filter with set 2, tap2. [11:2]: Prediction filter with set 2, tap3.

**VDPU\_Swreg156**

Address: Operational Base + offset (0x00270)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg36 Multi format reuse register36 except h264. VP6/VP7: [31:22]: Prediction filter with set 3, tap0. [21:12]: Prediction filter with set 3, tap1. [11:2]: Prediction filter with set 3, tap2.

**VDPU\_Swreg157**

Address: Operational Base + offset (0x00274)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg37 Multi format reuse register37 except h264. VP6/VP7: [31:22]: Prediction filter with set 3, tap3. [21:12]: Prediction filter with set 4, tap0. [11:2]: Prediction filter with set 4, tap1.

**VDPU\_Swreg158**

Address: Operational Base + offset (0x00278)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mfr_reg38 Multi format reuse register38 except h264. VP6/VP7: [31:22]: Prediction filter with set 4, tap2. [21:12]: Prediction filter with set 4, tap3. [11:2]: Prediction filter with set 5, tap0.

**VDPU\_Swreg164\_perf\_latency\_ctrl0**

Address: Operational Base + offset (0x00290)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	Sw_rd_latency_thr Sw_rd_latency_thr
7:4	RW	0x0	Sw_rd_latency_id Sw_rd_latency_id
3	RW	0x0	Sw_axi_cnt_type Sw_axi_cnt_type
2	RW	0x0	Sw_axi_perf_frm_type 1'b0: Clear by frame end. 1'b1: Clear by software configuration.
1	W1C	0x0	Sw_axi_perf_clr_e 1'b0: Software clear disable. 1'b1: Software clear enable.
0	RW	0x0	Sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

**VDPU\_Swreg165\_perf\_latency\_ctrl1**

Address: Operational Base + offset (0x00294)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	Sw_aw_count_id Sw_aw_count_id
7:4	RW	0x0	Sw_ar_count_id Sw_ar_count_id
3	RW	0x0	Sw_aw_cnt_id_type Sw_aw_cnt_id_type
2	RW	0x0	Sw_ar_cnt_id_type Sw_ar_cnt_id_type
1:0	RW	0x0	Sw_addr_align_type Sw_addr_align_type

**VDPU\_Swreg166\_perf\_rd\_max\_latency\_num0**

Address: Operational Base + offset (0x00298)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Rd_max_latency_num_ch0 Read max latency value of channel 0.

**VDPU\_Swreg167\_perf\_rd\_latency\_samp\_num**

Address: Operational Base + offset (0x0029c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Rd_latency_thr_num_ch0 The number of bigger than configed threshold value.

**VDPU\_Swreg168\_perf\_rd\_latency\_acc\_num**

Address: Operational Base + offset (0x002a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Rd_latency_acc_sum

**VDPU\_Swreg169\_perf\_rd\_axi\_total\_byte**

Address: Operational Base + offset (0x002a4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Perf_rd_axi_total_byte Perf_rd_axi_total_byte

**VDPU\_Swreg170\_perf\_wr\_axi\_total\_byte**

Address: Operational Base + offset (0x002a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Perf_wr_axi_total_byte Perf_wr_axi_total_byte

**VDPU\_Swreg171\_perf\_working\_cnt**

Address: Operational Base + offset (0x002ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Perf_working_cnt Perf_working_cnt

**13.6.6 VPU121 MMU Registers Summary**

Name	Offset	Size	Reset Value	Description
<u>VCODEC_MMU_DTE_ADDR</u>	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state
<u>VCODEC_MMU_STATUS</u>	0x0004	W	0x00000018	MMU status register
<u>VCODEC_MMU_COMMAND</u>	0x0008	W	0x00000000	MMU command register

Name	Offset	Size	Reset Value	Description
<u>VCODEC MMU PAGE FAULT ADDR</u>	0x000c	W	0x00000000	MMU logical address of last page fault
<u>VCODEC MMU ZAP ONE LINE</u>	0x0010	W	0x00000000	MMU Zap cache line register
<u>VCODEC MMU INT RAWSTATUS</u>	0x0014	W	0x00000000	MMU raw interrupt status register
<u>VCODEC MMU INT CLEAR</u>	0x0018	W	0x00000000	MMU raw interrupt status register
<u>VCODEC MMU INT MASK</u>	0x001c	W	0x00000000	MMU raw interrupt status register
<u>VCODEC MMU INT STATUS</u>	0x0020	W	0x00000000	MMU raw interrupt status register
<u>VCODEC MMU AUTO GATING</u>	0x0024	W	0x00000001	mmu auto gating

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.7 VPU121 MMU Detail Registers Description

#### VCODEC MMU DTE ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU current page Table address

#### VCODEC MMU STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x00000000	Reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY 1'b1: The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command. 1'b1: Page fault is active
0	RO	0x0	PAGING_ENABLED 1'b0: Paging is disabled 1'b1: Paging is enabled

#### VCODEC MMU COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	Reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET

**VCODEC MMU PAGE FAULT ADDR**

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

**VCODEC MMU ZAP ONE LINE**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Address to be invalidated from the page table cache

**VCODEC MMU INT RAWSTAT**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error status
0	RW	0x0	PAGE_FAULT Page fault status

**VCODEC MMU INT CLEAR**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	WO	0x0	READ_BUS_ERROR Write 1 to clear read bus error
0	WO	0x0	PAGE_FAULT Write 1 to page fault clear

**VCODEC MMU INT MASK**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Enable the read bus interrupt source when this bit is set to 1'b1
0	RW	0x0	PAGE_FAULT Enable the page fault interrupt source when this bit is set to 1'b1

**VCODEC MMU INT STATUS**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved



Bit	Attr	Reset Value	Description
1	RO	0x0	READ_BUS_ERROR 1'b1: Read bus error status
0	RO	0x0	PAGE_FAULT 1'b1: Page fault

**VCODEC\_MMU\_AUTO\_GATING**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x1	Mmu_auto_clkgating When it is 1'b1, the mmu will auto gating it self

**13.6.8 VDP345 Registers Summary**

Name	Offset	Size	Reset Value	Description
<u>rkvdec_swreg0_id</u>	0x0000	W	0x00000000	ID register (read only)
<u>rkvdec_swreg1_int</u>	0x0004	W	0x00000022	Interrupt and enable register
<u>rkvdec_swreg2_sysctrl</u>	0x0008	W	0x00000000	Data input and output endian setting and sys ctrl
<u>rkvdec_swreg3_picpar</u>	0x000c	W	0x00000000	Picture parameters
<u>rkvdec_swreg4_strm_rlc_base</u>	0x0010	W	0x00000000	The stream or rlc read data base address
<u>rkvdec_swreg5_stream_rlc_len</u>	0x0014	W	0x00000000	Amount of stream bytes in the input buffer or amount to rlc bytes in the input buffer
<u>rkvdec_swreg6_cabactbl_prob_base</u>	0x0018	W	0x00000000	Hevc & h264: The base address of cabac tablevp9: The base address of prob
<u>rkvdec_swreg7_decout_base</u>	0x001c	W	0x00000000	Base address of decoder output picture, suggest this register to config to even for advance ddr performance
<u>rkvdec_swreg8_y_virstride</u>	0x0020	W	0x00000000	The output picture y fac virtual stride, suggest this register to config to even for advance ddr performance
<u>rkvdec_swreg8_fbc_payload_st_offset</u>	0x0020	W	0x00000000	
<u>rkvdec_swreg9_yuv_virstride</u>	0x0024	W	0x00000000	The output picture yuv virtual stride

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg10 hevc refer0 base</u>	0x0028	W	0x00000000	Base address for reference picture index 0 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg10 h264 refer0 base</u>	0x0028	W	0x00000000	Base address for reference picture index 0, suggest this register to config to even for advance ddr performance
<u>rkvdec swreg10 avs2 refer0 base</u>	0x0028	W	0x00000000	Base address for reference picture index 0, suggest this register to config to even for advance ddr performance
<u>rkvdec swreg10 vp9 cprheader_offset</u>	0x0028	W	0x00000000	Vp9 compressed header offset, 2014.11.19 del this register, because we can decode out sw_vp9_cprheader_offset from the stream
<u>rkvdec swreg11 h264 refer1 base</u>	0x002c	W	0x00000000	Base address for reference picture index 1 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg11 vp9 referlast base</u>	0x002c	W	0x00000000	B=Base address for reference pictures suggest this register to config to even for advance ddr performance
<u>rkvdec swreg11 avs2 refer1 base</u>	0x002c	W	0x00000000	Base address for reference picture index 1
<u>rkvdec swreg11 hevc refer1 base</u>	0x002c	W	0x00000000	Base address for reference picture index 1
<u>rkvdec swreg12 vp9 refergolden base</u>	0x0030	W	0x00000000	Base address for golden pictures suggest this register to config to even for advance ddr performance
<u>rkvdec swreg12 hevc refer2 base</u>	0x0030	W	0x00000000	Base address for reference picture index 2
<u>rkvdec swreg12 avs2 refer2 base</u>	0x0030	W	0x00000000	Base address for reference picture index 2

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg12 h264 refer2 base</u>	0x0030	W	0x00000000	Base address for reference picture index 2 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg13 hevc refer3 base</u>	0x0034	W	0x00000000	Base address for reference picture index 3
<u>rkvdec swreg13 h264 refer3 base</u>	0x0034	W	0x00000000	Base address for reference picture index 3 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg13 avs2 refer3 base</u>	0x0034	W	0x00000000	Base address for reference picture index 3
<u>rkvdec swreg13 vp9 referalfter base</u>	0x0034	W	0x00000000	Base address for alter pictures suggest this register to config to even for advance ddr performance
<u>rkvdec swreg14 h264 refer4 base</u>	0x0038	W	0x00000000	Base address for reference picture index 4 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg14 vp9count base</u>	0x0038	W	0x00000000	Vp9 count base addr
<u>rkvdec swreg14 avs2 refer4 base</u>	0x0038	W	0x00000000	Base address for reference picture index 4
<u>rkvdec swreg14 hevc refer4 base</u>	0x0038	W	0x00000000	Base address for reference picture index 4
<u>rkvdec swreg15 hevc refer5 base</u>	0x003c	W	0x00000000	Base address for reference picture index 5
<u>rkvdec swreg15 h264 refer5 base</u>	0x003c	W	0x00000000	Base address for reference picture index 5 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg15 avs2 refer5 base</u>	0x003c	W	0x00000000	Base address for reference picture index 5
<u>rkvdec swreg15 vp9 segidlast base</u>	0x003c	W	0x00000000	Base address for last frame segment id

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg16 h264 refer6 base</u>	0x0040	W	0x00000000	Base address for reference picture index 6suggest this register to config to even for advance ddr performance
<u>rkvdec swreg16 vp9 segidcur base</u>	0x0040	W	0x00000000	Base address for cur frame segment id
<u>rkvdec swreg16 avs2 refer6 base</u>	0x0040	W	0x00000000	Base address for reference picture index 6
<u>rkvdec swreg16 hevc refer6 base</u>	0x0040	W	0x00000000	Base address for reference picture index 6
<u>rkvdec swreg17 vp9 frame size last</u>	0x0044	W	0x00000000	Vp9 last frame size
<u>rkvdec swreg17 hevc refer7 base</u>	0x0044	W	0x00000000	Base address for reference picture index 7
<u>rkvdec swreg17 avs2 refer7 base</u>	0x0044	W	0x00000000	Base address for reference picture index 7
<u>rkvdec swreg17 h264 refer7 base</u>	0x0044	W	0x00000000	Base address for reference picture index 7suggest this register to config to even for advance ddr performance
<u>rkvdec swreg18 hevc refer8 base</u>	0x0048	W	0x00000000	Base address for reference picture index 8
<u>rkvdec swreg18 h264 refer8 base</u>	0x0048	W	0x00000000	Base address for reference picture index 8suggest this register to config to even for advance ddr performance
<u>rkvdec swreg18 vp9 frame size golden</u>	0x0048	W	0x00000000	Vp9 golden frame size
<u>rkvdec swreg19 hevc refer9 base</u>	0x004c	W	0x00000000	Base address for reference picture index 9
<u>rkvdec swreg19 h264 refer9 base</u>	0x004c	W	0x00000000	Base address for reference picture index 9suggest this register to config to even for advance ddr performance
<u>rkvdec swreg19 vp9 frame size altref</u>	0x004c	W	0x00000000	Vp9 alfter frame size
<u>rkvdec swreg20 hevc refer10 base</u>	0x0050	W	0x00000000	Base address for reference picture index 10

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg20 h264 refer10_base</u>	0x0050	W	0x00000000	Base address for reference picture index 10 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg20 vp9 segid grp0</u>	0x0050	W	0x00000000	vp9 segid syntax grp0 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg21 hevc refer11_base</u>	0x0054	W	0x00000000	Base address for reference picture index 11
<u>rkvdec swreg21 h264 refer11_base</u>	0x0054	W	0x00000000	Base address for reference picture index 11 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg21 vp9 segid grp1</u>	0x0054	W	0x00000000	Vp9 segid syntax grp1 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg22 hevc refer12_base</u>	0x0058	W	0x00000000	Base address for reference picture index 12
<u>rkvdec swreg22 h264 refer12_base</u>	0x0058	W	0x00000000	Base address for reference picture index 12 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg22 vp9 segid grp2</u>	0x0058	W	0x00000000	Vp9 segid syntax grp2 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg23 hevc refer13_base</u>	0x005c	W	0x00000000	Base address for reference picture index 13
<u>rkvdec swreg23 h264 refer13_base</u>	0x005c	W	0x00000000	Base address for reference picture index 13 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg23 vp9 segid grp3</u>	0x005c	W	0x00000000	Vp9 segid syntax grp3 when write it is for last frame when read it is for cur frame

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg24 hevc refer14_base</u>	0x0060	W	0x00000000	Base address for reference picture index 14
<u>rkvdec swreg24 h264 refer14_base</u>	0x0060	W	0x00000000	Base address for reference picture index 14 suggest this register to config to even for advance ddr performance
<u>rkvdec swreg24 vp9 segid grp4</u>	0x0060	W	0x00000000	Vp9 segid syntax grp4 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg25 vp9 segid grp5</u>	0x0064	W	0x00000000	Vp9 segid syntax grp5 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg25 refer0_poc</u>	0x0064	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 0
<u>rkvdec swreg26 vp9 segid grp6</u>	0x0068	W	0x00000000	Vp9 segid syntax grp6 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg26 refer1_poc</u>	0x0068	W	0x00000000	hevc & h264 & avs2: The poc of reference picture index 1
<u>rkvdec swreg27 vp9 segid grp7</u>	0x006c	W	0x00000000	vp9 segid syntax grp7 when write it is for last frame when read it is for cur frame
<u>rkvdec swreg27 refer2_poc</u>	0x006c	W	0x00000000	hevc & h264 & avs2: the poc of reference picture index 2
<u>rkvdec swreg28 vp9 cprheader_config</u>	0x0070	W	0x00000000	vp9 compressed header config info
<u>rkvdec swreg28 refer3_poc</u>	0x0070	W	0x00000000	hevc & h264 & avs2: The poc of reference picture index 3
<u>rkvdec swreg29 vp9 lref_scale</u>	0x0074	W	0x00000000	vp9 scaling factor for last reference picture
<u>rkvdec swreg29 refer4_poc</u>	0x0074	W	0x00000000	hevc & h264 & avs2: The poc of reference picture index 4
<u>rkvdec swreg30 vp9 gref_scale</u>	0x0078	W	0x00000000	vp9 scaling factor for golden reference picture
<u>rkvdec swreg30 refer5_poc</u>	0x0078	W	0x00000000	hevc & h264 & avs2: The poc of reference picture index 5

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg31 vp9 aref scale</u>	0x007c	W	0x00000000	vp9 scaling factor for alfter reference picture
<u>rkvdec swreg31 refer6_poc</u>	0x007c	W	0x00000000	hevc & h264 & avs2:the poc of reference picture index 6
<u>rkvdec swreg32 vp9 ref deltas lastframe</u>	0x0080	W	0x00000000	vp9 ref deltas
<u>rkvdec swreg32 refer7_poc</u>	0x0080	W	0x00000000	hevc & h264 & avs2: The poc of reference picture index 7
<u>rkvdec swreg33 vp9 info last frame</u>	0x0084	W	0x00000000	vp9 info for last frame
<u>rkvdec swreg33 refer8_poc</u>	0x0084	W	0x00000000	hevc & h264: The poc of reference picture index 8
<u>rkvdec swreg34 vp9 intercmd base</u>	0x0088	W	0x00000000	inter cmd base addr
<u>rkvdec swreg34 refer9_poc</u>	0x0088	W	0x00000000	hevc & h264 :the poc of reference picture index 9
<u>rkvdec swreg35 vp9 intercmd num</u>	0x008c	W	0x00000000	vp9 intercmd num
<u>rkvdec swreg35 refer10_poc</u>	0x008c	W	0x00000000	hevc & h264: The poc of reference picture index 10
<u>rkvdec swreg36 vp9 lasttile size</u>	0x0090	W	0x00000000	vp9 last tile size
<u>rkvdec swreg36 refer11_poc</u>	0x0090	W	0x00000000	hevc & h264: The poc of reference picture index 11
<u>rkvdec swreg37 vp9 lastf hor_virstride</u>	0x0094	W	0x00000000	Register0000 Description
<u>rkvdec swreg37 refer12_poc</u>	0x0094	W	0x00000000	hevc & h264: The poc of reference picture index 12
<u>rkvdec swreg38 vp9 goldenf hor_virstride</u>	0x0098	W	0x00000000	vp9 golden frame horizontal virstride
<u>rkvdec swreg38 refer13_poc</u>	0x0098	W	0x00000000	hevc & h264: The poc of reference picture index 13
<u>rkvdec swreg39 vp9 altreff hor_virstride</u>	0x009c	W	0x00000000	vp9 altref frame horizontal virstride
<u>rkvdec swreg39 refer14_poc</u>	0x009c	W	0x00000000	hevc & h264: The poc of reference picture index 14
<u>rkvdec swreg40 cur_poc</u>	0x00a0	W	0x00000000	hevc & h264 & avs2 :the poc of cur picture
<u>rkvdec swreg41 colbuf_base</u>	0x00a4	W	0x00000000	128bit align

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg41 rlcwrite base</u>	0x00a4	W	0x00000000	the base address of rlc write base address when frame is ready , it is the address of the end of rlc write address
<u>rkvdec swreg42 vp9 last prob base</u>	0x00a8	W	0x00000000	it only used when hardware parse prob this base addr is for last prob
<u>rkvdec swreg42 avs2 head base</u>	0x00a8	W	0x00000000	the base address of avs2 head
<u>rkvdec swreg42 pps base</u>	0x00a8	W	0x00000000	the base address of pps
<u>rkvdec swreg43 avs2 head len</u>	0x00ac	W	0x00000000	the base address of rps
<u>rkvdec swreg43 rps base</u>	0x00ac	W	0x00000000	the base address of rps
<u>rkvdec swreg44 strmd error en</u>	0x00b0	W	0x00000000	cabac error enable config
<u>rkvdec swreg45 vp9 error info0</u>	0x00b4	W	0x00000000	vp9 error info 0now is for no use
<u>rkvdec swreg45 strmd error status</u>	0x00b4	W	0x00000000	cabac error status
<u>rkvdec swreg46 strmd error ctu</u>	0x00b8	W	0x00400000	strmd error ctu
<u>rkvdec swreg47 sao ctu position</u>	0x00bc	W	0x00000000	when there is any error, it is for the position of sao decode output to busifd
<u>rkvdec swreg48 vp9 last ystride</u>	0x00c0	W	0x00000000	last ref y stride
<u>rkvdec swreg48 h264 refer15 base</u>	0x00c0	W	0x00000000	h264: Base address for reference picture index 15suggest this register to config to even for advance ddr performance hevc & vp9: now is for no use
<u>rkvdec swreg49 vp9 golden y stride</u>	0x00c4	W	0x00000000	vp9 golden y stride
<u>rkvdec swreg49 h26x refer15 poc</u>	0x00c4	W	0x00000000	h264: The poc of reference picture index 15hevc : used for mvcvp9: now is no use
<u>rkvdec swreg50 vp9 altrefy y stride</u>	0x00c8	W	0x00000000	altref ref y stride
<u>rkvdec swreg50 h264 refer16 poc</u>	0x00c8	W	0x00000000	h264: The poc of reference picture index 16hevc & vp9: now is no use
<u>rkvdec swreg51 vp9 lastref y uvstride</u>	0x00cc	W	0x00000000	last ref yuv stride



Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg51 h264 refer17_poc</u>	0x00cc	W	0x00000000	h264: The poc of reference picture index 17hevc & vp9: now is no use
<u>rkvdec swreg52 h264 refer18_poc</u>	0x00d0	W	0x00000000	h264: The poc of reference picture index 18hevc & vp9: now is no use
<u>rkvdec swreg52 vp9 refcolmv_base</u>	0x00d0	W	0x00000000	vp9 refcolmv base addr
<u>rkvdec swreg53 h264 refer19_poc</u>	0x00d4	W	0x00000000	h264: The poc of reference picture index 19hevc & vp9: now is no use
<u>rkvdec swreg54 h264 refer20_poc</u>	0x00d8	W	0x00000000	h264: The poc of reference picture index 20hevc & vp9: now is no use
<u>rkvdec swreg55 h264 refer21_poc</u>	0x00dc	W	0x00000000	h264: The poc of reference picture index 21hevc & vp9: now is no use
<u>rkvdec swreg56 h264 refer22_poc</u>	0x00e0	W	0x00000000	h264: The poc of reference picture index 22hevc & vp9: now is no use
<u>rkvdec swreg57 h264 refer23_poc</u>	0x00e4	W	0x00000000	h264: The poc of reference picture index 23hevc & vp9: now is no use
<u>rkvdec swreg58 h264 refer24_poc</u>	0x00e8	W	0x00000000	h264: The poc of reference picture index 24hevc & vp9: now is no use
<u>rkvdec swreg59 h264 refer25_poc</u>	0x00ec	W	0x00000000	h264: The poc of reference picture index 25hevc & vp9: now is no use
<u>rkvdec swreg60 h264 refer26_poc</u>	0x00f0	W	0x00000000	h264: The poc of reference picture index 26hevc & vp9: now is no use
<u>rkvdec swreg61 h264 refer27_poc</u>	0x00f4	W	0x00000000	h264: The poc of reference picture index 27hevc & vp9: now is no use
<u>rkvdec swreg62 h264 refer28_poc</u>	0x00f8	W	0x00000000	h264: The poc of reference picture index 28hevc & vp9: now is no use
<u>rkvdec swreg63 h264 refer29_poc</u>	0x00fc	W	0x00000000	h264: The poc of reference picture index 29hevc & vp9: now is no use

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg64 hevc mvc0</u>	0x0100	W	0x00000000	Hevc mvc config register
<u>rkvdec swreg64 avs2 ctrl extra</u>	0x0100	W	0x00000000	Avs2 ctrl register
<u>rkvdec swreg64 vp9 prob</u>	0x0100	W	0x00000000	VP9 prob ctrl register
<u>rkvdec swreg65 hevc mvc1</u>	0x0104	W	0x00000000	Hevc MVC ctrl register
<u>rkvdec swreg66 error ref base</u>	0x0108	W	0x00000000	Error reference frame base address
<u>rkvdec swreg66 avs2 error ref base</u>	0x0108	W	0x00000000	Avs2 error reference frame base address
<u>rkvdec swreg67 error info</u>	0x010c	W	0x00000001	Error infomation
<u>rkvdec swreg68 performance sel</u>	0x0110	W	0x00000000	Performance montor ctrl
<u>rkvdec swreg69 performance cnt0</u>	0x0114	W	0x00000000	Performance count value0
<u>rkvdec swreg70 performance cnt1</u>	0x0118	W	0x00000000	Performance count value1
<u>rkvdec swreg71 performance cnt2</u>	0x011c	W	0x00000000	Performance count value2
<u>rkvdec swreg72 h264 refer30_poc</u>	0x0120	W	0x00000000	h264: The poc of reference picture index 30hevc & vp9: now is no use
<u>rkvdec swreg73 h264 refer31_poc</u>	0x0124	W	0x00000000	h264: The poc of reference picture index 31hevc & vp9: now is no use
<u>rkvdec swreg74 h264 cur poc1</u>	0x0128	W	0x00000000	when cur is field, h264 cur poc for bottom field
<u>rkvdec swreg75 h26x errorinfo base</u>	0x012c	W	0x00000000	h264/h265: error info base addrvp9: now is no use
<u>rkvdec swreg75 vp9 error info1</u>	0x012c	W	0x00000000	vp9 error info1now is for no use
<u>rkvdec swreg76 h26x errorinfo num</u>	0x0130	W	0x00000000	h264 error info num
<u>rkvdec swreg76 vp9 error ctu1</u>	0x0130	W	0x00000000	vp9 error ctu1, now is for no use
<u>rkvdec swreg77 h264 error enable</u>	0x0134	W	0x00000000	h264 error enable high bits
<u>rkvdec swreg78 colmv cur base</u>	0x0138	W	0x00000000	cur frame colmv output addr
<u>rkvdec swreg79 colmv ref0 base</u>	0x013c	W	0x00000000	ref0 frame colmv base addr
<u>rkvdec swreg80 colmv ref1 base</u>	0x0140	W	0x00000000	ref1 frame colmv base addr

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg81 colmv ref2 base</u>	0x0144	W	0x00000000	ref2 frame colmv base addr
<u>rkvdec swreg82 colmv ref3 base</u>	0x0148	W	0x00000000	ref3 frame colmv base addr
<u>rkvdec swreg83 colmv ref4 base</u>	0x014c	W	0x00000000	ref4 frame colmv base addr
<u>rkvdec swreg84 colmv ref5 base</u>	0x0150	W	0x00000000	ref5 frame colmv base addr
<u>rkvdec swreg85 colmv ref6 base</u>	0x0154	W	0x00000000	ref6 frame colmv base addr
<u>rkvdec swreg86 colmv ref7 base</u>	0x0158	W	0x00000000	ref7 frame colmv base addr
<u>rkvdec swreg87 colmv ref8 base</u>	0x015c	W	0x00000000	ref8 frame colmv base addr
<u>rkvdec swreg88 colmv ref9 base</u>	0x0160	W	0x00000000	ref9 frame colmv base addr
<u>rkvdec swreg89 colmv ref10 base</u>	0x0164	W	0x00000000	ref10 frame colmv base addr
<u>rkvdec swreg90 colmv ref11 base</u>	0x0168	W	0x00000000	ref11 frame colmv base addr
<u>rkvdec swreg91 colmv ref12 base</u>	0x016c	W	0x00000000	ref12 frame colmv base addr
<u>rkvdec swreg92 colmv ref13 base</u>	0x0170	W	0x00000000	ref13 frame colmv base addr
<u>rkvdec swreg93 colmv ref14 base</u>	0x0174	W	0x00000000	ref14 frame colmv base addr
<u>rkvdec swreg94 colmv ref15 base</u>	0x0178	W	0x00000000	ref15 frame colmv base addr
<u>rkvdec swreg95 scanlist addr</u>	0x017c	W	0x00000000	scanlist addr
<u>rkvdec swreg96 sd decout base</u>	0x0180	W	0x00000000	base address of decoder output picturesuggest this register to config to even for advance ddr performance
<u>rkvdec swreg97 sd y virstride</u>	0x0184	W	0x00000000	the output picture y fac virtual stridesuggest this register to config to even for advance ddr performance
<u>rkvdec swreg98 sd hor stride</u>	0x0188	W	0x00000000	picture parameters
<u>rkvdec swreg99 qos ctrl</u>	0x018c	W	0x00000000	AXI bus hurry ctrl
<u>rkvdec swreg100 PERF LATENCY CTRL0</u>	0x0190	W	0x00000000	Axi performance latency module contrl register
<u>rkvdec swreg101 PERF LATENCY CTRL1</u>	0x0194	W	0x00000000	PERF_LATENCY_CTRL1
<u>rkvdec swreg102 PERF RD MAX LATENCY NUM0</u>	0x0198	W	0x00000000	Read max latency number
<u>rkvdec swreg103 PERF RD LATENCY SAMP NUM</u>	0x019c	W	0x00000000	The number of bigger than configed threshold value

Name	Offset	Size	Reset Value	Description
<u>rkvdec swreg104 PERF RD LATENCY ACC SUM</u>	0x01a0	W	0x00000000	Total sample number
<u>rkvdec swreg105 PERF RD AXI TOTAL BYTE</u>	0x01a4	W	0x00000000	perf_rd_axi_total_byte
<u>rkvdec swreg106 PERF WR AXI TOTAL BYTE</u>	0x01a8	W	0x00000000	perf_wr_axi_total_byte
<u>rkvdec swreg107 PERF WORKING CNT</u>	0x01ac	W	0x00000000	perf_working_cnt
<u>rkvdec swreg108 qos1</u>	0x01b0	W	0x00000000	perf_working_cnt
<u>rkvdec swreg112 sysctrl extra0</u>	0x01c0	W	0x00000000	the output picture y fac virtual stridesuggest this register to config to even for advance ddr performance
<u>rkvdec swreg116 sw roi ctu offset st</u>	0x01d0	W	0x00000000	it will cal the error ctu num in the roiit will include the st ctu and end ctu
<u>rkvdec swreg117 sw roi ctu offset end</u>	0x01d4	W	0x00000000	it will cal the error ctu num in the roiit will include the st ctu and end ctu
<u>rkvdec swreg118 sw error ctu ctu num in roi</u>	0x01d8	W	0x00000000	the error ctu num in roi
<u>rkvdec swregff verison</u>	0x03fc	W	0x00000000	IP version

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.9 VDP345 Detail Registers Description

#### rkvdec swreg0 id

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Prod_num prod code
15:8	RW	0x00	Major_ver Major version
7:0	RW	0x00	Minor_ver Minor version

#### rkvdec swreg1 int

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_error_mode For VP9: 1'b0: When there is any stream error, the hardware will stop the decode and reset itself. 1'b1: When there is any stream error, the hardware will still decode the next slice. it is recommend that when vp9, it is configed to 1'b0. for H264/hevc/avs2: 1'b0: When there is any stream error, the hardware will stop the decoder and reset itself. 1'b1: When there is any stream error, the hardware will wait the end signal of deblocking and then reset request.

Bit	Attr	Reset Value	Description
30	RW	0x0	Sw_colmv_compress_en 1'b0: Disable 1'b1: Enable
29	RW	0x0	Sw_allow_16x8_cp_flag 1'b0: Not allow 1'b1: Allow The config value is depend on vop work mode
28	RW	0x0	Sw_fbc_e 1'b0: Disable 1'b1: Fbc enable
27	RW	0x0	Sw_colmv_error_mode 1'b0: When there is any colmv error, the hardware will stop the decoder and reset itself 1'b1: When there is any colmv error, the hardware will wait the end signal of deblocking and then reset itself
26	RO	0x0	bus_on_idle_flag 1'b0: Bus busy 1'b1: Bus idle
25	RW	0x0	Sw_allow_not_wr_unref_bframe 1'b1: If dec not reference b frame, will not write to ddr, if wan't to set this bit to 1, should set Sw_scl_down_en=1 also, it only used in hevc and not support tile mode.
24	RW	0x0	Sw_scl_down_en 1'b1: Enable 2ratio scaler down enable, it only used in hevc and not support tile mode.
23	RW	0x0	Sw_wr_ddr_align_en 1'b1: Set to 1 only when hevc mode decoder.
22	RW	0x0	Sw_softreset_rdy When it is 1'b1, it says that softreset has been done.
21	RW	0x0	Sw_force_softreset_valid When Sw_force_softreset_valid is 1'b1, Sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle; when Sw_force_softreset_valid is 1'b0, Sw_softrst_en will only be valid when the axi bus is idle.
20	RW	0x0	Sw_softrst_en_p Softreset enable signal Write 1 to soft reset, write 0 invalid pulse register.
19	RW	0x0	Sw_h264orvp9_cabac_error_mode 1'b0: When there is any stream error, the stream will stop the decoder and reset itself. 1'b1: When there is any stream error, the stream will try to decode next slice.
18	RW	0x0	Sw_cabu_end_sta Hevc: Cabac decode end status H264& vp9 : Stream decode status
17	RW	0x0	Sw_colmv_ref_error_sta Colmv ref error status Hevc&vp9: When it is 1'b1, it means that inter module read the invalid dpb frame. It will self reset the hardware. H264: When it is 1'b1, it means that inter module read the invalid dpb frame. When Sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not.

Bit	Attr	Reset Value	Description
16	RW	0x0	Sw_buf_empty_sta Buffer empty status, only when Sw_buf_empty_en is 1'b1, this bit is valid, now is for no valid.
15	RW	0x0	Sw_dec_timeout_sta When high the decoder has been idling for too long. it will self reset the hardware, only when Sw_dec_timeout_e is 1'b1, this bit is valid.
14	RW	0x0	Sw_dec_error_sta Hevc & vp9: When high, an error is found in input data stream decoding. It will self reset the hardware. H264: When high, an error is found in input data stream. Decoding when Sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not.
13	RW	0x0	Sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware.
12	RW	0x0	Sw_dec_rdy_sta When this bit is high, decoder has decoded a picture( the loop filter module send out a frame rdy).
11	RW	0x0	Sw_dec_commonirq_mode 1'b0: In H264 and vp9 mode, the interrupt will wait strmd end pulse. 1'b1: In H264 and vp9 mode, the interrupt will not wait strmd end pluse.
10	WO	0x0	Sw_dec_e_rewrite_valid Sw_dec_e rewrite valid signal Maybe for only when buffer empty, restart the decoder use.
9	RW	0x0	Sw_dec_irq_raw The raw status of Sw_dec_irq,SW should reset this bit after interrupt is handled.
8	RO	0x0	Sw_dec_irq When high, decoder requests an interrupt. Sw_dec_irq = Sw_dec_irq_raw && (Sw_dec_irq_dis == 1'b0).
7	RW	0x0	Sw_stmerror_waitdecfifo_empty 1'b0: The stream error process will no wait the ca2decfifo empty. 1'b1: The stream error process will wait the ca2decfifo empty. When Sw_dec_mode is HEVC and VP9, it always take effect; when Sw_dec_mode is H264, it only take effect when Sw_h264_error_mode is 1'b0.
6	RW	0x0	Sw_buf_empty_en Buffer empty interrupt enable, now is for no use.
5	RW	0x1	Sw_dec_timeout_e If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
4	RW	0x0	Sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status.
3	RW	0x0	Sw_timeout_mode Timeout mode select 1'b0: TIMEOUT_CYCLES is 241'b1. 1'b1: TIMEOUT_CYCLES is 181'b1.
2	RW	0x0	Sw_dec_e_strmd_clkgate_dis In stream module, there contains HEVC,H264,VP9 modules, when it is 1'b1, these modules will no auto clk gate.

Bit	Attr	Reset Value	Description
1	RW	0x1	Sw_dec_clkgate_e 1'b0: Clock is running for all structures. 1'b1: Clock is gated for decoder structures that are not used.
0	RW	0x0	Sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format. HW will reset this when picture is processed stream error for vp9 & hevc & (h264 when Sw_h264_error_mode is 1'b0).

**rkvdec\_swreg2\_sysctrl**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_ycacherd_prior 1'b0: Y cacherd prior is higher than uv 1'b1: Y cache prior is equal than uv Fbc mode: Sw_head_prior_high_en 1'b0: Fbc head fetch data prior normal 1'b1: Fbc head fetch data prior high
30	RW	0x0	Sw_colmv_mode 1'b0: Default colmv storage mode, the colmv is put in Sw_decout_base + Sw_yuv_virstride 1'b1: The colmv is put in swreg78_colmv_cur_base
29	RW	0x0	Sw_buspr_slot_disable 1'b1: Bus prefetch slot manage disable
28	RW	0x0	Sw_h26x_frame_orslice For H26x use 1'b0: Frame 1'b1: Slice When Sw_h26x_streamd_mode is 1'b0, this register is valid.
27	RW	0x0	Sw_h264_firstslice_flag 1'b1: First packet in the frame, for h264 decode to read rps/pps data. because the first_mb_in_slice may be wrong, so need this syntax
26	RW	0x0	Sw_h26x_stream_lastpacket When Sw_h26x_stream_mode is 1'b1, Sw_h26x_stream_lastpacket 1'b0: this packet is not the last packet of frame. 1'b1: The packet is the last packet of frame.
25	RW	0x0	Sw_h26x_stream_mode 1'b0: Stream packet is slice by slice or frame by frame, should use Sw_h26x_frame_orslice. 1'b1: Stream packet is random, should use Sw_h26x_stream_last.
24	RW	0x0	Sw_h26x_rps_mode 1'b0: Hardware parse rps mode 1'b1: Software parse rps mode
23	RW	0x0	Sw_wait_reset_en 1'b0: Hardware will auto reset when error occur. 1'b1: Wait software process reset when error occur.
22	RW	0x0	Sw_info_collect_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
21:20	RW	0x0	Sw_dec_mode 2'd0: Hevc 2'd1: H264 2'd2: Vp9 2'd3: Use Sw_dec_mode_plus(swreg112[31:24])
19	RW	0x0	Sw_inter_error_prc_mode 1'b0: Mv used pred. 1'b1: Mv=0, and Sw_error_ref_base will be used.
18:12	RW	0x00	Sw_strm_start_bit Exact bit of stream start word where decoding can be started (associates with Sw_str_rlc_base).
11	RW	0x0	Sw_rlc_mode 1'b0: HW decodes video from bit stream 1'b1: HW decodes video from RLC input data
10	RW	0x0	Sw_rlc_mode_direct_write Cabac decode output direct write enable. When this bit is enable , all the module other than cabac and busifd are not work.
9	RW	0x0	Sw_error_info_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	Sw_out_cbr_swap 1'b0: Cb(u) is in the lower address, cr(v) is in the higher address 1'b1: Cb(u) is in the higher address, cr(v) is in the lower address Sw_in_cbr_swap is the same with Sw_out_cbr_swap.
7	RW	0x0	Sw_out_swap32_e may be used for 64 or 128 bit environment 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped
6	RW	0x0	Sw_out_endian 1'b0: Little endian 1'b1: Big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
5	RW	0x0	Sw_str_swap64_e may be used for 128 bit environment 1'b0: No swapping of 64 bit words 1'b1: 64 bit data words are swapped
4	RW	0x0	Sw_str_swap32_e may be used for 64 or 128 bit environment 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped
3	RW	0x0	Sw_str_endian 1'b0: Little endian 1'b1: Big endian for litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
2	RW	0x0	Sw_in_swap64_e may be used for 128 bit environment 1'b0: No swapping of 64 bit words 1'b1: 64 bit data words are swapped
1	RW	0x0	Sw_in_swap32_e may be used for 64 or 128 bit environment 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped



Bit	Attr	Reset Value	Description
0	RW	0x0	Sw_in_endian 1'b0: Little endian 1'b1: Big endian for little endian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.

**rkvdec\_swreg3\_picpar**

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Sw_slice_num_lowbits Hevc: Slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame) Just only used for rps read. H264: Slice number in a frame (0~4095, when it is 1, it real means 1 slice in a frame), for H264, it means Sw_slice_num_lowbits. Vp9: No use
20:12	RW	0x000	Sw_uv_hor_virstride Picture horizontal virtual stride (the unit is 128bit) The max is $(4096 \times 1.5 + 128) / 16 = 0x188$ Suggest this register to config to even for advance ddr performance.
11	RW	0x0	Sw_slice_num_highbit The highest bit of Sw_slice_num
10	RW	0x0	Sw_uv_hor_virstride_highbit Sw_uv_hor_virstride high bit
9:0	RW	0x000	Sw_y_hor_virstride Picture horizontal virtual stride (the unit is 128bit) the max is $(4096 \times 1.5 + 128) / 16 = 0x188$ Suggest this register to config to even for advance ddr performance. Fbc mode: Used for head hor virstirde.

**rkvdec\_swreg4\_strm\_rlc\_base**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_strm_rlc_base When swreg2.Sw_rlc_mode = 1, it is base address for rlc data. When swreg2.Sw_rlc_mode = 0, it is base address for stream, after a frame is decoded ready or error (stream error, time out, bus error), it is the last address of the stream. The address should 128bit align.

**rkvdec\_swreg5\_stream\_rlc\_len**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved
26:0	RW	0x0000000	Sw_stream_len Amount of stream 8bits in the input buffer, byte unitL the max of Sw_stream_len: $4096 \times 2304 \times 1.5 \times 1.5 = 0x1440000$ .

**rkvdec\_swreg6\_cabactbl\_prob\_base**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_cabactbl_base The base address of cabac table The address should 128bit align. For hevc/h264: Cabac tble base For vp9: Software parse prob mode: processed prob base Hardware parse prob mode: delta_prob_en + delta_prob base

**rkvdec swreg7 decout base**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_decout_base Base address of decoder output picture The address should be 128bit align. In H264 decode format, the top field and bottom field are the same addr. Fbc mode: Fbc_head_base_addr[27:0]: The head base of fbc wr.

**rkvdec swreg8 y virstride**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	Reserved
20:0	RW	0x00000000	Sw_y_virstride The output picture y virtual stride (the unit is 128bit) The max: $(4096 \times 1.5 + 128) \times 2304 = 0xdc8000$ we can know the Sw_uvout_base = Sw_decout_base + (Sw_y_virstride <<4)

**rkvdec swreg8 fbc payload st offset**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_payload_st_offset The offset should be 128bit align. Note: The payload will be store in the base: Sw_decout_base + Sw_payload_st_offset.

**rkvdec swreg9 yuv virstride**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_fbc_force_uncompress 1'b0: Allow fbce compress yuv block 1'b1: Force all yuv block use uncompress mode
30:22	RO	0x000	Reserved
21:0	RW	0x00000000	Sw_yuv_virstride The output picture yuv virtual stride (the unit is 128bit) The max: $(4096 \times 1.5 + 128) \times 2304 \times 1.5 = 0x14ac000$ We can know the Sw_mvout_base = Sw_decout_base + (Sw_yuv_virstride <<4). For yuv422: $4096 \times 2304 \times 2 \times 1.25 = 0x1680000$ For fbc mode: Sw_fbc_payload_stride[21:0]: The stride of payload Sw_mvout_base = Sw_decout_base + (Sw_yuv_virstride <<4)

**rkvdec swreg10 hevc refer0 base**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer0_base Base address for reference picture index 0 (the address should be 128bit align). Fbc mode: Hevc ref0 head base
3:0	RW	0x0	Sw_ref_valid_0_3 Valid flag for picture index 0 ~3

**rkvdec swreg10 h264 refer0 base**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer0_base Base address for reference picture index0 (the address should be 128bit align). Fbc mode: H264 ref0 head base
3	RW	0x0	Sw_ref0_colmv_use_flag Ref0 colmv use flag
2	RW	0x0	Sw_ref0_botfield_used Bottom field is used The same meaning with ref_valid
1	RW	0x0	Sw_ref0_topfield_used Top field is used The same meaning with ref_valid
0	RW	0x0	Sw_ref0_field 1'b0: Frame 1'b1: Field

**rkvdec swreg10 avs2 refer0 base**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer0_base Base address for reference picture index0 (the address should be 128bit align). Fbc mode: Avs2 ref0 head base
3	RW	0x0	Sw_ref0_valid_flag Reference picture0 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref0_bottomfield_flag refer0 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref0_field 1'b0: Frame 1'b1: Field

**rkvdec swreg10 vp9 cprheader offset**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	Sw_vp9_cprheader_offset Vp9 compressed header offset, at most 2000 probs, 10bit per prob, 20000 bit at most. Now is for no use, because it can read from the last syntax of the uncompressed header.

**rkvdec swreg11 h264 refer1 base**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer1_base Base address for reference picture index1 (the address should be 128bit align). Fbc mode: H264 ref1 head base
3	RW	0x0	Sw_ref1_colmv_use_flag Ref1 colmv use flag
2	RW	0x0	Sw_ref1_botfield_used Ref1 bottom field is used
1	RW	0x0	Sw_ref1_topfield_used Ref1 topfield is used
0	RW	0x0	Sw_ref1_field 1'b0: Frame 1'b1: Field

**rkvdec swreg11 vp9 referlast base**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9last_base Base address for last (the address should be 128bit align). Fbc mode: Vp9 last ref frame head base.

**rkvdec swreg11 avs2 refer1 base**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer1_base Base address for reference picture index 1 (the address should be 128bit align). Fbc mode: Avs2 ref1 head base
3	RW	0x0	Sw_ref1_valid_flag Reference picture1 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref1_bottomfield_flag Refer1 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref1_field 1'b0: Frame 1'b1: Field

**rkvdec swreg11 hevc refer1 base**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer1_base Base address for reference picture index 1 (the address should be 128bit align) Fbc mode: Hevc ref1 head base
3:0	RW	0x0	Sw_ref_valid_4_7 Valid flag for picture index 4~7

**rkvdec swreg12 vp9 refergolden base**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9golden_base Base address for golden (the address should be 128bit align) Fbc mode: Vp9 golden ref frame head base

**rkvdec swreg12 hevc refer2 base**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer2_base Base address for reference picture index 2 (the address should be 128bit align) Fbc mode: Hevc ref2 head base
3:0	RW	0x0	Sw_ref_valid_8_11 Valid flag for picture index 8~11

**rkvdec swreg12 avs2 refer2 base**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer2_base Base address for reference picture index 2 (the address should be 128bit align) Fbc mode: Avs2 ref2 head base
3	RW	0x0	Sw_ref2_valid_flag Reference picture2 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref2_bottomfield_flag Refer2 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref2_field 1'b0: Frame 1'b1: Field

**rkvdec swreg12 h264 refer2 base**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer2_base Base address for reference picture index2 (the address should be 128bit align). Fbc mode: H264 ref2 head base
3	RW	0x0	Sw_ref2_colmv_use_flag Ref2 colmv use flag
2	RW	0x0	Sw_ref2_botfield_used Ref2 bottom field is used

Bit	Attr	Reset Value	Description
1	RW	0x0	Sw_ref2_topfield_used Ref2 topfield is used
0	RW	0x0	Sw_ref2_field 1'b0: Frame 1'b1: Field

**rkvddec swreg13 hevc refer3 base**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer3_base Base address for reference picture index 3 (the address should be 128bit align) Fbc mode: Hevc ref3 head base
3	RO	0x0	Reserved
2:0	RW	0x0	Sw_ref_valid_12_14 Valid flag for picture index 12~14

**rkvddec swreg13 h264 refer3 base**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer3_base Base address for reference picture index3 (the address should be 128bit align) Fbc mode: H264 ref3 head base
3	RW	0x0	Sw_ref3_colmv_use_flag Ref3 colmv use flag
2	RW	0x0	Sw_ref3_botfield_used Ref3 bottom field is used
1	RW	0x0	Sw_ref3_topfield_used Ref3 topfield is used
0	RW	0x0	Sw_ref3_field 1'b0: Frame 1'b1: Field

**rkvddec swreg13 avs2 refer3 base**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer3_base Base address for reference picture index 3 (the address should be 128bit align) Fbc mode: Avs2 ref3 head base
3	RW	0x0	Sw_ref3_valid_flag Reference picture3 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref3_bottomfield_flag Refer3 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref3_field 1'b0: Frame 1'b1: Field

**rkvddec swreg13 vp9 referalfter base**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9alter_base Base address for alter (the address should be 128bit align) Fbc mode: Vp9 after ref frame head base.

**rkvdec swreg14 h264 refer4 base**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer4_base Base address for reference picture index4 (the address should be 128bit align). Fbc mode: H264 ref4 head base
3	RW	0x0	Sw_ref4_colmv_use_flag Ref4 colmv use flag
2	RW	0x0	Sw_ref4_botfield_used Ref4 bottom field is used
1	RW	0x0	Sw_ref4_topfield_used Ref4 topfield is used
0	RW	0x0	Sw_ref4_field 1'b0: Frame 1'b1: Field

**rkvdec swreg14 vp9count base**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Sw_vp9_count_prob_base Software parse prob: Used as vp9 count write base Hardware parse prob: Used as vp9 prob write base
2:1	RO	0x0	Reserved
0	RW	0x0	Sw_vp9count_update_en When 1'b1, the hardware will always update count. When 1'b0, the hardware will auto check whether update the count.

**rkvdec swreg14 avs2 refer4 base**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer4_base Base address for reference picture index 4(the address should be 128bit align) Fbc mode: Avs2 ref4 head base
3	RW	0x0	Sw_ref4_valid_flag reference picture4 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref4_bottomfield_flag refer4 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref4_field 1'b0: Frame 1'b1: Field

**rkvdec swreg14 hevc refer4 base**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer4_base Base address for reference picture index 4(the address should be 128bit align) Fbc mode: Hevc ref4 head base

**rkvdec swreg15 hevc refer5 base**

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer5_base Base address for reference picture index 5(the address should be 128bit align) Fbc mode: Hevc ref5 head base

**rkvdec swreg15 h264 refer5 base**

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer5_base Base address for reference picture index5 (the address should be 128bit align) Fbc mode: H264 ref5 head base
3	RW	0x0	Sw_ref5_colmv_use_flag Ref5 colmv use flag
2	RW	0x0	Sw_ref5_botfield_used Ref5 bottom field is used
1	RW	0x0	Sw_ref5_topfield_used Ref5 topfield is used
0	RW	0x0	Sw_ref5_field 1'b0: Frame 1'b1: Field

**rkvdec swreg15 avs2 refer5 base**

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer5_base Base address for reference picture index 5(the address should be 128bit align) Fbc mode: Avs2 ref5 head base
3	RW	0x0	Sw_ref5_valid_flag Reference picture5 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref5_bottomfield_flag Refer5 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref5_field 1'b0: Frame 1'b1: Field

**rkvdec swreg15 vp9 segidlast base**

Address: Operational Base + offset (0x003c)



Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9segidlast_base Base address for vp9 last frame segment id (the address should be 128bit align).

**rkvdec swreg16 h264 refer6 base**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer6_base Base address for reference picture index6 (the address should be 128bit align). Fbc mode: H264 ref6 head base
3	RW	0x0	Sw_ref6_colmv_use_flag Ref6 colmv use flag
2	RW	0x0	Sw_ref6_botfield_used Ref6 botfield is used
1	RW	0x0	Sw_ref6_topfield_used Ref6 topfield is used
0	RW	0x0	Sw_ref6_field 1'b0: Frame 1'b1: Field

**rkvdec swreg16 vp9 segidcur base**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9segidcur_base Base address for vp9 cur frame segment id (the address should be 128bit align).

**rkvdec swreg16 avs2 refer6 base**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer6_base Base address for reference picture index 6(the address should be 128bit align). Fbc mode: Avs2 ref6 head base
3	RW	0x0	Sw_ref6_valid_flag Reference picture6 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref6_bottomfield_flag Refer6 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref6_field 1'b0: Frame 1'b1: Field

**rkvdec swreg16 hevc refer6 base**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_refer6_base Base address for reference picture index 6(the address should be 128bit align). Fbc mode: Hevc ref6 head base

**rkvdec swreg17 vp9 frame size last**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_frameheight_last Last frame frame_size_height
15:0	RW	0x0000	Sw_framewidth_last Last frame frame_size_width

**rkvdec swreg17 hevc refer7 base**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer7_base Base address for reference picture index 7(the address should be 128bit align). Fbc mode: Hevc ref7 head base

**rkvdec swreg17 avs2 refer7 base**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer7_base Base address for reference picture index 7(the address should be 128bit align). Fbc mode: Avs2 ref7 head base Avs2 most support 8 reference frame.
3	RW	0x0	Sw_ref7_valid_flag Reference picture7 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref7_bottomfield_flag Refer7 is top field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	Reserved
0	RW	0x0	Sw_ref7_field 1'b0: Frame 1'b1: Field

**rkvdec swreg17 h264 refer7 base**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer7_base Base address for reference picture index7 (the address should be 128bit align) Fbc mode: H264 ref7 head base
3	RW	0x0	Sw_ref7_colmv_use_flag Ref7 colmv use flag
2	RW	0x0	Sw_ref7_botfield_used Ref7 bottom field is used
1	RW	0x0	Sw_ref7_topfield_used Ref7 topfield is used
0	RW	0x0	Sw_ref7_field 1'b0: Frame 1'b1: Field

**rkvdec swreg18 hevc refer8 base**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer8_base Base address for reference picture index 8(the address should be 128bit align). Fbc mode: Hevc ref8 head base

**rkvdec swreg18 h264 refer8 base**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer8_base Base address for reference picture index8 (the address should be 128bit align). Fbc mode: H264 ref8 head base
3	RW	0x0	Sw_ref8_colmv_use_flag Ref8 colmv use flag
2	RW	0x0	Sw_ref8_botfield_used Ref8 bottom field is used
1	RW	0x0	Sw_ref8_topfield_used Ref8 topfield is used
0	RW	0x0	Sw_ref8_field 1'b0: Frame 1'b1: Field

**rkvdec swreg18 vp9 frame size golden**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_frameheight_golden Golden frame_size_height
15:0	RW	0x0000	Sw_framewidth_golden Golden frame_size_width

**rkvdec swreg19 hevc refer9 base**

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer9_base Base address for reference picture index 9(the address should be 128bit align) Fbc mode: Hevc ref9 head base

**rkvdec swreg19 h264 refer9 base**

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer9_base Base address for reference picture index9 (the address should be 128bit align). Fbc mode: H264 ref9 head base
3	RW	0x0	Sw_ref9_colmv_use_flag Ref9 colmv use flag
2	RW	0x0	Sw_ref9_botfield_used Ref9 bottom field is used
1	RW	0x0	Sw_ref9_topfield_used Ref9 topfield is used
0	RW	0x0	Sw_ref9_field 1'b0: Frame 1'b1: Field

**rkvdec swreg19 vp9 frame size altref**

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_frameheight_alter Alter frame_size_height
15:0	RW	0x0000	Sw_framewidth_alter Alter frame_size_width

**rkvdec swreg20 hevc refer10 base**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer10_base Base address for reference picture index 10(the address should be 128bit align). Fbc mode: Hevc ref10 head base

**rkvdec swreg20 h264 refer10 base**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer10_base Base address for reference picture index10 (the address should be 128bit align) Fbc mode: H264 ref10 head base
3	RW	0x0	Sw_ref10_colmv_use_flag Ref10 colmv use flag
2	RW	0x0	Sw_ref10_botfield_used Ref10 bottom field is used
1	RW	0x0	Sw_ref10_topfield_used Ref10 topfield is used
0	RW	0x0	Sw_ref10_field 1'b0: Frame 1'b1: Field

**rkvdec swreg20 vp9 segid grp0**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid0_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid0_referinfo Specifies segment it's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid0_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid0_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid0_frame_loopfilter_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid0_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid0_Frame_qp_delta_en Frame_qp_delta feature enable.

Bit	Attr	Reset Value	Description
0	RW	0x0	Sw_vp9segid_abs_delta Used to decide quant and loopfilter param.

**rkvdec swreg21 hevc refer11 base**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer11_base Base address for reference picture index 11(the address should be 128bit align). Fbc mode: Hevc ref11 head base

**rkvdec swreg21 h264 refer11 base**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer11_base Base address for reference picture index11 (the address should be 128bit align). Fbc mode: H264 ref11 head base
3	RW	0x0	Sw_ref11_colmv_use_flag Ref11 colmv use flag
2	RW	0x0	Sw_ref11_botfield_used Ref11 bottom field is used
1	RW	0x0	Sw_ref11_topfield_used Ref11 topfield is used
0	RW	0x0	Sw_ref11_field 1'b0: Frame 1'b1: Field

**rkvdec swreg21 vp9 segid grp1**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid1_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid1_referinfo Specifies segment it's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid1_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid1_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid1_frame_loopfilter_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid1_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid1_Frame_qp_delta_en Frame_qp_delta feature enable.

**rkvdec swreg22 hevc refer12 base**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer12_base Base address for reference picture index 12(the address should be 128bit align). Fbc mode: Hevc ref12 head base

**rkvdec swreq22 h264 refer12 base**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer12_base Base address for reference picture index12 (the address should be 128bit align). Fbc mode: H264 ref12 head base
3	RW	0x0	Sw_ref12_colmv_use_flag Ref12 colmv use flag
2	RW	0x0	Sw_ref12_botfield_used Ref12 bottom field is used
1	RW	0x0	Sw_ref12_topfield_used Ref12 topfield is used
0	RW	0x0	Sw_ref12_field 1'b0: Frame 1'b1: Field

**rkvdec swreq22 vp9 segid grp2**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid2_frame_skip_en Frame skip feature enable
21:20	RW	0x0	Sw_vp9segid2_referinfo Specifies segment it's reference_info which is used to get ref_frame[0]
19	RW	0x0	Sw_vp9segid2_referinfo_en Frame reference info enable
18:12	RW	0x00	Sw_vp9segid2_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	Sw_vp9segid2_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	Sw_vp9segid2_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	Sw_vp9segid2_Frame_qp_delta_en Frame_qp_delta feature enable

**rkvdec swreq23 hevc refer13 base**

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer13_base Base address for reference picture index 13(the address should be 128bit align). Fbc mode: Hevc ref13 head base

**rkvdec swreq23 h264 refer13 base**

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer13_base Base address for reference picture index13 (the address should be 128bit align). Fbc mode: H264 ref13 head base
3	RW	0x0	Sw_ref13_colmv_use_flag Ref13 colmv use flag
2	RW	0x0	Sw_ref13_botfield_used Ref13 bottom field is used
1	RW	0x0	Sw_ref13_topfield_used Ref13 topfield is used
0	RW	0x0	Sw_ref13_field 1'b0: Frame 1'b1: Field

**rkvdec swreg23 vp9 segid grp3**

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid3_frame_skip_en Frame skip feature enable
21:20	RW	0x0	Sw_vp9segid3_referinfo Specifies segment it's reference_info which is used to get ref_frame[0]
19	RW	0x0	Sw_vp9segid3_referinfo_en Frame reference info enable
18:12	RW	0x00	Sw_vp9segid3_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	Sw_vp9segid3_frame_loopfilter_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	Sw_vp9segid3_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	Sw_vp9segid3_Frame_qp_delta_en Frame_qp_delta feature enable

**rkvdec swreg24 hevc refer14 base**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer14_base Base address for reference picture index 14(the address should be 128bit align) Fbc mode: Hevc ref14 head base

**rkvdec swreg24 h264 refer14 base**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer14_base Base address for reference picture index14 (the address should be 128bit align). Fbc mode: H264 ref14 head base
3	RW	0x0	Sw_ref14_colmv_use_flag Ref14 colmv use flag
2	RW	0x0	Sw_ref14_botfield_used Ref14 bottom field is used

Bit	Attr	Reset Value	Description
1	RW	0x0	Sw_ref14_topfield_used Ref14 topfield is used
0	RW	0x0	Sw_ref14_field 1'b0: Frame 1'b1: Field

**rkvdec swreg24 vp9 segid grp4**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid4_frame_skip_en Frame skip feature enable
21:20	RW	0x0	Sw_vp9segid4_referinfo Specifies segment it's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid4_referinfo_en Frame reference info enable
18:12	RW	0x00	Sw_vp9segid4_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid4_frame_loopfilter_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	Sw_vp9segid4_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid4_Frame_qp_delta_en Frame_qp_delta feature enable.

**rkvdec swreg25 vp9 segid grp5**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid5_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid5_referinfo Specifies segment it's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid5_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid5_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid5_frame_loopfilter_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid5_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid5_Frame_qp_delta_en Frame_qp_delta feature enable.

**rkvdec swreg25 refer0 poc**

Address: Operational Base + offset (0x0064)



Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer0_poc the poc of reference picture index 0

**rkvdec swreq26 vp9 segid grp6**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid6_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid6_referinfo Specifies segment it's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid6_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid6_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid6_frame_loopfilter_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid6_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid6_Frame_qp_delta_en Frame_qp_delta feature enable.

**rkvdec swreq26 refer1 poc**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer1_poc the poc of reference picture index 1

**rkvdec swreq27 vp9 segid grp7**

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_vp9segid7_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid7_referinfo Specifies segment it's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid7_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid7_Frame_loopfilter_value Specifies segment it's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid7_frame_loopfilter_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid7_Frame_qp_delta Specifies segment it's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid7_Frame_qp_delta_en Frame_qp_delta feature enable.

**rkvdec swreq27 refer2 poc**

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer2_poc the poc of reference picture index 2

**rkvdec swreg28 vp9 cprheader config**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	Reserved
4:3	RW	0x0	Sw_vp9_frame_reference_mode Frame_reference_mode specifies frame reference mode. SINGLE_REFERENCE = 0, COMPOUND_REFERENCE = 1, REFERENCE_MODE_SELECT = 2, REFERENCE_MODES = 3, When frame_reference_mode_flag0 is not present, it equal to 0 by default. When frame_reference_mode_flag1 is not present, it equal to 0 by default. Frame_reference_mode = frame_reference_mode_flag0 == 0 ? Frame_reference_mode_flag1 == 0 ? REFERENCE_MODE_SELECT : COMPOUND_REFERENCE) : SINGLE_REFERENCE
2:0	RW	0x0	Sw_vp9_tx_mode Tx_mode specifies frame transform mode. ONLY_4X4 = 0, // only 4x4 transform used ALLOW_8X8 = 1, // allow block transform size up to 8x8 ALLOW_16X16 = 2, // allow block transform size up to 16x16 ALLOW_32X32 = 3, // allow block transform size up to 32x32 TX_MODE_SELECT = 4, // transform specified for each block

**rkvdec swreg28 refer3 poc**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer3_poc The poc of reference picture index 3

**rkvdec swreg29 vp9 lref scale**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_vp9_lref_ver_scale Vertical scaling factor for last reference picture
15:0	RW	0x0000	Sw_vp9_lref_hor_scale Horizontal scaling factor for last reference picture Sw_vp9_lref_hor_scale = (last_ref_width / cur_width) * 0x4000

**rkvdec swreg29 refer4 poc**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer4_poc The poc of reference picture index 4

**rkvdec swreg30 vp9 gref scale**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_vp9_gref_ver_scale Vertical scaling factor for golden reference picture
15:0	RW	0x0000	Sw_vp9_gref_hor_scale Horizontal scaling factor for golden reference picture $Sw\_vp9\_gref\_hor\_scale = (golden\_ref\_width / cur\_width) * 0x4000$

**rkvdec swreg30 refer5 poc**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer5_poc The poc of reference picture index 5

**rkvdec swreg31 vp9 aref scale**

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_vp9_aref_ver_scale Vertical scaling factor for alfter reference picture
15:0	RW	0x0000	Sw_vp9_aref_hor_scale Horizontal scaling factor for alfter reference picture $Sw\_vp9\_gref\_hor\_scale = (alfter\_ref\_width / cur\_width) * 0x4000$

**rkvdec swreg31 refer6 poc**

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer6_poc The poc of reference picture index 6

**rkvdec swreg32 vp9 ref deltas lastframe**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:0	RW	0x00000000	Sw_vp9_ref_deltas_lastframe Vp9 ref deltas of lastframe, for cal loopfilter filter type use.

**rkvdec swreg32 refer7 poc**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer7_poc The poc of reference picture index 7

**rkvdec swreg33 vp9 info lastframe**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22:20	RW	0x0	Sw_vp9_color_space_lastkeyframe Vp9 last keyframe color_space
19	RW	0x0	Sw_vp9_last_widthheight_eqcur Last width and height equal cur frame
18	RW	0x0	Sw_vp9_last_intra_only Vp9 last frame intra only flag To give inter command use It is for last_dec_frame

Bit	Attr	Reset Value	Description
17	RW	0x0	Sw_vp9_last_show_frame For cal the flag use_prev_in_find_mv_refs which is to inter cmd. It is for last_dec_frame.
16	RW	0x0	Sw_segmentation_enable_1stframe 1'b1: Sw_segmentation_enable for last frame. It is for last_dec_frame.
15:14	RO	0x0	Reserved
13:0	RW	0x0000	Sw_vp9_mode_deltas_lastframe Vp9 mode deltas It is for last dec frame.

**rkvdec\_swreg33\_refer8\_poc**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer8_poc The poc of reference picture index 8

**rkvdec\_swreg34\_vp9\_intercmd\_base**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9_intercmd_base Vp9 inter command base addr, when Sw_rlc_mode is 1'b1; when Sw_dec_mode is VP9 and Sw_rlc_mode is 1'b1, when read this register, after a frame is decoded ready or error (stream error, time out, bus error), it is the end address of the intercmd.

**rkvdec\_swreg34\_refer9\_poc**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer9_poc The poc of reference picture index 9

**rkvdec\_swreg35\_vp9\_intercmd\_num**

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Sw_vp9_intercmd_num When rlc_mode is 1'b1, for Sw_vp9_intercmd_num. It's unit is 128bit. It count from 1.

**rkvdec\_swreg35\_refer10\_poc**

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer10_poc The poc of reference picture index 10

**rkvdec\_swreg36\_vp9\_lasttile\_size**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Sw_vp9_lasttile_size Vp9 last tile size ofr cur frame. Its unit is byte. The real meaning the current frame size.

**rkvdec swreg36 refer11 poc**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer11_poc The poc of reference picture index 11.

**rkvdec swreg37 vp9 lastf hor virstride**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved
25:16	RW	0x000	Sw_vp9_lastfuv_hor_virstride Vp9 last frame uv horizontal virstride
15:10	RO	0x00	Reserved
9:0	RW	0x000	Sw_vp9_lastfy_hor_virstride Vp9 last frame y horizontal virstride For Fbc mode: Vp9 head hor stride of last frame

**rkvdec swreg37 refer12 poc**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer12_poc The poc of reference picture index 12

**rkvdec swreg38 vp9 goldenf hor virstride**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved
25:16	RW	0x000	Sw_vp9_goldenuv_hor_virstride Vp9 golden uv horizontal virstirde
15:10	RO	0x00	Reserved
9:0	RW	0x000	Sw_vp9_goldenfy_hor_virstride Vp9 golden frame y horizontal virstride For fbc mode: Vp9 head hor stride of golden frame

**rkvdec swreg38 refer13 poc**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer13_poc The poc of reference picture index 13

**rkvdec swreg39 vp9 altreff hor virstride**

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved
25:16	RW	0x000	Sw_vp9_altreffuv_hor_virstride Vp9 altreff uv horizontal virstirde
15:10	RO	0x00	Reserved
9:0	RW	0x000	Sw_vp9_altreffy_hor_virstride Vp9 altref frame y horizontal virstride For fbc mode: Vp9 head hor stride of after frame

**rkvdec swreg39 refer14 poc**

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer14_poc The poc of reference picture index 14

**rkvdec swreg40 cur\_poc**

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_cur_poc The poc of the cur picture For H264, it may be cur frame poc or cur top field poc

**rkvdec swreg41 colbuf\_base**

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colbuf_base The base address of deblocking colbuf wr and rd base addr (128bit align).

**rkvdec swreg41 rlcwrite\_base**

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Sw_rlcwrite_base The base address of rlcwrite(the address should 64bit align) cabac output write to this rlcwrite base address when Sw_rlc_mode_direct_write in swreg2_sysctrl is valid.

**rkvdec swreg42 vp9 last\_prob\_base**

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9_last_porb_base The base address of last prob (the address should 128bit align).

**rkvdec swreg42 avs2 head\_base**

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_avs2_head_base The base address of avs2 head (the address should 128bit align) It will include sequence and picture level syntax.

**rkvdec swreg42 pps\_base**

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_pps_base The base address of pps (the address should 128bit align) It is for storing sps(sequence parameter set) and pps(picture parameter set).

**rkvdec swreg43 avs2 head\_len**

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	Sw_avs2_head_len It's unit is 128bit 0: 128bit 1: 2*128bit 2: 3*128bit ..... 15: 16*128bit

**rkvdec swreg43 rps base**

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_rps_base Rps(reference picture set) base address (the address should 128bit align).

**rkvdec swreg44 strmd error en**

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_strmd_error_e Strmd error enable regs In HEVC,it is called Sw_cabac_error_e For VP9, it use Sw_strmd_error_e[3:0] Sw_strmd_error_e[0] is for Sw_vp9_tilesize_error Sw_strmd_error_e[1] is for Sw_vp9_segskip_error Sw_strmd_error_e[2] is for Sw_vp9_error_init_error Sw_strmd_error_e[3] is for Sw_vp9_uncpr Avs2: [0]: Slice_horizontal_position logic error [1]: Rame_end_error [2]: Slice_vertical_position out of range [3]: Slice_horizontal_position out of range [4]: Slice_qp [5]: Aec_byte_alignment_bit [6]: Aec_lcu_stuffing_bit [7]: Mv_diff_x [8]: Mv_diff_y [9]: Cu_qp_delta [10]: Intra_luma_pred_mode [11]: Intra_chroma_pred_mode [12]: Coeff_level_minus1_pos_in_band [13]: Slice_error_end [14]: Slice ctu coordinate error

**rkvdec swreg45 vp9 error info0**

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Vp9_error_info0 For vp9 16 tile cols, every cols contains 4bits Vp9_error_info0[3:0] is for col 0. Vp9_error_info0[1:0] is to tell tile_rows_cnt[1:0]. Vp9_error_info0[3:2] is to tell the error type. 2'b00: No error 2'b01: Tilesize error 2'b10: Seg skip error 2'b11: Ref scale error

**rkvdec swreg45 strmd error status**

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Sw_colmv_error_ref_pidx When Sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module. It is For H264 and HEVC.
27:0	RW	0x0000000	Sw_strmd_error_status Strmd error status In HEVC & H264, it is called cabac error status.

**rkvdec swreg46 strmd error ctu**

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved
24	RW	0x0	Sw_vp9_error_ctu0_en 1'b1: There is atleast a error in vp9 strmd now ,is no for use.
23	RO	0x0	Reserved
22:16	RW	0x40	Sw_streamfifo_space2full It is for debug use, to tell the stream fifo space to full. For HEVC, H264 and VP9.
15:8	RW	0x00	Sw_strmd_error_ctu_yoffset Strmd error ctu yoffset For HEVC, H264 and VP9 For VP9, it is the value of stSw_vp9_error_ctu0_y
7:0	RW	0x00	Sw_strmd_error_ctu_xoffset strmd error ctu xoffset for all HEVC and H264 and VP9 for vp9, it is the value of stSw_vp9_error_ctu0_x

**rkvdec swreg47 sao ctu position**

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved
25:16	RW	0x000	Sw_saowr_yoffset Saowr y offset , its unit is 4 line pixel 0: Sao begin to write 0~3 pic line 1: Sao begin to write 4-7 pic line ..... Only valid when ip has any error.
15:9	RO	0x00	Reserved
8:0	RW	0x000	Sw_saowr_xoffset Saowr x address offset, its unit is 128bit 0: Sao begin to write cur line first 128bit 1: Sao begin to write cur line second 128bit ..... Only valid when ip has any error.

**rkvdec swreg48 vp9 last ystride**

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	Reserved
20:0	RW	0x000000	Sw_vp9_lastfy_virstride Vp9 last frame y stride



**rkvdec swreg48 h264 refer15 base**

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer15_base Base address for reference picture index15(the address should be 128bit align). Fbc mode: H264 ref15 head base
3	RW	0x0	Sw_ref15_colmv_use_flag Ref15 colmv use flag
2	RW	0x0	Sw_ref15_botfield_used Ref15 bottom field is used
1	RW	0x0	Sw_ref15_topfield_used Ref15 topfield is used
0	RW	0x0	Sw_ref15_field 1'b0: Frame 1'b1: Field

**rkvdec swreg49 vp9 golden ystride**

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	Reserved
20:0	RW	0x000000	Sw_vp9_goldeny_virstride Vp9 golden frame y stride

**rkvdec swreg49 h26x refer15 poc**

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer15_poc The poc of reference picture index 15 Used to hevc for mvc

**rkvdec swreg50 vp9 altrefy ystride**

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	Reserved
20:0	RW	0x000000	Sw_vp9_altrefy_virstride Vp9 altref frame y stride

**rkvdec swreg50 h264 refer16 poc**

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer16_poc The poc of reference picture index 16

**rkvdec swreg51 vp9 lastref yuvstride**

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved
21:0	RW	0x000000	Sw_vp9_lastref_yuv_virstride Vp9 lastref frame yuv vir stride

**rkvdec swreg51 h264 refer17 poc**

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer17_poc The poc of reference picture index 17

**rkvdec swreg52 h264 refer18 poc**

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer18_poc The poc of reference picture index 18

**rkvdec swreg52 vp9 refcolmv base**

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_vp9_refcolmv_base Vp9 ref colmv base addr

**rkvdec swreg53 h264 refer19 poc**

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer19_poc The poc of reference picture index 19

**rkvdec swreg54 h264 refer20 poc**

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer20_poc The poc of reference picture index 20

**rkvdec swreg55 h264 refer21 poc**

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer21_poc The poc of reference picture index 21

**rkvdec swreg56 h264 refer22 poc**

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer22_poc The poc of reference picture index 22

**rkvdec swreg57 h264 refer23 poc**

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer23_poc The poc of reference picture index 23

**rkvdec swreg58 h264 refer24 poc**

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer24_poc The poc of reference picture index 24

**rkvdec swreg59 h264 refer25 poc**

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer25_poc The poc of reference picture index 25

**rkvdec swreg60 h264 refer26 poc**

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer26_poc The poc of reference picture index 26

**rkvdec swreg61 h264 refer27 poc**

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer27_poc The poc of reference picture index 27

**rkvdec swreg62 h264 refer28 poc**

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer28_poc The poc of reference picture index 28

**rkvdec swreg63 h264 refer29 poc**

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer29_poc The poc of reference picture index 29

**rkvdec swreg64 hevc mvc0**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15:0	RW	0x0000	Sw_ref_pic_layer_same_with_cur reference picture layer same with current picture

**rkvdec swreg64 avs2 ctrl extra**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_slice_hor_pos_ctrl 1'b0: Use default 255 1'b1: Use fixed 256

**rkvdec swreg64 vp9 prob**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_inter_coef_rfsh_flag 1'b0: Inter coef unneed refresh in current intra frame 1'b1: Inter coef should be refresh in current intra frame
30	RW	0x0	Sw_last_key_frame_flag The flag of last frame is key frame 1'b0: Not key frame 1'b1: Key frame

Bit	Attr	Reset Value	Description
29	RW	0x0	Sw_vp9_allow_high_precision_mv The enable of high precision mv prob refresh update 1'b0: Disable 1'b1: Enable
28	RW	0x0	Sw_vp9_interp_filter_switch_en The enable of interp filter prob refresh update 1'b0: Disable 1'b1: Enable
27	RW	0x0	Sw_vp9_comp_ref_rfsh_en The enable of comp reference prob refresh update 1'b0: Disable 1'b1: Enable
26	RW	0x0	Sw_vp9_single_ref_rfsh_en The enable of single reference prob refresh update 1'b0: Disable 1'b1: Enable
25	RW	0x0	Sw_vp9_ref_mode_rfsh_en The enable of reference mode prob refresh update 1'b0: Disable 1'b1: Enable
24	RW	0x0	Sw_vp9_txfmmode_rfsh_en The enable of tx mode prob refresh update 1'b0: Disable 1'b1: Enable
23	RW	0x0	Sw_vp9_intra_only_flag The flag of intra only 1'b0: Inter frame 1'b1: Intra only frame include key frame
22	RW	0x0	Sw_vp9_prob_save_en The flag of write updated prob to DDR 1'b0: Not need write updated prob to DDR 1'b1: Will write updated prob to DDR
21	RW	0x0	Sw_vp9_refresh_en The enable of prob backward refresh 1'b0: Disable refresh parse 1'b1: Enable refresh parse
20	RW	0x0	Sw_vp9_prob_update_en The enable of used hardware to parse prob 1'b0: Software parse prob 1'b1: Hardware parse prob

**rkvdec swreg65 hevc mvc1**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	Reserved
17	RW	0x0	Sw_mvc_poc15_valid_flag Mvc poc15 valid flag
16	RW	0x0	Sw_vps_poc_lsb_aligned_flag Rps POC lsb aligned flag
15	RW	0x0	Sw_poc_reset_info_present_flag The flag of poc reset information
14	RW	0x0	Sw_max_one_active_ref_layer_flag The flag of max reference layer be activated
13	RW	0x0	Sw_default_ref_layers_active_flag The flag of default reference layers which be activated

Bit	Attr	Reset Value	Description
12:7	RW	0x00	Sw_num_reflayer_pics The number of reference layer pictures
6:1	RW	0x00	Sw_num_direct_ref_layers The number of direct reference layers
0	RW	0x0	Sw_poc_lsb_not_present_flag Poc lsb not present flag

**rkvdec swreg66 error ref base**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_error_ref_base Error reference frame base address

**rkvdec swreg66 avs2 error ref base**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_error_ref_base Error reference frame base address
3:2	RO	0x0	Reserved
1	RW	0x0	Sw_ref_error_topfield_flag Refer error is top field flag 1'b0: Tottom field flag 1'b1: Top field flag
0	RW	0x0	Sw_ref_error_field 1'b0: Frame 1'b1: Field

**rkvdec swreg67 error info**

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29	RW	0x0	Sw_error_prc_deb_en 1'b0: Disable 1'b1: Enable only valid when Sw_error_prc_intra_mode_sel = 1'b1.
28	RW	0x0	Sw_error_prc_intra_mode_sel 1'b0: Use inter mode to proc error ctu 1'b1: Use intra mode to proc error ctu
27:25	RO	0x0	Reserved
24	RW	0x0	All_frame_error_flag 1'b1: All frame ctu error
23:21	RO	0x0	Reserved
20:16	RW	0x00	Sw_pic_idx_replace Hevc: [4:1]: Default pic idx [0]: Invalid H264: [4:1]: Default pic idx [0]: Field mode: 1'b0: Top field; 1'b1: Bottom field Frame mode:invalid
15	RO	0x0	Reserved
14:0	RW	0x0001	Sw_error_ctu_num H264 and hevc error ctu number

**rkvdec swreg68 performance sel**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved
21:16	RW	0x00	Perf_cnt2_sel Performance monitor ctrl count2
15:14	RO	0x0	Reserved
13:8	RW	0x00	Perf_cnt1_sel Performance monitor ctrl count1
7:6	RO	0x0	Reserved
5:0	RW	0x00	Perf_cnt0_sel Performance monitor ctrl count0

**rkvdec\_swreg69 performance cnt0**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Perf_cnt0 Performance count value0

**rkvdec\_swreg70 performance cnt1**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Perf_cnt1 Performance count value1

**rkvdec\_swreg71 performance cnt2**

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Perf_cnt2 Performance count value2

**rkvdec\_swreg72 h264 refer30 poc**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer30_poc The poc of reference picture index 30

**rkvdec\_swreg73 h264 refer31 poc**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer31_poc The poc of reference picture index 31

**rkvdec\_swreg74 h264 cur\_poc1**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_h264_cur_poc1 H264 cur poc for bottom field

**rkvdec\_swreg75 h26x errorinfo base**

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Sw_errorinfo_base Error info base addr H264: Every slice contains 256 bits error info

**rkvdec swreg75 vp9 error info1**

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Vp9_error_info1 For vp9 16 tile cols, every cols contains 4bits Vp9_error_info0[3:0] is for col 8 Vp9_error_info0[1:0] is to tell tile_rows_cnt[1:0] Vp9_error_info0[3:2] is to tell the error type 2'b00: No error 2'b01: Tilesize error 2'b10: Seg skip error

**rkvdec swreg76 h26x errorinfo num**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:16	RW	0x0000	Sw_error_packet_num Error packet number
15	RW	0x0	Sw_strmd_detect_error_flag Stream logic error detected, it will stop decode.
14	RO	0x0	Reserved
13:0	RW	0x0000	Sw_slicedec_num H264 decoded num, the max slice num for H264 is 4096.

**rkvdec swreg76 vp9 error ctu1**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15	RW	0x0	Vp9_error_ctu1_en 1'b1: There are at least two ctus error
14	RO	0x0	Reserved
13:8	RW	0x00	Vp9_error_ctu1_y To tell the error ctu1 y position
7:6	RO	0x0	Reserved
5:0	RW	0x00	Vp9_error_ctu1_x To tell the error ctu1 x position

**rkvdec swreg77 h264 error e**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:28	RW	0x0	Sw_strmd_error_en Sw_strmd_error_en[0]: HEVC, H264 slice end error enable Sw_strmd_error_en[1]: HEVC, H264, VP9 frame end error enable
27:0	RW	0x00000000	Sw_h264_error_en_highbits H264 error enable bits

**rkvdec swreg78 colmv cur base**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_cur_base Only valid when Sw_colmv_mode is 1'b1. Cur frame colmv base addr. For HEVC, H264 and vp9.

**rkvdec swreg79 colmv ref0 base**

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref0_base Only valid when Sw_colmv_mode is 1'b1. Ref0 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg80 colmv ref1 base**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref1_base Only valid when Sw_colmv_mode is 1'b1. Ref1 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg81 colmv ref2 base**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref2_base Only valid when Sw_colmv_mode is 1'b1. Ref2 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg82 colmv ref3 base**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref3_base Only valid when Sw_colmv_mode is 1'b1. Ref3 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg83 colmv ref4 base**

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref4_base Only valid when Sw_colmv_mode is 1'b1. Ref4 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg84 colmv ref5 base**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref5_base Only valid when Sw_colmv_mode is 1'b1. Ref5 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg85 colmv ref6 base**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref6_base Only valid when Sw_colmv_mode is 1'b1. Ref6 frame colmv base addr. For H264 and HEVC.



**rkvdec swreg86 colmv ref7 base**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref7_base Only valid when Sw_colmv_mode is 1'b1. Ref7 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg87 colmv ref8 base**

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref8_base Only valid when Sw_colmv_mode is 1'b1. Ref8 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg88 colmv ref9 base**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref9_base Only valid when Sw_colmv_mode is 1'b1. Ref9 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg89 colmv ref10 base**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref10_base Only valid when Sw_colmv_mode is 1'b1. Ref10 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg90 colmv ref11 base**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref11_base Only valid when Sw_colmv_mode is 1'b1. Ref11 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg91 colmv ref12 base**

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref12_base Only valid when Sw_colmv_mode is 1'b1. Ref12 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg92 colmv ref13 base**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Sw_colmv_ref13_base Only valid when Sw_colmv_mode is 1'b1. Ref13 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg93 colmv ref14 base**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref14_base Only valid when Sw_colmv_mode is 1'b1. Ref14 frame colmv base addr. For H264 and HEVC.

**rkvdec swreg94 colmv ref15 base**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref15_base Only valid when Sw_colmv_mode is 1'b1. Ref15 frame colmv base addr. Only for HEVC.

**rkvdec swreg95 scanlist addr**

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Scanlist_addr Should be align to 16byte,and will be used For H264 and HEVC.
3:1	RO	0x0	Reserved
0	RW	0x0	Scanlist_addr_valid_en 1'b0: Scanlist addr get from pps table 1'b1: Scanlist addr get from config

**rkvdec swreg96 sd decout base**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_sd_decout_base Base address of decoder output picture The address should be 128bit align. In H264 decode format, the top field and bottom field are the same addr.

**rkvdec swreg97 sd y virstride**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31	RO	0x0	Sw_no_ref_bframe_dec 1'b1: Find this frame is not reference B frame
30:21	RO	0x000	Reserved
20:0	RW	0x0000000	Sw_sd_y_virstride The output picture y virtual stride (the unit is 128bit) The max: (4096x1.5 +128) x 2304 = 0xdc8000 We can know the Sw_uvout_base = Sw_decout_base + (Sw_y_virstride <<4).

**rkvdec swreg98 sd hor stride**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	Sw_sd_uv_hor_virstride Picture horizontal virtual stride (the unit is 128bit) The max is $(4096 \times 1.5 + 128) / 16 = 0x188$ Suggest this register to config to even for advance ddr performance.
15:10	RO	0x00	Reserved
9:0	RW	0x000	Sw_sd_y_hor_virstride Picture horizontal virtual stride (the unit is 128bit) The max is $(4096 \times 1.5 + 128) / 16 = 0x188$ Suggest this register to config to even for advance ddr performance.

**rkvdec\_swreg99\_qos\_ctrl**

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Sw_block_gating_en_l2 Every bits: 1'b0: Disable 1'b1: Enable auto gating
27:26	RW	0x0	Sw_axi_wr_hurry_level 2'b00: Hurry off 2'b01~2'b11: Hurry level
25:24	RW	0x0	Sw_axi_rd_hurry_level 2'b00: Hurry off 2'b01~2'b11: Hurry level
23:16	RW	0x00	Sw_bus2mc_buffer_qos_level Range is: 0~255 This value is means that Sw_bus2mc_buffer_qos_level <= left space, it will give hurry.
15:0	RW	0x0000	swreg_block_gating_e Block gating enable ctrl flag

**rkvdec\_swreg100\_PERF\_LATENCY\_CTRL0**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	Reserved
19:8	RW	0x000	Sw_rd_latency_thr Rd channel latency threshold
7:4	RW	0x0	Sw_rd_latency_id Rd channel id for performance test
3	RW	0x0	Sw_axi_cnt_type Sw_axi_cnt_type 1'b0: Axi transfer num count 1'b1: Ddr align transfer num count
2	RW	0x0	Sw_axi_perf_frm_type 1'b0: Clear by frame end 1'b1: Clear by software configuration
1	WO	0x0	Sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enable Clear pulse
0	RW	0x0	Sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

**rkvdec swreg101 PERF LATENCY CTRL1**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	Reserved
12	RW	0x0	Sw_rd_total_bytes_mode 1'b0: Cal all id 1'b1: Cal Sw_ar_count_id
11:8	RW	0x0	Sw_aw_count_id Sw_aw_count_id
7:4	RW	0x0	Sw_ar_count_id Sw_ar_count_id
3	RW	0x0	Sw_aw_cnt_id_type Sw_aw_cnt_id_type 1'b0: Count all wr-channels 1'b1: Count Sw_wr_cont_id wr-channel only
2	RW	0x0	Sw_ar_cnt_id_type Sw_ar_cnt_id_type 1'b0: Count all rd-channels 1'b1: Count Sw_ar_cont_id rd-channel only
1:0	RW	0x0	Sw_addr_align_type sw_addr_align_type 2'd0: 16 byte align 2'd1: 32byte align 2'd2: 64byte align 2'd3: 128byte align

**rkvdec swreg102 PERF RD MAX LATENCY NUM0**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15:0	RO	0x0000	Rd_max_latency_num_ch0 Read max latency value of channel 0

**rkvdec swreg103 PERF RD LATENCY SAMP NUM**

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Rd_latency_thr_num_ch0 Read latency thresod number channel 0

**rkvdec swreg104 PERF RD LATENCY ACC SUM**

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Rd_latency_acc_sum Total sample number

**rkvdec swreg105 PERF RD AXI TOTAL BYTE**

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Perf_rd_axi_total_byte The bandwidth of total read bytes

**rkvdec swreg106 PERF WR AXI TOTAL BYTE**

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Perf_wr_axi_total_byte The bandwidth of total write bytes

**rkvdec swreg107 PERF WORKING CNT**

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Perf_working_cnt The total running cycle of current frame

**rkvdec swreg108 qos1**

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_wr_wait_cycle_qos Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr, it will give hurry.

**rkvdec swreg112 sysctrl extra0**

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Sw_dec_mode_plus 8'd0: Avs2 8'd1: Av1 Other: Reverse Only sw_dec_mode=2'd3, such mode will be used.

**rkvdec swreg116 sw roi ctu offset st**

Address: Operational Base + offset (0x01d0)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_roi_error_ctu_cal_en 1'b0: Disable 1'b1: Enable
30:24	RO	0x00	Reserved
23:16	RW	0x00	Sw_roi_y_ctu_offset_st The start offset of ctu_y when roi check.
15:8	RO	0x00	Reserved
7:0	RW	0x00	Sw_roi_x_ctu_offset_st The start offset of ctu_x when roi check.

**rkvdec swreg117 sw roi ctu offset end**

Address: Operational Base + offset (0x01d4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:16	RW	0x00	Sw_roi_y_ctu_offset_end The end offset of ctu_y when roi check.
15:8	RO	0x00	Reserved
7:0	RW	0x00	Sw_roi_x_ctu_offset_end The end offset of ctu_x when roi check.

**rkvdec swreg118 sw error ctu ctu num in roi**

Address: Operational Base + offset (0x01d8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Sw_error_ctu_num_in_roi the error ctu num in roi

**13.6.10 VDPU345 CACHE Registers Summary**

Name	Offset	Size	Reset Value	Description
<u>pref cache VERSION</u>	0x0000	W	0xcac20101	VERSION register
<u>pref cache SIZE</u>	0x0004	W	0x07100206	L2 cache SIZE
<u>pref cache STATUS</u>	0x0008	W	0x00000000	Status register
<u>pref cache COMMAND</u>	0x0010	W	0x00000000	Command setting register
<u>pref cache CLEAR_PAGE</u>	0x0014	W	0x00000000	Clear page register
<u>pref cache MAX_READS</u>	0x0018	W	0x0000001c	Maximum read register
<u>pref cache ENABLE</u>	0x001c	W	0x00000003	Enables cacheable accesses and cache read allocation
<u>pref cache PERFCNT_SRC_0</u>	0x0020	W	0x00000000	Performance counter 0 source register
<u>pref cache PERFCNT_VAL0</u>	0x0024	W	0x00000000	Performance counter 0 value register
<u>pref cache PERFCNT_SRC_1</u>	0x0028	W	0x00000000	This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: Bad hit number, slave
<u>pref cache PERFCNT_VAL1</u>	0x002c	W	0x00000000	Performance counter 1 value register

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.11 VDP U345 CACHE Detail Registers Description

#### pref cache VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Minor version
15:8	RO	0x01	VERSION_MAJOR Major version
7:0	RO	0x01	VERSION_MINOR The id of product

#### pref cache SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x07	External_bus_width Log2 external bus width in bits
23:16	RO	0x10	CACHE_SIZE Log2 cache size in bytes For Y channel, its value is 0x10 For UV channel, its value is 0xf
15:8	RO	0x02	ASSOCIATIVITY Log2 associativity
7:0	RO	0x06	LINE_SIZE Log2 line size in bytes

**pref cache STATUS**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	DATA_BUSY Set when the cache is busy handling data.
0	RW	0x0	CMD_BUSY Set when the cache is busy handling commands.

**pref cache COMMAND**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	Reserved
5:4	RW	0x0	Sw_addrb_sel 2'b00: To sel b[14:6] 2'b01: To sel b[15:9], b[7:6] 2'b10: To sel b[16:10], b[7:6] 2'b11: To sel b[17:11], b[7:6]
3:0	RW	0x0	COMMAND 1'b1: Clear entire cache

**pref cache CLEAR PAGE**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE Writing an address, invalidates all lines in that page from the cache.

**pref cache MAX READS**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	Reserved
4:0	RW	0x1c	MAX_READS Limit the number of outstanding read transactions to this amount.

**pref cache ENABLE**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	Reserved
4	RW	0x0	Sw_cache_linsize 1'b0: The cache line is 32bytes 1'b1: The cache line is 64bytes
3	RW	0x0	Sw_cache_clk_disgate Cache clk disgate When it is 1'b0, enable cache clk auto clkgating When it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	Sw_readbuffer_counter_reject_en Default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: Normal origin counter reject
1	RW	0x1	Permit_cache_read_allocate 1'b1: Permit cache read allocate
0	RW	0x1	Permit_cacheable_access 1'b1: Permit cacheable access

**pref cache PERFCNT SRC0**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	Reserved
6:0	RW	0x00	PERFCNT_SRC0 This register holds all the possible source values for Performance Counter 0 0: Disabled 1: Total clock cycles 2: Active clock cycles 3: Read transactions, master 4: Word reads, master 5: Read transactions, slave 6: Word reads, slave 7: Read hit, slave 8: Read misses, slave 9: Read invalidates, slave 10: Cacheable read transactions, slave 11: Bad hit number, slave

**pref cache PERFCNT VAL0**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Performance counter 0 value

**pref cache PERFCNT SRC1**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x00000000	Reserved
6:0	RW	0x00	PERFCNT_SRC1 This register holds all the possible source values for Performance Counter 1 0: Disabled 1: Total clock cycles 2: Active clock cycles 3: Read transactions, master 4: Word reads, master 5: Read transactions, slave 6: Word reads, slave 7: Read hit, slave 8: Read misses, slave 9: Read invalidates, slave 10: Cacheable read transactions, slave 11: Bad hit number, slave

**pref cache PERFCNT VAL1**

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Performance counter 1 value

**13.6.12 VDP0345 MMU Registers Summary**



Name	Offset	Size	Reset Value	Description
<u>rkvdec mmu DTE ADDR</u>	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state
<u>rkvdec mmu STATUS</u>	0x0004	W	0x00000018	MMU status register
<u>rkvdec mmu COMMAND</u>	0x0008	W	0x00000000	MMU command register
<u>rkvdec mmu PAGE FAULT ADDR</u>	0x000c	W	0x00000000	MMU logical address of last page fault
<u>rkvdec mmu ZAP ONE LINE</u>	0x0010	W	0x00000000	MMU Zap cache line register
<u>rkvdec mmu INT RAWSTAT</u>	0x0014	W	0x00000000	MMU raw interrupt status register
<u>rkvdec mmu INT CLEAR</u>	0x0018	W	0x00000000	MMU raw interrupt status register
<u>rkvdec mmu INT MASK</u>	0x001c	W	0x00000000	MMU raw interrupt status register
<u>rkvdec mmu INT STATUS</u>	0x0020	W	0x00000000	MMU raw interrupt status register
<u>rkvdec mmu AUTO GATING</u>	0x0024	W	0x00000001	MMU auto gating

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.13 VDPU345 MMU Detail Registers Description

#### rkvdec mmu DTE ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR Mmu dte base addr , the address must be 4kb aligned

#### rkvdec mmu STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	Reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault.
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty.
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled.

**rkvdec mmu COMMAND**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	Reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

**rkvdec mmu PAGE\_FAULT\_ADDR**

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

**rkvdec mmu ZAP ONE LINE**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Address to be invalidated from the page table cache

**rkvdec mmu INT RAWSTAT**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

**rkvdec mmu INT CLEAR**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	WO	0x0	READ_BUS_ERROR Read bus error
0	WO	0x0	PAGE_FAULT Page fault

**rkvdec mmu INT MASK**

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error Enable an interrupt source if the corresponding mask bit is set to 1.
0	RW	0x0	PAGE_FAULT Page fault Enable an interrupt source if the corresponding mask bit is set to 1.

**rkvdec mmu INT STATUS**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RO	0x0	READ_BUS_ERROR Read bus error
0	RO	0x0	PAGE_FAULT Page fault

**rkvdec mmu AUTO GATING**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x1	Mmu_auto_gating When it is 1'b1, the mmu will auto gating itself.

**13.6.14 VDP345 LLP Registers Summary**

Name	Offset	Size	Reset Value	Description
rkvdec link swreg0 link mode irq	0x0000	W	0x00000000	The interrupt of LLP mode
rkvdec link swreg1 cfg start addr	0x0004	W	0x00000000	the address of register data
rkvdec link swreg2 link mode	0x0008	W	0x00000000	The LLP table add ctrl
rkvdec link swreg3 config done	0x000c	W	0x00000000	Config finish ctrl register
rkvdec link swreg4 decoded num	0x0010	W	0x00000000	The frame number which have been decoded
rkvdec link swreg5 dec total num	0x0014	W	0x00000000	The total needed decoder number
rkvdec link swreg6 link mode en	0x0018	W	0x00000000	LLP enable flag

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access**13.6.15 VDP345 LLP Detail Registers Description****rkvdec link swreg0 link mode irq**

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	Reserved
9	RW	0x0	rkvdec_irq_raw The irq of decoded
8	RW	0x0	Link_table_irq When high, decoder requests an interrupt. link table irq = Sw_dec_irq_raw && (Sw_dec_irq_dis == 1'b0)
7:3	RO	0x00	Reserved
2	RW	0x0	Sw_error_irq_dis 1'b0: If there are any error ,not matter Sw_dec_irq_dis ,it will give an interrupt. 1'b1: If it will give interrupt ,it only according to Sw_dec_irq_dis
1	RW	0x0	Cache_cfg_mode_sel 1'b0: Use rtl default value to config cache, ip will auto clr cache when it begin to start dec a frame. 1'b1: Use config in ddr to config cache .

**rkvdec link swreg1 cfg start addr**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	Reg_cfg_addr It should be align to 32 byte.

**rkvdec link swreg2 link mode**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Link_mode 1'b0: Normal mode,the first to start link mode 1'b1: Add extra ready frame to decoder
30	RO	0x0	Reserved
29:0	RW	0x00000000	Pre_frame_num 1'b1: Config 1 frame

**rkvdec link swreg3 config done**

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	WO	0x0	Config_done After config okay, config this bit to 1

**rkvdec link swreg4 decoded num**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	Decoder_error_flag 1'b0: No error 1'b1: Error, you will need to see swreg1 to check error type.
30	RO	0x0	Reserved
29:0	RO	0x00000000	Decoder_num The frame number which have been decoded

**rkvdec link swreg5 dec total num**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:0	RO	0x00000000	Dec_total_num The total needed decoder number

**rkvdec link swreg6 link mode en**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x0	Link_mode_en When error see by hw, it will auto reset to 0.

**13.6.16 VEPu54X LAYER1 Register Address Mapping**

The summary of LAYER1 register is listed below.

Table 13-10 VEPu LAYER1 Address Mapping

Name	Offset	Size	Reset Value	Description
<u>VEPU_VERSION</u>	0x0000	W	0x50600311	VEPU version. It contains IP function summary and sub-version informations.

Name	Offset	Size	Reset Value	Description
<u>VEPU_ENC_STRT</u>	0x0004	W	0x00000000	Start cmd register.(auto clock gating enable, auto reset enable and tmvp adjust enable when frame done are also allocated here.)
<u>VEPU_ENC_CLR</u>	0x0008	W	0x00000000	VEPU clear register
<u>VEPU_LKT_ADDR</u>	0x000C	W	0x00000000	Link table
<u>VEPU_INT_EN</u>	0x0010	W	0x00000000	VEPU interrupt enable
<u>VEPU_INT_MSK</u>	0x0014	W	0x00000000	VEPU interrupt mask
<u>VEPU_INT_CLR</u>	0x0018	W	0x00000000	VEPU interrupt clear
<u>VEPU_INT_STA</u>	0x001C	W	0x00000000	VEPU interrupt state
<u>VEPU_ENC_RSL</u>	0x0030	W	0x00000000	Resolution
<u>VEPU_ENC_PIC</u>	0x0034	W	0x00000000	VEPU common configuration
<u>VEPU_ENC_WDG</u>	0x0038	W	0x00000000	VEPU watch dog configure register
<u>VEPU_DTRNS_MAP</u>	0x003C	W	0x00000000	Data transaction mapping (endian and order)
<u>VEPU_DTRNS_CFG</u>	0x0040	W	0x00000000	(AXI bus) Data transaction configuration
<u>VEPU_SRC_FMT</u>	0x0044	W	0x00000000	Video source format
<u>VEPU_SRC_UDFY</u>	0x0048	W	0x00000000	Weight of user defined formula for RGB to Y conversion
<u>VEPU_SRC_UDFU</u>	0x004C	W	0x00000000	Weight of user defined formula for RGB to U conversion
<u>VEPU_SRC_UDFV</u>	0x0050	W	0x00000000	Weight of user defined formula for RGB to V conversion
<u>VEPU_SRC_UDFO</u>	0x0054	W	0x00000000	Offset of user defined formula for RGB to YUV conversion
<u>VEPU_SRC_PROC</u>	0x0058	W	0x00000000	Video source process
<u>VEPU_KLUT_OFST</u>	0x0064	W	0x00000000	Offset of (RDO) chroma cost weight table
<u>VEPU_KLUT_WGT0</u>	0x0068	W	0x00000000	(RDO) Chroma weight table configure register0
<u>VEPU_KLUT_WGT1</u>	0x006C	W	0x00000000	(RDO) Chroma weight table configure register1
<u>VEPU_KLUT_WGT2</u>	0x0070	W	0x00000000	(RDO) Chroma weight table configure register2
<u>VEPU_KLUT_WGT3</u>	0x0074	W	0x00000000	(RDO) Chroma weight table configure register3
<u>VEPU_KLUT_WGT4</u>	0x0078	W	0x00000000	(RDO) Chroma weight table configure register4
<u>VEPU_KLUT_WGT5</u>	0x007C	W	0x00000000	(RDO) Chroma weight table configure register5
<u>VEPU_KLUT_WGT6</u>	0x0080	W	0x00000000	(RDO) Chroma weight table configure register6
<u>VEPU_KLUT_WGT7</u>	0x0084	W	0x00000000	(RDO) Chroma weight table configure register7
<u>VEPU_KLUT_WGT8</u>	0x0088	W	0x00000000	(RDO) Chroma weight table configure register8
<u>VEPU_KLUT_WGT9</u>	0x008C	W	0x00000000	(RDO) Chroma weight table configure register9
<u>VEPU_KLUT_WGT10</u>	0x0090	W	0x00000000	(RDO) Chroma weight table configure register10

Name	Offset	Size	Reset Value	Description
<u>VEPU_KLUT_WGT11</u>	0x0094	W	0x00000000	(RDO) Chroma weight table configure register11
<u>VEPU_KLUT_WGT12</u>	0x0098	W	0x00000000	(RDO) Chroma weight table configure register12
<u>VEPU_KLUT_WGT13</u>	0x009C	W	0x00000000	(RDO) Chroma weight table configure register13
<u>VEPU_KLUT_WGT14</u>	0x00A0	W	0x00000000	(RDO) Chroma weight table configure register14
<u>VEPU_KLUT_WGT15</u>	0x00A4	W	0x00000000	(RDO) Chroma weight table configure register15
<u>VEPU_KLUT_WGT16</u>	0x00A8	W	0x00000000	(RDO) Chroma weight table configure register16
<u>VEPU_KLUT_WGT17</u>	0x00AC	W	0x00000000	(RDO) Chroma weight table configure register17
<u>VEPU_KLUT_WGT18</u>	0x00B0	W	0x00000000	(RDO) Chroma weight table configure register18
<u>VEPU_KLUT_WGT19</u>	0x00B4	W	0x00000000	(RDO) Chroma weight table configure register19
<u>VEPU_KLUT_WGT20</u>	0x00B8	W	0x00000000	(RDO) Chroma weight table configure register20
<u>VEPU_KLUT_WGT21</u>	0x00BC	W	0x00000000	(RDO) Chroma weight table configure register21
<u>VEPU_KLUT_WGT22</u>	0x00C0	W	0x00000000	(RDO) Chroma weight table configure register22
<u>VEPU_KLUT_WGT23</u>	0x00C4	W	0x00000000	(RDO) Chroma weight table configure register23
<u>VEPU_RC_CFG</u>	0x00C8	W	0x00000000	Rate control configuration
<u>VEPU_RC_QP</u>	0x00CC	W	0x00000000	QP configuration for rate control
<u>VEPU_RC_TGT</u>	0x00D0	W	0x00000000	The target bit rate for rate control
<u>VEPU_RC_ADJ0</u>	0x00D4	W	0x00000000	QP adjust configuration for rate control
<u>VEPU_RC_ADJ1</u>	0x00D8	W	0x00000000	QP adjust configuration for rate control
<u>VEPU_RC_DTHD0</u>	0x00DC	W	0x00000000	Bits rate deviation threshold0
<u>VEPU_RC_DTHD1</u>	0x00E0	W	0x00000000	Bits rate deviation threshold1
<u>VEPU_RC_DTHD2</u>	0x00E4	W	0x00000000	Bits rate deviation threshold2
<u>VEPU_RC_DTHD3</u>	0x00E8	W	0x00000000	Bits rate deviation threshold3
<u>VEPU_RC_DTHD4</u>	0x00EC	W	0x00000000	Bits rate deviation threshold4
<u>VEPU_RC_DTHD5</u>	0x00F0	W	0x00000000	Bits rate deviation threshold5
<u>VEPU_RC_DTHD6</u>	0x00F4	W	0x00000000	Bits rate deviation threshold6
<u>VEPU_RC_DTHD7</u>	0x00F8	W	0x00000000	Bits rate deviation threshold7
<u>VEPU_RC_DTHD8</u>	0x00FC	W	0x00000000	Bits rate deviation threshold8
<u>VEPU_ROI_QTHD0</u>	0x0100	W	0x00000000	ROI QP threshold configuration0
<u>VEPU_ROI_QTHD1</u>	0x0104	W	0x00000000	ROI QP threshold configuration1
<u>VEPU_ROI_QTHD2</u>	0x0108	W	0x00000000	ROI QP threshold configuration2
<u>VEPU_ROI_QTHD3</u>	0x010C	W	0x00000000	ROI QP threshold configuration3
<u>VEPU_PIC_OFST</u>	0x0110	W	0x00000000	Encoding picture offset
<u>VEPU_SRC_STRD</u>	0x0114	W	0x00000000	Video source stride
<u>VEPU_ADR_SRC0</u>	0x0118	W	0x00000000	Base address of the 1st storage area for video source
<u>VEPU_ADR_SRC1</u>	0x011C	W	0x00000000	Base address of the 2nd storage area for video source

Name	Offset	Size	Reset Value	Description
<u>VEPU_ADR_SRC2</u>	0x0120	W	0x00000000	Base address of the 3rd storage area for video source
<u>VEPU_ADR_ROI</u>	0x0124	W	0x00000000	Base address for ROI configuration, 16 bytes aligned
<u>VEPU_ADR_RFPW_H</u>	0x0128	W	0x00000000	Base address of header_block for compressed reference frame write, 4K bytes aligned
<u>VEPU_ADR_RFPW_B</u>	0x012C	W	0x00000000	Base address of body_block for compressed reference frame write, 4K bytes aligned
<u>VEPU_ADR_RFPR_H</u>	0x0130	W	0x00000000	Base address of header_block for compressed reference frame read, 4K bytes aligned
<u>VEPU_ADR_RFPR_B</u>	0x0134	W	0x00000000	Base address of body_block for compressed reference frame read, 4K bytes aligned
<u>VEPU_ADR_CMVW</u>	0x0138	W	0x00000000	Base address for col-located Mv write, 1KB aligned, HEVC only
<u>VEPU_ADR_CMVR</u>	0x013C	W	0x00000000	Base address for col-located Mv read, 1KB aligned, HEVC only
<u>VEPU_ADR_DSPW</u>	0x0140	W	0x00000000	Base address for down-sampled reference frame write, 1KB aligned
<u>VEPU_ADR_DSPR</u>	0x0144	W	0x00000000	Base address for down-sampled reference frame read, 1KB aligned
<u>VEPU_ADR_MEIW</u>	0x0148	W	0x00000000	Base address for ME information write, 1KB aligned
<u>VEPU_ADR_BSBT</u>	0x014C	W	0x00000000	Top address of bit stream buffer, 128B aligned
<u>VEPU_ADR_BSBB</u>	0x0150	W	0x00000000	Bottom address of bit stream buffer, 128B aligned
<u>VEPU_ADR_BSBR</u>	0x0154	W	0x00000000	Read address of bit stream buffer, 128B aligned
<u>VEPU_ADR_BSBS</u>	0x0158	W	0x00000000	Start address of bit stream buffer
<u>VEPU_SLI_SPLT</u>	0x015C	W	0x00000000	Slice split configuration
<u>VEPU_SLI_BYTE</u>	0x0160	W	0x00000000	Number of bytes for slice split
<u>VEPU_ME_RNGE</u>	0x0164	W	0x00000000	Motion estimation range
<u>VEPU_ME_CFG</u>	0x0168	W	0x00000000	Motion estimation configuration
<u>VEPU_ME_CACH</u>	0x016C	W	0x00000000	ME cache configuration
<u>VEPU_SYNT_LONG_REFM_0</u>	0x0170	W	0x00000000	Long term reference frame mark0 for HEVC
<u>VEPU_SYNT_LONG_REFM_1</u>	0x0174	W	0x00000000	Long term reference frame mark1 for HEVC
<u>VEPU_IPRD_CSTS</u>	0x0194	W	0x00000000	Cost function configuration for intra prediction
<u>VEPU_RDO_CFG_H264</u>	0x0198	W	0x00000000	H.264 RDO configuration, share address with HEVC
<u>VEPU_RDO_CFG_HEVC</u>	0x0198	W	0x00000000	HEVC RDO configuration, share address with H.264
<u>VEPU_SYNT_NAL_H264</u>	0x019C	W	0x00000000	NAL configuration for H.264, share address with HEVC
<u>VEPU_SYNT_NAL_HEVC</u>	0x019C	W	0x00000000	NAL configuration for HEVC, share address with H.264

Name	Offset	Size	Reset Value	Description
<u>VEPU_SYNT_SPS_H264</u>	0x01A0	W	0x00000000	Sequence parameter set syntax configuration for H.264, share address with HEVC
<u>VEPU_SYNT_SPS_HEVC</u>	0x01A0	W	0x00000000	Sequence parameter set syntax configuration for HEVC, share address with H.264
<u>VEPU_SYNT_PPS_H264</u>	0x01A4	W	0x00000000	Picture parameter set configuration for H.264, share address with HEVC
<u>VEPU_SYNT_PPS_HEVC</u>	0x01A4	W	0x00000000	Picture parameter set configuration for HEVC, share address with H.264
<u>VEPU_SYNT_SLI0_H264</u>	0x01A8	W	0x00000000	Slice header configuration0 for H.264, share address with HEVC
<u>VEPU_SYNT_SLI0_HEVC</u>	0x01A8	W	0x00000000	Slice header configuration0 for HEVC, share address with H.264
<u>VEPU_SYNT_SLI1_H264</u>	0x01AC	W	0x00000000	Slice header configuration1 for H.264, share address with HEVC
<u>VEPU_SYNT_SLI1_HEVC</u>	0x01AC	W	0x00000000	Slice header configuration1 for HEVC, share address with H.264
<u>VEPU_SYNT_SLI2_H264</u>	0x01B0	W	0x00000000	Slice header configuration2 for H.264, share address with HEVC
<u>VEPU_SYNT_SLI2_HEVC</u>	0x01B0	W	0x00000000	Slice header configuration2 for HEVC, share address with H.264
<u>VEPU_SYNT_REFM0_H264</u>	0x01B4	W	0x00000000	Reference frame mark0 for H.264, share address with HEVC
<u>VEPU_SYNT_REFM0_HEVC</u>	0x01B4	W	0x00000000	Reference frame mark0 for HEVC, share address with H.264
<u>VEPU_SYNT_REFM1_H264</u>	0x01B8	W	0x00000000	Reference frame mark1 for H.264, share address with HEVC
<u>VEPU_SYNT_REFM1_HEVC</u>	0x01B8	W	0x00000000	Reference frame mark1 for HEVC, share address with H.264
<u>VEPU_OSD_CFG</u>	0x01C0	W	0x00000000	OSD configuration
<u>VEPU_OSD_INV</u>	0x01C4	W	0x00000000	OSD color inverse configuration
<u>VEPU_SYNT_REFM2</u>	0x01C8	W	0x00000000	Reference frame mark2 for HEVC
<u>VEPU_SYNT_REFM2_H264</u>	0x01C8	W	0x00000000	Reference frame mark2 for H264
<u>VEPU_SYNT_REFM3</u>	0x01CC	W	0x00000000	Reference frame mark3 for HEVC
<u>VEPU_OSD0_POS</u>	0x01D0	W	0x00000000	OSD region0 position
<u>VEPU_OSD1_POS</u>	0x01D4	W	0x00000000	OSD region1 position
<u>VEPU_OSD2_POS</u>	0x01D8	W	0x00000000	OSD region2 position
<u>VEPU_OSD3_POS</u>	0x01DC	W	0x00000000	OSD region3 position
<u>VEPU_OSD4_POS</u>	0x01E0	W	0x00000000	OSD region4 position
<u>VEPU_OSD5_POS</u>	0x01E4	W	0x00000000	OSD region5 position
<u>VEPU_OSD6_POS</u>	0x01E8	W	0x00000000	OSD region6 position
<u>VEPU_OSD7_POS</u>	0x01EC	W	0x00000000	OSD region7 position
<u>VEPU_ADR_OSD0</u>	0x01F0	W	0x00000000	Base address for OSD region0, 16B aligned
<u>VEPU_ADR_OSD1</u>	0x01F4	W	0x00000000	Base address for OSD region1, 16B aligned
<u>VEPU_ADR_OSD2</u>	0x01F8	W	0x0	Base address for OSD region2, 16B aligned
<u>VEPU_ADR_OSD3</u>	0x01FC	W	0x00000000	Base address for OSD region3, 16B aligned



Name	Offset	Size	Reset Value	Description
<u>VEPU_ADR_OSD4</u>	0x0200	W	0x00000000	Base address for OSD region4, 16B aligned
<u>VEPU_ADR_OSD5</u>	0x0204	W	0x00000000	Base address for OSD region5, 16B aligned
<u>VEPU_ADR_OSD6</u>	0x0208	W	0x00000000	Base address for OSD region6, 16B aligned
<u>VEPU_ADR_OSD7</u>	0x020C	W	0x00000000	Base address for OSD region7, 16B aligned
<u>VEPU_ST_BSL</u>	0x0210	W	0x00000000	Bit stream length for current frame
<u>VEPU_ST_SSE_L32</u>	0x0214	W	0x00000000	Low 32 bits of encoding distortion (SSE)
<u>VEPU_ST_SSE_QP</u>	0x0218	W	0x00000000	High 8 bits of encoding distortion (SSE) and sum of QP for the encoded frame
<u>VEPU_ST_SAO</u>	0x021C	W	0x00000000	Number of CTUs which adjusted by SAO
<u>VEPU_ST_ENC</u>	0x0228	W	0x00000000	VEPU working status
<u>VEPU_ST_LKT</u>	0x022C	W	0x00000000	Status of link table mode encoding
<u>VEPU_ST_NADR</u>	0x0230	W	0x00000000	Address of the processing link table node
<u>VEPU_ST_BSB</u>	0x0234	W	0x00000000	Status of bit stream buffer
<u>VEPU_ST_BUS</u>	0x0238	W	0x00000000	VEPU bus status
<u>VEPU_ST_SNUM</u>	0x023C	W	0x00000000	Slice number status
<u>VEPU_ST_SLEN</u>	0x0240	W	0x00000000	Status of slice length
<u>VEPU_ST_PNUM_P64</u>	0x0244	W	0x00000000	Number of 64x64 inter predicted blocks
<u>VEPU_ST_PNUM_P32</u>	0x0248	W	0x00000000	Number of 32x32 inter predicted blocks
<u>VEPU_ST_PNUM_P16</u>	0x024C	W	0x00000000	Number of 16x16 inter predicted blocks
<u>VEPU_ST_PNUM_P8</u>	0x0250	W	0x00000000	Number of 8x8 inter predicted blocks
<u>VEPU_ST_PNUM_I32</u>	0x0254	W	0x00000000	Number of 32x32 intra predicted blocks
<u>VEPU_ST_PNUM_I16</u>	0x0258	W	0x00000000	Number of 16x16 intra predicted blocks
<u>VEPU_ST_PNUM_I8</u>	0x025C	W	0x00000000	Number of 8x8 intra predicted blocks
<u>VEPU_ST_PNUM_I4</u>	0x0260	W	0x00000000	Number of 4x4 intra predicted blocks
<u>VEPU_ST_B8_QP0</u>	0x0264	W	0x00000000	Number of block8x8s with QP=0
<u>VEPU_ST_B8_QP1</u>	0x0268	W	0x00000000	Number of block8x8s with QP=1
<u>VEPU_ST_B8_QP2</u>	0x026C	W	0x00000000	Number of block8x8s with QP=2
<u>VEPU_ST_B8_QP3</u>	0x0270	W	0x00000000	Number of block8x8s with QP=3
<u>VEPU_ST_B8_QP4</u>	0x0274	W	0x00000000	Number of block8x8s with QP=4
<u>VEPU_ST_B8_QP5</u>	0x0278	W	0x00000000	Number of block8x8s with QP=5
<u>VEPU_ST_B8_QP6</u>	0x027C	W	0x00000000	Number of block8x8s with QP=6
<u>VEPU_ST_B8_QP7</u>	0x0280	W	0x00000000	Number of block8x8s with QP=7
<u>VEPU_ST_B8_QP8</u>	0x0284	W	0x00000000	Number of block8x8s with QP=8
<u>VEPU_ST_B8_QP9</u>	0x0288	W	0x00000000	Number of block8x8s with QP=9
<u>VEPU_ST_B8_QP10</u>	0x028C	W	0x00000000	Number of block8x8s with QP=10

Name	Offset	Size	Reset Value	Description
VEPU ST B8 QP11	0x0290	W	0x00000000	Number of block8x8s with QP=11
VEPU ST B8 QP12	0x0294	W	0x00000000	Number of block8x8s with QP=12
VEPU ST B8 QP13	0x0298	W	0x00000000	Number of block8x8s with QP=13
VEPU ST B8 QP14	0x029C	W	0x00000000	Number of block8x8s with QP=14
VEPU ST B8 QP15	0x02A0	W	0x00000000	Number of block8x8s with QP=15
VEPU ST B8 QP16	0x02A4	W	0x00000000	Number of block8x8s with QP=16
VEPU ST B8 QP17	0x02A8	W	0x00000000	Number of block8x8s with QP=17
VEPU ST B8 QP18	0x02AC	W	0x00000000	Number of block8x8s with QP=18
VEPU ST B8 QP19	0x02B0	W	0x00000000	Number of block8x8s with QP=19
VEPU ST B8 QP20	0x02B4	W	0x00000000	Number of block8x8s with QP=20
VEPU ST B8 QP21	0x02B8	W	0x00000000	Number of block8x8s with QP=21
VEPU ST B8 QP22	0x02BC	W	0x00000000	Number of block8x8s with QP=22
VEPU ST B8 QP23	0x02C0	W	0x00000000	Number of block8x8s with QP=23
VEPU ST B8 QP24	0x02C4	W	0x00000000	Number of block8x8s with QP=24
VEPU ST B8 QP25	0x02C8	W	0x00000000	Number of block8x8s with QP=25
VEPU ST B8 QP26	0x02CC	W	0x00000000	Number of block8x8s with QP=26
VEPU ST B8 QP27	0x02D0	W	0x00000000	Number of block8x8s with QP=27
VEPU ST B8 QP28	0x02D4	W	0x00000000	Number of block8x8s with QP=28
VEPU ST B8 QP29	0x02D8	W	0x00000000	Number of block8x8s with QP=29
VEPU ST B8 QP30	0x02DC	W	0x00000000	Number of block8x8s with QP=0
VEPU ST B8 QP31	0x02E0	W	0x00000000	Number of block8x8s with QP=31
VEPU ST B8 QP32	0x02E4	W	0x00000000	Number of block8x8s with QP=32
VEPU ST B8 QP33	0x02E8	W	0x00000000	Number of block8x8s with QP=33
VEPU ST B8 QP34	0x02EC	W	0x00000000	Number of block8x8s with QP=34
VEPU ST B8 QP35	0x02F0	W	0x00000000	Number of block8x8s with QP=35
VEPU ST B8 QP36	0x02F4	W	0x00000000	Number of block8x8s with QP=36
VEPU ST B8 QP37	0x02F8	W	0x00000000	Number of block8x8s with QP=37
VEPU ST B8 QP38	0x02FC	W	0x00000000	Number of block8x8s with QP=38
VEPU ST B8 QP39	0x0300	W	0x00000000	Number of block8x8s with QP=39
VEPU ST B8 QP40	0x0304	W	0x00000000	Number of block8x8s with QP=40
VEPU ST B8 QP41	0x0308	W	0x00000000	Number of block8x8s with QP=41
VEPU ST B8 QP42	0x030C	W	0x00000000	Number of block8x8s with QP=42
VEPU ST B8 QP43	0x0310	W	0x00000000	Number of block8x8s with QP=43
VEPU ST B8 QP44	0x0314	W	0x00000000	Number of block8x8s with QP=44
VEPU ST B8 QP45	0x0318	W	0x00000000	Number of block8x8s with QP=45
VEPU ST B8 QP46	0x031C	W	0x00000000	Number of block8x8s with QP=46
VEPU ST B8 QP47	0x0320	W	0x00000000	Number of block8x8s with QP=47
VEPU ST B8 QP48	0x0324	W	0x00000000	Number of block8x8s with QP=48
VEPU ST B8 QP49	0x0328	W	0x00000000	Number of block8x8s with QP=49
VEPU ST B8 QP50	0x032C	W	0x00000000	Number of block8x8s with QP=50
VEPU ST B8 QP51	0x0330	W	0x00000000	Number of block8x8s with QP=51
VEPU ST CPLX TMP	0x0334	W	0x00000000	Temporal complexity(MADP) for current encoding and reference frame

Name	Offset	Size	Reset Value	Description
<u>VEPU_ST_BNUM_CME</u>	0x0338	W	0x00000000	Number of CME blocks in frame. H.264: number CME blocks (4 MBs) in 16x64 aligned extended frame, except for the CME blocks configured as force intra. HEVC: number CME blocks (CTU) in 64x64 aligned extended frame, except for the CME blocks configured as force intra.
<u>VEPU_ST_CPLX_SPT</u>	0x033C	W	0x00000000	Spatial complexity(MADI) for current encoding frame
<u>VEPU_ST_BNUM_B16</u>	0x0340	W	0x00000000	Number of 16x16 blocks in frame. H.264: number of macro-blocks in encoding frame. HEVC: number of 16x16 blocks in 16x16 aligned extended frame.
<u>VEPU_L2CFG_ADDR</u>	0x03F0	W	0x00000000	Level2 configuration address
<u>VEPU_L2CFG_WDATA</u>	0x03F4	W	0x00000000	L2 configuration write data
<u>VEPU_L2CFG_RDATA</u>	0x03F8	W	0x00000000	L2 configuration read data
<u>VEPU_OSD_PLT0</u>	0x0400	W	0x00000000	User defined OSD palette color0
<u>VEPU_OSD_PLT1</u>	0x0404	W	0x00000000	User defined OSD palette color1
<u>VEPU_OSD_PLT255</u>	0x07FC	W	0x00000000	OSD palette color255
<u>VEPU_ST_WDG</u>	0x085C	W	0x00000000	VEPU watch dog status
<u>VEPU_ST_PPL</u>	0x0860	W	0x00000000	VEPU pipe line status
<u>VEPU_ST_SLI_NUM</u>	0x0874	W	0x00000000	Number of slices
<u>VEPU_DBG_DMA_RFPR</u>	0x08E4	W	0x00000000	Debug register for DMA RFPR channel
<u>VEPU_DBG_DMA_CH_ST</u>	0x08E8	W	0x00000000	Debug register for DMA status
<u>VEPU_MMU0_ADDR</u>	0x0F00	W	0x00000000	Page table address for AXI0 MMU
<u>VEPU_MMU0_ST</u>	0x0F04	W	0x00000000	Status of the MMU for AXI0
<u>VEPU_MMU0_CMD</u>	0x0F08	W	0x00000000	MMU command for AXI0
<u>VEPU_MMU0_PFA</u>	0x0F0C	W	0x00000000	Address of the last page fault for MMU0
<u>VEPU_MMU0_ZAP</u>	0x0F10	W	0x00000000	Zap address for MMU0
<u>VEPU_MMU0_ERR</u>	0x0F14	W	0x00000000	MMU error
<u>VEPU_MMU0_INT_CLR</u>	0x0F18	W	0x00000000	Interrupt clear for MMU0
<u>VEPU_MMU0_INT_MSK</u>	0x0F1C	W	0x00000000	Interrupt mask for MMU0
<u>VEPU_MMU0_INT_STA</u>	0x0F20	W	0x00000000	Interrupt status for MMU0
<u>VEPU_MMU0_ACKG</u>	0x0F24	W	0x00000000	Auto clock gating for MMU0
<u>VEPU_MMU1_ADDR</u>	0x0F40	W	0x00000000	Page table address for AXI1 MMU
<u>VEPU_MMU1_ST</u>	0x0F44	W	0x00000000	Status of the MMU for AXI1
<u>VEPU_MMU1_CMD</u>	0x0F48	W	0x00000000	MMU command for AXI1
<u>VEPU_MMU1_PFA</u>	0x0F4C	W	0x00000000	Address of the last page fault for MMU1
<u>VEPU_MMU1_ZAP</u>	0x0F50	W	0x00000000	Zap address for MMU1
<u>VEPU_MMU1_ERR</u>	0x0F54	W	0x00000000	MMU error
<u>VEPU_MMU1_INT_CLR</u>	0x0F58	W	0x00000000	Interrupt clear for MMU1
<u>VEPU_MMU1_INT_MSK</u>	0x0F5C	W	0x00000000	Interrupt mask for MMU1
<u>VEPU_MMU1_INT_STA</u>	0x0F60	W	0x00000000	Interrupt status for MMU1
<u>VEPU_MMU1_ACKG</u>	0x0F64	W	0x00000000	Auto clock gating for MMU1

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.17 VEPUS4X LAYER1 Detail Register Description

#### VEPU\_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x50	ip_id VEPU ID. It is constant 0x50.
23	RO	0x0	reserved
22:21	RO	0x3	fbf_cap FBC capability: 2'h0: No FBC 2'h3: Support AFBC for video source and FBC for reconstructed picture Others: Reserved
20	RO	0x0	bfrm_cap B frame encoding capability. 1 means VEPu supports B frame encoding while 0 means not.
19:18	RO	0x0	filtr_cap Pre-process filter capability 2'h0: Basic pre-process filter 2'h3: No pre-process filter Others: Reserved
17:16	RO	0x0	osd_cap OSD capability. 2'h0: 8-area OSD with 256-color palette 2'h3: No OSD Others: Reserved
15:12	RO	0x0	res_cap Max resolution 4'h0: 4096x2304 4'h1: 1920x1088 Others: Reserved
11:10	RO	0x0	reserved
9	RO	0x1	hevc_cap HEVC encoding capability. 1 means VEPu supports HEVC encoding while 0 means not
8	RO	0x1	h264_cap H.264 encoding capability. 1 means VEPu supports H.264 encoding, while 0 means not.
7:0	RO	0x11	sub_ver VEPU sub-version. 0x11 for PUMA

**VEPU\_ENC\_STRT**

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	enc_done_tmvp_en Enc_done need wait tmvp write done by dma.
17	RW	0x0	resetrn_hw_en Encoder auto reset core clock domain when frame finished.
16	RW	0x0	cke VEPU auto clock gating enable
15:10	RO	0x00	reserved
9:8	RW	0x0	vepu_cmd VEPU command: 2'h0: N/A 2'h1: One frame encoding by register configuration 2'h2: Multi-frame encoding start with link table mode 2'h3: Multi-frame encoding update (with link table mode)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	lkt_num Number of new nodes in link table. only for link table mode.

**VEPU\_ENC\_CLR**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	force_clr Force clear. Clear all sub-modules besides regfile and AHB data path.
0	R/W SC	0x0	safe_clr Safe clr. It only clears DMA module to confirm AXI transaction integrity. 1'h0: Safe clear is not performing. 1'h1: Safe clear is performing.

**VEPU\_LKT\_ADDR**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	lkt_addr High 28 bits of the address for the first node in link table.
3:0	RO	0x0	reserved

**VEPU\_INT\_EN**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x00000000	reserved
8	RW	0x0	wdg_en Watch dog(time out) interrupt enable.
7	RW	0x0	rbus_err_en AXI read channel error interrupt enable.
6	RW	0x0	wbus_err_en AXI write channel error interrupt enable.
5	RW	0x0	brsp_otsd_en AXI write response outstanding overflow interrupt enable.
4	RW	0x0	bsf_oflw_en Bit stream buffer overflow enable.
3	RW	0x0	slc_done_en One slice encoding finish interrupt enable.
2	RW	0x0	sclr_done_en Safe clear finish interrupt enable.
1	RW	0x0	lkt_done_en Link table (node) finish interrupt enable.
0	RW	0x0	enc_done_en One frame encoding finish interrupt enable.

**VEPU\_INT\_MSK**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x00000000	reserved
8	RW	0x0	wdg_msk Watch dog(time out) interrupt mask.
7	RW	0x0	rbus_err_msk AXI read channel error interrupt mask.

Bit	Attr	Reset Value	Description
6	RW	0x0	wbus_err_msk AXI write channel error interrupt mask.
5	RW	0x0	brsp_otsd_msk AXI write response outstanding overflow interrupt mask.
4	RW	0x0	bsf_oflw_msk Bit stream buffer overflow mask.
3	RW	0x0	slc_done_msk One slice encoding finish interrupt mask.
2	RW	0x0	sclr_done_msk Safe clear finish interrupt mask.
1	RW	0x0	lkt_done_msk Link table (node) finish interrupt mask.
0	RW	0x0	enc_done_msk One frame encoding finish interrupt mask.

**VEPU\_INT\_CLR**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	W1 C	0x0	wdg_clr Watch dog(time out) interrupt clear.
7	W1 C	0x0	rbus_err_clr AXI read channel error interrupt clear.
6	W1 C	0x0	wbus_err_clr AXI write channel error interrupt clear.
5	W1 C	0x0	brsp_otsd_clr AXI write response outstanding overflow interrupt clear.
4	W1 C	0x0	bsf_oflw_clr Bit stream buffer overflow clear.
3	W1 C	0x0	slc_done_clr One slice encoding finish interrupt clear.
2	W1 C	0x0	sclr_done_clr Safe clear finish interrupt clear.
1	W1 C	0x0	lkt_done_clr Link table (node) finish interrupt clear.
0	W1 C	0x0	enc_done_clr One frame encoding finish interrupt clear.

**VEPU\_INT\_STA**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	wdg_sta Watch dog(time out) interrupt status.
7	RO	0x0	rbus_err_sta AXI read channel error interrupt status.
6	RO	0x0	wbus_err_sta AXI write channel error interrupt status.
5	RO	0x0	brsp_otsd_sta AXI write response outstanding overflow interrupt status.
4	RO	0x0	bsf_oflw_sta Bit stream buffer overflow status.
3	RO	0x0	slc_done_sta One slice encoding finish interrupt status.

Bit	Attr	Reset Value	Description
2	RO	0x0	sclr_done_sta Safe clear finish interrupt status.
1	RO	0x0	lkt_done_sta Link table (node) finish interrupt status.
0	RO	0x0	enc_done_sta One frame encoding finish interrupt status.

**VEPU\_ENC\_RSL**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	pic_hfill Filling pixels to keep (encoding) picture height is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.
25	RO	0x0	reserved
24:16	RW	0x000	pic_hd8_m1 Ceil(encoding picture height/8) -1
15:10	RW	0x00	pic_wfill Filling pixels to keep (encoding) picture width is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.
9	RO	0x0	reserved
8:0	RW	0x000	pic_wd8_m1 Ceil(encoding picture width/8) -1

**VEPU\_ENC\_PIC**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	node_int Node interrupt enable (only for link table node configuration).
30	RW	0x0	slen_fifo Slice length fifo enable.
29	RW	0x0	satd_byps_en RDO intra-prediction satd path bypass enable.
28	RW	0x0	dchs_rxe Dual-core handshake rx enable.
27:26	RW	0x0	dchs_txid Dual-core handshake tx ID.
25:24	RW	0x0	dchs_rxid Dual-core handshake Rx ID.
23	RW	0x0	atr_thd_sel 1'h0: Select atr_thd group 1'h1: Select atr_thd group1
22:19	RW	0x0	log2_ctu_num Logarithm of bit width to express ctu number in current picture, HEVC only.
18:14	RW	0x00	num_pic_tot_cur NumPicTotalCurr for HEVC reference picture list modification.
13:8	RW	0x00	pic_qp QP value for current frame encoding.
7:6	RO	0x0	reserved
5	RW	0x0	rdo_wgt_sel Select the group of RDO weight parameters(VEPU2_RDO_WGTA_QP* and VEP2_RDO_WGTB*). 1'h0: Select weight group A (VEPU2_RDO_WGTA_QP*) 1'h1: Select weight group B(VEPU2_RDO_WGTB_QP*)

Bit	Attr	Reset Value	Description
4	RW	0x0	bs_scp Output start code prefix.
3	RW	0x0	mei_stor Output ME(motion estimation) information.
2	RW	0x0	cur_frm_ref Current frame should be referenced in future.
1	RW	0x0	roi_en ROI(region of interest) encoding enable.
0	RW	0x0	enc_std Video standard. 1'h0: H.264 encoding 1'h1: HEVC encoding

**VEPU\_ENC\_WDG**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rfp_load_thd Reference picture loading timeout threshold. 8'h0: No time limit 8'hx: x*256 core clock cycles
23:0	RW	0x000000	vs_load_thd Video source loading timeout threshold. 24'h0: No time limit 24'hx: x*256 core clock cycles

**VEPU\_DTRNS\_MAP**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	afbc_bsize AFBC video source loading burst size. 1'h0: 32 bytes 1'h1: 64 bytes
26:23	RW	0x0	lktw_bus_edin Data swap for link table write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
22:19	RW	0x0	roir_bus_edin Data swap for ROI configuration read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
18:15	RW	0x0	lktr_bus_edin Data swap for link table read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits



Bit	Attr	Reset Value	Description
14:12	RW	0x0	bsw_bus_edin Data swap for bis stream write channel. [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
11:8	RW	0x0	meiw_bus_edin Data swap for ME information write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
7:4	RW	0x0	src_bus_edin Data swap for video source loading channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
3	RW	0x0	rfpw_bus_ordr Swap the position of 64 bits in 128 bits for reference picture.
2	RW	0x0	dspw_bus_ordr Swap the position of 64 bits in 128 bits for down-sampled picture.
1	RW	0x0	cmvw_bus_ordr Swap the position of 64 bits in 128 bits for co-located Mv(HEVC only).
0	RO	0x0	reserved

**VEPU DTRNS CFG**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	dspr_otsd Down sampled reference picture read outstanding enable. 1'h0: No outstanding 1'h1: Outstanding read, which improves data transaction efficiency, but core clock frequency should not lower than bus clock frequency.
6:0	RW	0x00	axi_brspcke AXI write response channel check enable. [6]: Reconstructed picture write response check enable. [5]: ME information write response check enable. [4]: CTU information write response check enable. [3]: Down-sampled picture write response check enable. [2]: Bit stream write response check enable. [1]: Link table mode write response check enable. [0]: Reserved for video preprocess.

**VEPU SRC FMT**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	src_range Video source clip (low active). 1'h0: [16:235] for luma and [16:240] for chroma. 1'h1: [0:255] for both luma and chroma.

Bit	Attr	Reset Value	Description
5:2	RW	0x0	src_cfmt Video source color format. 4'h0: BGRA8888 4'h1: RGB888 4'h2: RGB565 4'h4: YUV422 SP 4'h5: YUV422 P 4'h6: YUV420 SP 4'h7: YUV420 P 4'h8: YUYV422 4'h9: UYVY422 Others: Reserved
1	RW	0x0	rbuv_swap Swap the position of R and B for BGRA8888, RGB888, RGB 656 format; Swap the position of U and V for YUV422-SP, YUV420-SP, YUYV422 and UYUV422 format. 1'h0: RGB or YUYV or UYVY. 1'h1: BGR or YVYU or VYUY.
0	RW	0x0	alpha_swap Swap the position of alpha and RGB for ARBG8888. 1'h0: BGRA8888 or RGBA8888. 1'h1: ABGR8888 or ARGB8888.

**VEPU\_SRC\_UDFY**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2y Weight of RED in RGB to Y conversion formula.
17:9	RW	0x000	csc_wgt_g2y Weight of GREEN in RGB to Y conversion formula.
8:0	RW	0x000	csc_wgt_b2y Weight of BLUE in RGB to Y conversion formula.

**VEPU\_SRC\_UDFU**

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2u Weight of RED in RGB to U conversion formula.
17:9	RW	0x000	csc_wgt_g2u Weight of GREEN in RGB to U conversion formula.
8:0	RW	0x000	csc_wgt_b2u Weight of BLUE in RGB to U conversion formula.

**VEPU\_SRC\_UDFV**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2v Weight of RED in RGB to V conversion formula.
17:9	RW	0x000	csc_wgt_g2v Weight of GREEN in RGB to V conversion formula.
8:0	RW	0x000	csc_wgt_b2v Weight of BLUE in RGB to V conversion formula.

**VEPU\_SRC\_UDFO**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	csc_ofst_y Offset of RGB to Y conversion formula.
15:8	RW	0x00	csc_ofst_u Offset of RGB to U conversion formula.
7:0	RW	0x00	csc_ofst_v Offset of RGB to V conversion formula.

**VEPU\_SRC\_PROC**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	afbcd_en AFBC decompress enable (for AFBC format video source).
29	RW	0x0	txa_en Video source texture analysis enable.
28:27	RW	0x0	src_rot Video source rotation mode. 2'h0: 0 degree 2'h1: Clockwise 90 degree 2'h2: Clockwise 180 degree 2'h3: Clockwise 280 degree
26	RW	0x0	src_mirr Video source mirror mode enable.
25:0	RO	0x0000000	reserved

**VEPU\_KLUT\_OFST**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	chrm_klut_ofst Offset of (RDO) chroma cost weight table, values from 0 to 6.

**VEPU\_KLUT\_WGT0**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt1_l9 Low 9 bits of data1 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt0 Data0 in chroma cost weight table.

**VEPU\_KLUT\_WGT1**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt2 Data2 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt1_h9 High 9 bits of data1 in chroma cost weight table.

**VEPU\_KLUT\_WGT2**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt4_l9 Low 9 bits of data4 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt3 Data3 in chroma cost weight table.

**VEPU\_KLUT\_WGT3**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt5 Data5 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt4_h9 High 9 bits of data4 in chroma cost weight table.

**VEPU\_KLUT\_WGT4**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt7_l9 Low 9 bits of data7 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt6 Data6 in chroma cost weight table.

**VEPU\_KLUT\_WGT5**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt8 Data8 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt7_h9 High 9 bits of data7 in chroma cost weight table.

**VEPU\_KLUT\_WGT6**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt10_l9 Low 9 bits of data10 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt9 Data9 in chroma cost weight table.

**VEPU\_KLUT\_WGT7**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt11 Data11 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt10_h9 High 9 bits of data10 in chroma cost weight table.

**VEPU\_KLUT\_WGT8**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt13_l9 Low 9 bits of data13 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt12 Data12 in chroma cost weight table.

**VEPU\_KLUT\_WGT9**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt14 Data14 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt13_h9 High 9 bits of data13 in chroma cost weight table.

**VEPU\_KLUT\_WGT10**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt16_l9 Low 9 bits of data16 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt15 Data15 in chroma cost weight table.

**VEPU\_KLUT\_WGT11**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt17 Data17 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt16_h9 High 9 bits of data16 in chroma cost weight table.

**VEPU\_KLUT\_WGT12**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt19_l9 Low 9 bits of data19 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt18 Data18 in chroma cost weight table.

**VEPU\_KLUT\_WGT13**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt20 Data20 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt19_h9 High 9 bits of data19 in chroma cost weight table.

**VEPU\_KLUT\_WGT14**

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt22_l9 Low 9 bits of data22 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt21 Data21 in chroma cost weight table.

**VEPU KLUT WGT15**

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt23 Data23 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt22_h9 High 9 bits of data22 in chroma cost weight table.

**VEPU KLUT WGT16**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt25_l9 Low 9 bits of data25 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt24 Data24 in chroma cost weight table.

**VEPU KLUT WGT17**

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt26 Data26 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt25_h9 High 9 bits of data25 in chroma cost weight table.

**VEPU KLUT WGT18**

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt28_l9 Low 9 bits of data28 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt27 Data27 in chroma cost weight table.

**VEPU KLUT WGT19**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt29 Data29 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt28_h9 High 9 bits of data28 in chroma cost weight table.

**VEPU KLUT WGT20**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt31_l9 Low 9 bits of data31 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt30 Data30 in chroma cost weight table.

**VEPU\_KLUT\_WGT21**

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrn_klut_wgt32 Data32 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrn_klut_wgt31_h9 High 9 bits of data31 in chroma cost weight table.

**VEPU\_KLUT\_WGT22**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrn_klut_wgt34_l9 Low 9 bits of data34 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrn_klut_wgt33 Data33 in chroma cost weight table.

**VEPU\_KLUT\_WGT23**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	chrn_klut_wgt34_h9 High 9 bits of data34 in chroma cost weight table.

**VEPU\_RC\_CFG**

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rc_ctu_num RC adjustment intervals, base on CTU number.
15:3	RO	0x0000	reserved
2	RW	0x0	aq_mode Mode of aq_delta calculation for CU32 and CU64. 1'b0: aq_delta of CU32/CU64 is calculated by corresponding MAD132/64; 1'b1: aq_delta of CU32/CU64 is calculated by corresponding 4/16 CU16 qp_deltas.
1	RW	0x0	aq_en Adaptive quantization enable.
0	RW	0x0	rc_en Rate control enable.

**VEPU\_RC\_QP**

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	rc_min_qp Min QP for rate control and AQ mode.

Bit	Attr	Reset Value	Description
25:20	RW	0x00	rc_max_qp Max QP for rate control and AQ mode.
19:16	RW	0x0	rc_qp_range QP adjust range(delta_qp) in rate control. Delta_qp is constrained between -rc_qp_range to rc_qp_range.
15:0	RO	0x0000	reserved

**VEPU\_RC\_TGT**

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	ctu_ebit Target bit num for one 64x64 CTU(for HEVC) or one 16x16 MB(for H.264), with 1/16 precision.

**VEPU\_RC\_ADJ0**

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x00	qp_adj4 QP adjust step4 for rate control.
19:15	RW	0x00	qp_adj3 QP adjust step3 for rate control.
14:10	RW	0x00	qp_adj2 QP adjust step2 for rate control.
9:5	RW	0x00	qp_adj1 QP adjust step1 for rate control.
4:0	RW	0x00	qp_adj0 QP adjust step0 for rate control.

**VEPU\_RC\_ADJ1**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	qp_adj8 QP adjust step8 for rate control.
14:10	RW	0x00	qp_adj7 QP adjust step7 for rate control.
9:5	RW	0x00	qp_adj6 QP adjust step6 for rate control.
4:0	RW	0x00	qp_adj5 QP adjust step5 for rate control.

**VEPU\_RC\_DTHD0**

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd0 Bits rate deviation threshold0.

**VEPU\_RC\_DTHD1**

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd1 Bits rate deviation threshold1.



**VEPU\_RC\_DTHD2**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd2 Bits rate deviation threshold2.

**VEPU\_RC\_DTHD3**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd3 Bits rate deviation threshold3.

**VEPU\_RC\_DTHD4**

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd4 Bits rate deviation threshold4.

**VEPU\_RC\_DTHD5**

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd5 Bits rate deviation threshold5.

**VEPU\_RC\_DTHD6**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd6 Bits rate deviation threshold6.

**VEPU\_RC\_DTHD7**

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd7 Bits rate deviation threshold7.

**VEPU\_RC\_DTHD8**

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd8 Bits rate deviation threshold8.

**VEPU\_ROI\_QTHD0**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmin_area2 Min QP for 16x16 CU inside ROI area2.
23:18	RW	0x00	qpmax_area1 Max QP for 16x16 CU inside ROI area1.
17:12	RW	0x00	qpmin_area1 Min QP for 16x16 CU inside ROI area1.
11:6	RW	0x00	qpmax_area0 Max QP for 16x16 CU inside ROI area0.

Bit	Attr	Reset Value	Description
5:0	RW	0x00	qpmin_area0 Min QP for 16x16 CU inside ROI area0.

**VEPU ROI QTHD1**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmax_area4 Max QP for 16x16 CU inside ROI area4.
23:18	RW	0x00	qpmin_area4 Min QP for 16x16 CU inside ROI area4.
17:12	RW	0x00	qpmax_area3 Max QP for 16x16 CU inside ROI area3.
11:6	RW	0x00	qpmin_area3 Min QP for 16x16 CU inside ROI area3.
5:0	RW	0x00	qpmax_area2 Max QP for 16x16 CU inside ROI area2.

**VEPU ROI QTHD2**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmin_area7 Min QP for 16x16 CU inside ROI area7.
23:18	RW	0x00	qpmax_area6 Max QP for 16x16 CU inside ROI area6.
17:12	RW	0x00	qpmin_area6 Min QP for 16x16 CU inside ROI area6.
11:6	RW	0x00	qpmax_area5 Max QP for 16x16 CU inside ROI area5.
5:0	RW	0x00	qpmin_area5 Min QP for 16x16 CU inside ROI area5.

**VEPU ROI QTHD3**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	qpmap_mode QP threshold generation for the CUs whose size is bigger than 16x16. 2'h0: Mean value of 16x16 CU QP thresholds 2'h1: Max value of 16x16 CU QP thresholds 2'h2: Min value of 16x16 CU QP thresholds 2'h3: Reserved
29:6	RO	0x000000	reserved
5:0	RW	0x00	qpmax_area7 Max QP for 16x16 CU inside ROI area7.

**VEPU PIC OFST**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pic_ofst_x Horizontal offset for encoding picture.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	pic_ofst_y Vertical offset for encoding picture.

**VEPU\_SRC\_STRD**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_strd1 CHROMA stride of video source, only for YUV format. Note that U and V stride must be the same when color format is YUV planar.
15:0	RW	0x0000	src_strd0 Video source stride0, based on pixel (byte). Note that if the video format is YUV, src_strd is the LUMA component stride while src_strd1 is the CHROMA component stride.

**VEPU\_ADR\_SRC0**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src0 Base address of the 1st storage area for video source. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src0 is configured as the base address of video source frame buffer. YUV422/420 semi-planar have 2 storage area, while adr_src0 is configured as the base address of Y frame buffer. YUV422/420 planar have 3 storage area, while adr_src0 is configured as the base address of Y frame buffer. Note that if the video source is compressed by AFBC, adr_src0 is configured as the base address of compressed frame buffer.

**VEPU\_ADR\_SRC1**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src1 Base address of the 2nd storage area for video source. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src1 is reserved. YUV422/420 semi-planar have 2 storage area, while adr_src1 is configured as the base address of CHROMA frame buffer. YUV422/420 planar have 3 storage area, while adr_src1 is configured as the base address of U frame buffer. Note that if the video source is compressed by AFBC, adr_src1 should be configured to 0.

**VEPU\_ADR\_SRC2**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src2 Base address of V frame buffer when video source is uncompress and color format is YUV422/420 planar.

**VEPU\_ADR\_ROI**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	roi_addr High 28 bits of base address for ROI configuration.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

**VEPU\_ADR\_RFPW\_H**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpw_h_addr High 20 bits of the header_block base address for compressed reference frame write.
11:0	RO	0x000	reserved

**VEPU\_ADR\_RFPW\_B**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpw_b_addr High 20 bits of the body_block base address for compressed reference frame write.
11:0	RO	0x000	reserved

**VEPU\_ADR\_RFPR\_H**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpr_h_addr High 20 bits of the header_block base address for compressed reference frame read.
11:0	RO	0x000	reserved

**VEPU\_ADR\_RFPR\_B**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpr_b_addr High 20 bits of the body_block base address for compressed reference frame read.
11:0	RO	0x000	reserved

**VEPU\_ADR\_CMVW**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	cmvw_addr High 22 bits of base address for col-located Mv write, HEVC only.
9:0	RO	0x000	reserved

**VEPU\_ADR\_CMVR**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	cmvr_addr High 22 bits of base address for col-located Mv read, HEVC only.
9:0	RO	0x000	reserved

**VEPU\_ADR\_DSPW**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	dspw_addr High 22 bits of base address for down-sampled reference frame write.

Bit	Attr	Reset Value	Description
9:0	RO	0x000	reserved

**VEPU\_ADR\_DSPR**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	dspr_addr High 22 bits of base address for down-sampled reference frame read.
9:0	RO	0x000	reserved

**VEPU\_ADR\_MEIW**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	meiw_addr High 22 bits of base address for ME information write.
9:0	RO	0x000	reserved

**VEPU\_ADR\_BSBT**

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	bsbt_addr High 25 bits of the top address of bit stream buffer.
6:0	RO	0x00	reserved

**VEPU\_ADR\_BSBB**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	bsbb_addr High 25 bits of the bottom address of bit stream buffer.
6:0	RO	0x00	reserved

**VEPU\_ADR\_BSBR**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	bsbr_addr Read address of bit stream buffer, 128B aligned. VEPU will pause when write address meets read address and then send an interrupt. SW should move some data out from bit stream buffer and change this register accordingly. After that VEPU will continue processing automatically.
6:0	RO	0x00	reserved

**VEPU\_ADR\_BSBS**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_bsbs Start address of bit stream buffer. VEPU begins to write bit stream from this address and increase address automatically. Note that the VEPU's real-time write address is marked in BSB_STUS.

**VEPU\_SLI\_SPLT**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sli_splt_cnum_m1 Number of CTU/MB for slice split. Valid when slice is splited by CTU/MB.
15:14	RO	0x0	reserved
13	RW	0x0	sli_flsh Slice flush. Flush all the bit stream after each slice finished.
12:3	RW	0x000	sli_max_num_m1 Max slice num in one frame.
2	RW	0x0	sli_splt_cpst Slice split compensation when slice is splited by byte. Byte distortion of current slice will be compensated in the next slice.
1	RW	0x0	sli_splt_mode Slice split mode. 1'h0: Slice splited by byte. 1'h1: Slice splited by number of MB(H.264)/CTU(HEVC).
0	RW	0x0	sli_splt Slice split enable.

**VEPU SLI BYTE**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sli_splt_byte Byte number for each slice when slice is splited by byte.

**VEPU ME RNGE**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_frm_num Frame number difference value between current and reference frame, HEVC only.
15:14	RO	0x0	reserved
13:11	RW	0x0	rme_srch_v RME vertical search range, values from 4 to 5.
10:8	RW	0x0	rme_srch_h RME horizontal search range, values from 3 to 7.
7:4	RW	0x0	cme_srch_v CME vertical search range, base on 16 pixel.
3:0	RW	0x0	cme_srch_h CME horizontal search range, base on 16 pixels.

**VEPU ME CFG**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	fme_dis [4]: Disable 64x64 block FME. [3]: Disable 32x32 block FME. [2]: Disable 16x16 block FME. [1]: Disable 8x8 block FME. [0]: Disable 4x4 block FME.

Bit	Attr	Reset Value	Description
26:22	RW	0x00	rme_dis [4]: Disable 64x64 block RME. [3]: Disable 32x32 block RME. [2]: Disable 16x16 block RME. [1]: Disable 8x8 block RME. [0]: Disable 4x4 block RME.
21	RW	0x0	colmv_load Load co-located Mvs as predicated Mv candidates, HEVC only.
20	RW	0x0	colmv_stor Store col-Mv information to external memory, HEVC only.
19:18	RW	0x0	pmv_num PMV number (should be constant2).
17:16	RW	0x0	mv_llmt Motion vector limit ( by level), H.264 only. 2'h0: Mvy is limited to [-64,63]. Others: Mvy is limited to [-128,127].
15:8	RW	0x00	pmv_mdst_v Min vertical distance for PMV selection.
7:0	RW	0x00	pmv_mdst_h Min horizontal distance for PMV selection.

**VEPU ME CACH**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	cach_l2_map L2 cach mapping, base on pixels. 2'h0: 32x512 2'h1: 16x1024 2'h2: 8x2048 2'h3: 4x4096
15:11	RW	0x00	cme_rama_h Height of CME RAMA district, base on 4 pixels.
10:0	RW	0x000	cme_rama_max CME's max RAM address.

**VEPU SYNT LONG REFM0**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	poc_lsb_lt2 Poc_lsb_lt[2]
15:0	RW	0x0000	poc_lsb_lt1 Poc_lsb_lt[1]

**VEPU SYNT LONG REFM1**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_poc_msb_cycl2 Delta_poc_msb_cycle_lt[2]
15:0	RW	0x0000	dlt_poc_msb_cycl1 Delta_poc_msb_cycle_lt[1]

**VEPU IPRD CSTS**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vthd_c CHROMA variance threshold to select intra prediction cost function.
15:12	RO	0x0	reserved
11:0	RW	0x000	vthd_y LUMA variance threshold to select intra prediction cost function.

**VEPU RDO CFG H264**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	atf_intra_e Intra mode anti-flicker enable.
18	RW	0x0	atf_lvl_e Block level anti-flicker enable.
17:16	RW	0x0	atf_edg Edge of anti-flicker, base on MB. the MBs inside edge should not influenced.
15	RW	0x0	atr_e Anti-ring enable.
14	RW	0x0	scl_lst_sel Scale list selection. 1'h0: Flat scale list. 1'h1: Default scale list.
13	RW	0x0	ccwa_e Chroma cost weight adjustment(KLUT) enable.
12:5	RW	0x00	rdo_mask [7]: Disable intra4x4. [6]: Disable intra8x8. [5]: Disable intra16x16. [4]: Disable inter8x8 with T4. [3]: Disable inter8x8 with T8. [2]: Disable inter16x16 with T4. [1]: Disable inter16x16 with T8. [0]: Disable skip mode.
4	RW	0x0	chrm_spcl Chroma special candidates enable.
3	RW	0x0	vlc_lmt CAVLC syntax limit.
2	RW	0x0	arb_sel Reserved
1	RW	0x0	inter_4x4 4x4 sub MB enable.
0	RW	0x0	rect_size Limit sub_mb_rect_size for low level.

**VEPU RDO CFG HEVC**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	scl_lst_sel Scale list selection. 1'h0: Flat scale list. 1'h1: Default scale list.



Bit	Attr	Reset Value	Description
23	RW	0x0	ccwa_e Chroma cost weight adjustment(KLUT) enable.
22:19	RW	0x0	cu_intra_e [3]: Intra 32x32 mode enable. [2]: Intra 16x16 mode enable. [1]: Intra 8x8 mode enable. [0]: Intra 4x4 mode enable.
18:10	RO	0x000	reserved
9:6	RW	0x0	cu_inter_e [3]: 64x64 inter mode enable. [2]: 32x32 inter mode enable. [1]: 16x16 inter mode enable. [0]: 8x8 inter mode enable.
5:4	RO	0x0	reserved
3	RW	0x0	rdoq_e Reserved
2	RW	0x0	chrn_spcl 4 special chroma candidates enable.
1	RW	0x0	ltm_idx0l0 The 1st reference frame in ref-list0 is long term.
0	RW	0x0	ltm_col Co-located picture is long term reference frame.

**VEPU SYNT NAL H264**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:2	RW	0x00	nal_unit_type nal_unit_type
1:0	RW	0x0	nal_ref_idc nal_ref_idc

**VEPU SYNT NAL HEVC**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	nal_unit_type nal_unit_type

**VEPU SYNT SPS H264**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:9	RO	0x0000000	reserved
8:5	RW	0x0	mpoc_lm4 log2_max_pic_order_cnt_lsb_minus4
4	RW	0x0	drct_8x8 direct_8x8_inference_flag
3:0	RW	0x0	max_fnum log2_max_frame_num_minus4

**VEPU SYNT SPS HEVC**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	strg_intra_smth strong_intra_smoothing_enabled_flag
19:16	RW	0x0	log2_max_poc_lsb log2_max_pic_order_cnt_lsb_minus4
15	RW	0x0	tmpl_mvp_e sps_temporal_mvp_enabled_flag
14:9	RW	0x00	num_lt_ref_pic num_long_term_ref_pics_sps
8	RW	0x0	lt_ref_pic_prsnt long_term_ref_pics_present_flag
7:1	RW	0x00	num_st_ref_pic num_short_term_ref_pic_sets
0	RW	0x0	smpl_adpt_ofst_e sample_adaptive_offset_enabled_flag

**VEPU SYNT PPS H264**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	dbf_cp_flg deblocking_filter_control_present_flag
23	RW	0x0	wght_pred weight_pred_flag
22:18	RW	0x00	cr_ofst second_chroma_qp_index_offset
17:13	RW	0x00	cb_ofst chroma_qp_index_offset
12:7	RW	0x00	pic_init_qp pic_init_qp_minus26 + 26
6:5	RW	0x0	num_ref1_idx num_ref_idx_l1_active_minus1
4:3	RW	0x0	num_ref0_idx num_ref_idx_l0_active_minus1
2	RW	0x0	csip_flag constrained_intra_pred_flag
1	RW	0x0	trns_8x8 transform_8x8_mode_flag
0	RW	0x0	etpy_mode entropy_coding_mode_flag

**VEPU SYNT PPS HEVC**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:19	RW	0x0	cu_qp_dlt_depth diff_cu_qp_delta_depth
18	RW	0x0	sli_seg_hdr_extn slice_segment_header_extension_present_flag
17	RW	0x0	lst_mdfy_prsnt_flg lists_modification_present_flag
16	RW	0x0	dblk_fltr_ovrd_e deblocking_filter_override_enabled_flag
15	RW	0x0	lp_fltr_acrs_sli pps_loop_filter_across_slices_enabled_flag

Bit	Attr	Reset Value	Description
14	RW	0x0	chrm_qp_ofst_prsnt pps_slice_chroma_qp_offsets_present_flag. VEPU only supports PPS level chroma QP adjustments so this field should be configured to 0.
13	RW	0x0	cu_qp_dlt_en cu_qp_delta_enabled_flag
12:7	RW	0x00	pic_init_qp init_qp_minus26+26
6	RW	0x0	cbc_init_prsnt_flag cabac_init_present_flag
5	RW	0x0	sgn_dat_hid_e sign_data_hiding_enabled_flag
4:2	RW	0x0	num_extr_sli_hdr num_extra_slice_header_bits
1	RW	0x0	out_flg_prsnt_flg output_flag_present_flag
0	RW	0x0	dpdnt_sli_seg_en dependent_slice_segments_enable_flag

**VEPU SYNT SLI0 H264**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	frm_num frame_num
15:14	RO	0x0	reserved
13:12	RW	0x0	cbc_init_idc cabac_init_idc
11	RW	0x0	num_ref_ovrd num_ref_idx_active_override_flag
10	RW	0x0	drct_smv direct_spatial_mv_pred_flag
9:2	RW	0x00	pps_id pic_parameter_set_id
1:0	RW	0x0	sli_type slice_type: 0->P, 1->B, 2->I.

**VEPU SYNT SLI0 HEVC**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RW	0x0	no_out_pri_pic no_output_of_prior_pics_flag
30:25	RW	0x00	sli_pps_id slice_pic_parameter_set_id
24	RW	0x0	dpdnt_sli_seg_flg dependent_slice_segment_flag
23:17	RW	0x00	sli_rsrv_flg slice_served_flag
16:15	RW	0x0	sli_type slice_type: 0->B, 1->P, 2->I.
14	RW	0x0	pic_out_flg pic_output_flag
13	RW	0x0	sli_tmprl_mvp_e slice_temporal_mvp_enabled_flag

Bit	Attr	Reset Value	Description
12	RW	0x0	sli_sao_luma_flg slice_sao_luma_flag
11	RW	0x0	sli_sao_chrm_flg slice_sao_chroma_flag
10	RW	0x0	num_refidx_act_ovrd num_ref_idx_active_override_flag
9:8	RW	0x0	num_refidx_l0_act num_ref_idx_l0_active_minus1
7:6	RW	0x0	num_refidx_l1_act num_ref_idx_l1_active_minus1
5	RW	0x0	ref_pic_lst_mdf_l0 ref_pic_list_modification_flag_l0
4	RO	0x0	reserved
3	RW	0x0	mrg_lft_flg sao_merge_left_flag
2	RW	0x0	mrg_up_flg sao_merge_up_flag
1	RW	0x0	mvd_l1_zero_flg mvd_l1_zero_flag
0	RW	0x0	cbc_init_flg cabac_init_flag

**VEPU SYNT SLI1 H264**

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	poc_lsb pic_order_cnt_lsb
15:0	RW	0x0000	idr_pid idr_pic_id

**VEPU SYNT SLI1 HEVC**

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	lst_entry_l0 list_entry_l0
26	RW	0x0	col_frm_l0_flg collocated_from_l0_flag
25	RW	0x0	col_ref_idx collocated_ref_idx
24	RO	0x0	reserved
23:22	RW	0x0	max_mrg_cnd 5 - five_minus_max_num_merge_cand, values from 0 to 3
21:16	RW	0x00	sli_qp slice_qp
15:11	RW	0x00	sli_cb_qp_ofst Actually this field should be configured as pps_cb_qp_offset.
10	RW	0x0	dblk_fltr_ovrd_flg deblocking_filter_override_flag

Bit	Attr	Reset Value	Description
9	RW	0x0	sp_dblk_fltr_dis slice/pps_deblocking_filter_disabled_flag. If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_deblocking_filter_disabled_flag. Otherwise it is pps_deblocking_filter_disabled_flag.
8	RW	0x0	sli_lp_fltr_acrs_sli slice_loop_filter_across_slices_enabled_flag
7:4	RW	0x0	sp_beta_ofst_div2 slice/pps_beta_offset_div2. If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_beta_offset_div2. Otherwise it is pps_beta_offset_div2.
3:0	RW	0x0	sp_tc_ofst_div2 slice/pps_tc_offset_div2. If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_tc_offset_div2. Otherwise it is pps_tc_offset_div2.

**VEPU SYNT SLI2 H264**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rodr_pic_num abs_diff_pic_num_minus1/long_term_pic_num
15:13	RO	0x0	reserved
12:11	RW	0x0	dis_dblk_idc disable_deblocking_filter_idc
10:7	RW	0x0	sli_alph_ofst slice_alpha_c0_offset_div2
6:3	RW	0x0	sli_beta_ofst slice_beta_offset_div2
2	RW	0x0	ref_list0_rodr ref_pic_list_reordering_flag_l0
1:0	RW	0x0	rodr_pic_idx reordering_of_pic_nums_idc

**VEPU SYNT SLI2 HEVC**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sli_hdr_ext_len slice_segment_header_extension_length
15:0	RW	0x0000	sli_poc_lsb slice_pic_order_cnt_lsb

**VEPU SYNT REFM0 H264**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:26	RW	0x0	mmco_type2 memory_management_control_operation[2]
25:23	RW	0x0	mmco_type1 memory_management_control_operation[1]

Bit	Attr	Reset Value	Description
22:7	RW	0x0000	mmco_parm0 MMCO parameters which have different meanings according to different mmco_parm0 value. difference_of_pic_nums_minus1 for mmco_parm0 equals 0 or 3. long_term_pic_num for mmco_parm0 equals 2. long_term_frame_idx for mmco_parm0 equals 6. max_long_term_frame_idx_plus1 for mmco_parm0 equals 4.
6:4	RW	0x0	mmco_type0 memory_management_control_operation
3	RW	0x0	mmco4_pre A No.4 MMCO should be executed firstly if mmo4_pre is 1
2	RW	0x0	arpm_flg adaptive_ref_pic_marking_mode_flag
1	RW	0x0	ltrf_flg long_term_reference_flag
0	RW	0x0	nopp_flg no_output_of_prior_pics_flag

**VEPU\_SYNT\_REFM0\_HEVC**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	num_lt_sps num_long_term_sps
29:24	RW	0x00	st_ref_pic_idx short_term_ref_pic_set_idx
23:22	RW	0x0	num_lt_pic num_long_term_pics
21:17	RW	0x00	lt_idx_sps lt_idx_sps
16:1	RW	0x0000	poc_lsb_lt0 poc_lsb_lt[0]
0	RW	0x0	st_ref_pic_flg short_term_ref_pic_set_sps_flag

**VEPU\_SYNT\_REFM1\_H264**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mmco_parm2 MMCO parameters which have different meanings according to different mmco_parm2 value. difference_of_pic_nums_minus1 for mmco_parm2 equals 0 or 3. long_term_pic_num for mmco_parm2 equals 2. long_term_frame_idx for mmco_parm2 equals 6. max_long_term_frame_idx_plus1 for mmco_parm2 equals 4.
15:0	RW	0x0000	mmco_parm1 MMCO parameters which have different meanings according to different mmco_parm1 value. difference_of_pic_nums_minus1 for mmco_parm1 equals 0 or 3. long_term_pic_num for mmco_parm1 equals 2. long_term_frame_idx for mmco_parm1 equals 6. max_long_term_frame_idx_plus1 for mmco_parm1 equals 4.

**VEPU\_SYNT\_REFM1\_HEVC**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	used_by_lt_flg2 used_by_curr_pic_lt_flag[2]
30	RW	0x0	used_by_lt_flg1 used_by_curr_pic_lt_flag[1]
29	RW	0x0	used_by_lt_flg0 used_by_curr_pic_lt_flag[0]
28	RW	0x0	dlt_poc_msb_prsnt2 delta_poc_msb_present_flag[2]
27	RW	0x0	dlt_poc_msb_prsnt1 delta_poc_msb_present_flag[1]
26	RW	0x0	dlt_poc_msb_prsnt0 delta_poc_msb_present_flag[0]
25:10	RW	0x0000	dlt_poc_msb_cycl0 delta_poc_msb_cycle_lt[0]
9:5	RW	0x00	num_negative_pics num_neg_pic
4	RW	0x0	num_pos_pic num_positive_pics
3:0	RW	0x0	used_by_s0_flg used_by_curr_pic_s0_flag

**VEPU OSD CFG**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	osd_plt_typ OSD palette type. 1'h1: Default type. 1'h0: User defined type.
16	RW	0x0	osd_plt_cks OSD palette clock selection. 1'h0: Configure bus clock domain. 1'h1: Core clock domain.
15:8	RW	0x00	osd_inv_e OSD inverse color enable, each bit controls corresponding region.
7:0	RW	0x00	osd_e OSD region enable, each bit controls corresponding OSD region.

**VEPU OSD INV**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	osd_ithd_r7 Color inverse threshold for OSD region7.
27:24	RW	0x0	osd_ithd_r6 Color inverse threshold for OSD region6.
23:20	RW	0x0	osd_ithd_r5 Color inverse threshold for OSD region5.
19:16	RW	0x0	osd_ithd_r4 Color inverse threshold for OSD region4.
15:12	RW	0x0	osd_ithd_r3 Color inverse threshold for OSD region3.
11:8	RW	0x0	osd_ithd_r2 Color inverse threshold for OSD region2.

Bit	Attr	Reset Value	Description
7:4	RW	0x0	osd_ithd_r1 Color inverse threshold for OSD region1.
3:0	RW	0x0	osd_ithd_r0 Color inverse threshold for OSD region0.

**VEPU\_SYNT\_REFM2**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_poc_s0_m11 delta_poc_s0_minus1[1]
15:0	RW	0x0000	dlt_poc_s0_m10 delta_poc_s0_minus1[0]

**VEPU\_SYNT\_REFM2\_H264**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	long_term_frame_idx2 long_term_frame_idx[2] (when mmco equal 3)
7:4	RW	0x0	long_term_frame_idx1 long_term_frame_idx[1] (when mmco equal 3)
3:0	RW	0x0	long_term_frame_idx0 long_term_frame_idx[0] (when mmco equal 3)

**VEPU\_SYNT\_REFM3**

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_poc_s0_m13 delta_poc_s0_minus1[3]
15:0	RW	0x0000	dlt_poc_s0_m12 delta_poc_s0_minus1[2]

**VEPU\_OSD0\_POS**

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd0_rb_y Y coordinate/16 of OSD region0's right-bottom point.
23:16	RW	0x00	osd0_rb_x X coordinate/16 of OSD region0's right-bottom point.
15:8	RW	0x00	osd0_lt_y Y coordinate/16 of OSD region0's left-top point.
7:0	RW	0x00	osd0_lt_x X coordinate/16 of OSD region0's left-top point.

**VEPU\_OSD1\_POS**

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd1_rb_y Y coordinate/16 of OSD region1's right-bottom point.
23:16	RW	0x00	osd1_rb_x X coordinate/16 of OSD region1's right-bottom point.
15:8	RW	0x00	osd1_lt_y Y coordinate/16 of OSD region1's left-top point.



Bit	Attr	Reset Value	Description
7:0	RW	0x00	osd1_lt_x X coordinate/16 of OSD region1's left-top point.

**VEPU OSD2 POS**

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd2_rb_y Y coordinate/16 of OSD region2's right-bottom point.
23:16	RW	0x00	osd2_rb_x X coordinate/16 of OSD region2's right-bottom point.
15:8	RW	0x00	osd2_lt_y Y coordinate/16 of OSD region2's left-top point.
7:0	RW	0x00	osd2_lt_x X coordinate/16 of OSD region2's left-top point.

**VEPU OSD3 POS**

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd3_rb_y Y coordinate/16 of OSD region3's right-bottom point.
23:16	RW	0x00	osd3_rb_x X coordinate/16 of OSD region3's right-bottom point.
15:8	RW	0x00	osd3_lt_y Y coordinate/16 of OSD region3's left-top point.
7:0	RW	0x00	osd3_lt_x X coordinate/16 of OSD region3's left-top point.

**VEPU OSD4 POS**

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd4_rb_y Y coordinate/16 of OSD region4's right-bottom point.
23:16	RW	0x00	osd4_rb_x X coordinate/16 of OSD region4's right-bottom point.
15:8	RO	0x00	reserved
7:0	RW	0x00	osd4_lt_x X coordinate/16 of OSD region4's left-top point.

**VEPU OSD5 POS**

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd5_rb_y Y coordinate/16 of OSD region5's right-bottom point.
23:16	RW	0x00	osd5_rb_x X coordinate/16 of OSD region5's right-bottom point.
15:8	RW	0x00	osd5_lt_y Y coordinate/16 of OSD region5's left-top point.
7:0	RW	0x00	osd5_lt_x X coordinate/16 of OSD region5's left-top point.

**VEPU OSD6 POS**

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd6_rb_y Y coordinate/16 of OSD region6's right-bottom point.
23:16	RW	0x00	osd6_rb_x X coordinate/16 of OSD region6's right-bottom point.
15:8	RW	0x00	osd6_lt_y Y coordinate/16 of OSD region6's left-top point.
7:0	RW	0x00	osd6_lt_x X coordinate/16 of OSD region6's left-top point.

**VEPU OSD7 POS**

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd7_rb_y Y coordinate/16 of OSD region7's right-bottom point.
23:16	RW	0x00	osd7_rb_x X coordinate/16 of OSD region7's right-bottom point.
15:8	RW	0x00	osd7_lt_y Y coordinate/16 of OSD region7's left-top point.
7:0	RW	0x00	osd7_lt_x X coordinate/16 of OSD region7's left-top point.

**VEPU ADR OSD0**

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd0_addr High 28 bits of base address for OSD region0.
3:0	RO	0x0	reserved

**VEPU ADR OSD1**

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd1_addr High 28 bits of base address for OSD region1.
3:0	RO	0x0	reserved

**VEPU ADR OSD2**

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd2_addr High 28 bits of base address for OSD region2.
3:0	RO	0x0	reserved

**VEPU ADR OSD3**

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd3_addr High 28 bits of base address for OSD region3.
3:0	RO	0x0	reserved

**VEPU ADR OSD4**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd4_addr High 28 bits of base address for OSD region4.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

**VEPU\_ADR\_OSD5**

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd5_addr High 28 bits of base address for OSD region5.
3:0	RO	0x0	reserved

**VEPU\_ADR\_OSD6**

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd6_addr High 28 bits of base address for OSD region6.
3:0	RO	0x0	reserved

**VEPU\_ADR\_OSD7**

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd7_addr High 28 bits of base address for OSD region7.
3:0	RO	0x0	reserved

**VEPU\_ST\_BSL**

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	bs_lgth Bit stream length for current frame.

**VEPU\_ST\_SSE\_L32**

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sse_l32 Low 32 bits of encoding distortion (SSE).

**VEPU\_ST\_SSE\_QP**

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	sse_h8 High bits of encoding distortion(SSE).
23:22	RO	0x0	reserved
21:0	RO	0x0000000	qp_sum Sum of QP for the encoded frame.

**VEPU\_ST\_SAO**

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	sao_ynum Number of CTUs whose LUMA component are adjusted by SAO.
11:0	RO	0x000	sao_cnum Number of CTUs whose CHROMA component are adjusted by SAO.

**VEPU\_ST\_ENC**

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	st_sclr Status of safe clear. 1'h0: Safe clear is finished or not started. 1'h1: VEPu is performing safe clear.
1:0	RO	0x0	st_enc VEPU working status. 2'h0: Idle. 2'h1: Working in register configuration mode. 2'h2: Working in link table configuration mode.

**VEPU\_ST\_LKT**

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	fnum_int Number of frames has been encoded since link table mode started, updated only when corresponding link table node send interrupt (VEPU_ENC_PIC_node_int==1).
15:8	RO	0x00	fnum_cfg Number of frames has been configured since link table mode started.
7:0	RO	0x00	fnum_enc Number of frames has been encoded since link table mode started.

**VEPU\_ST\_NADR**

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	node_addr High 28 bits of the address for the processing linke table node.
3:0	RO	0x0	reserved

**VEPU\_ST\_BSB**

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	bsbw_addr High 28 bits of bit stream buffer write address.
3:0	RO	0x0	reserved

**VEPU\_ST\_BUS**

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:21	RO	0x00	axir_err AXI read error. [5]: ROI configuration (AXIO_ARID==7) [4]: Down-sampled picture (AXIO_ARID==6) [3]: Co-located Mv (AXIO_ARID==5) [2]: Link table (AXIO_ARID==4) [1]: Reference picture (AXIO_ARID==1,2,3,8) [0]: Video source load (AXI1)

Bit	Attr	Reset Value	Description
20:14	RO	0x00	axib_err AXI write response error. [6]: Reconstructed picture channel (AXIO_WID==5) [5]: ME information channel (AXIO_WID==4) [4]: Co-located Mv channel (AXIO_WID==3) [3]: Down-sampled picture channel (AXIO_WID==2) [2]: Bit stream channel (AXIO_WID==1) [1]: Link table node channel (AXIO_WID==0) [0]: Reserved
13:7	RO	0x00	axib_ovfl AXI write response outstanding overflow. [6]: Reconstructed picture channel (AXIO_WID==5) [5]: ME information channel (AXIO_WID==4) [4]: Co-located Mv channel (AXIO_WID==3) [3]: Down-sampled picture channel (AXIO_WID==2) [2]: Bit stream channel (AXIO_WID==1) [1]: Link table node channel (AXIO_WID==0) [0]: Reserved.
6:0	RO	0x00	axib_idl AXI write response idle. [6]: Reconstructed picture channel (AXIO_WID==5) [5]: ME information channel (AXIO_WID==4) [4]: Co-located Mv channel (AXIO_WID==3) [3]: Down-sampled picture channel (AXIO_WID==2) [2]: Bit stream channel (AXIO_WID==1) [1]: Link table node channel (AXIO_WID==0) [0]: Reserved

**VEPU\_ST\_SNUM**

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	sli_num Number for slices has been encoded and not read out (by reading ST_SLEN).

**VEPU\_ST\_SLEN**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RO	0x0000000	sli_len Byte length for the earlist encoded slice which has not been read out( by reading VEPUS_ST_SLEN).

**VEPU\_ST\_PNUM\_P64**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	pnum_p64 Number of 64x64 inter predicted blocks.

**VEPU\_ST\_PNUM\_P32**

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:0	RO	0x0000	pnum_p32 Number of 32x32 inter predicted blocks.

**VEPU ST PNUM P16**

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pnum_p16 Number of 16x16 inter predicted blocks.

**VEPU ST PNUM P8**

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	pnum_p8 Number of 8x8 inter predicted blocks.

**VEPU ST PNUM I32**

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	pnum_i32 Number of 32x32 intra predicted blocks.

**VEPU ST PNUM I16**

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pnum_i16 Number of 16x16 intra predicted blocks.

**VEPU ST PNUM I8**

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	pnum_i8 Number of 8x8 intra predicted blocks.

**VEPU ST PNUM I4**

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	pnum_i4 Number of 4x4 intra predicted blocks.

**VEPU ST B8 QP0**

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp0 Number of block8x8s with QP=0. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP1**

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp1 Number of block8x8s with QP=1. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP2**

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp2 Number of block8x8s with QP=2. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP3**

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp3 Number of block8x8s with QP=3. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP4**

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp4 Number of block8x8s with QP=4. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP5**

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp5 Number of block8x8s with QP=5. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP6**

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp6 Number of block8x8s with QP=6. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP7**

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp7 Number of block8x8s with QP=7. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) block8x8s; while H.264 MB is considered as 4 block8x8s.

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp7 Number of block8x8s with QP=7. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP8**

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp8 Number of block8x8s with QP=8. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP9**

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp9 Number of block8x8s with QP=9. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP10**

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp10 Number of block8x8s with QP=10. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP11**

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp11 Number of block8x8s with QP=11. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP12**

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp12 Number of block8x8s with QP=12. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP13**

Address: Operational Base + offset (0x0298)



Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp13 Number of block8x8s with QP=13. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP14**

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp14 Number of block8x8s with QP=14. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP15**

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp15 Number of block8x8s with QP=15. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP16**

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp16 Number of block8x8s with QP=16. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP17**

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp17 Number of block8x8s with QP=17. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP18**

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp18 Number of block8x8s with QP=18. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP19**

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	b8num_qp19 Number of block8x8s with QP=19. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP20**

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp20 Number of block8x8s with QP=20. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP21**

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp21 Number of block8x8s with QP=21. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP22**

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp22 Number of block8x8s with QP=22. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP23**

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp23 Number of block8x8s with QP=23. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP24**

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp24 Number of block8x8s with QP=24. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP25**

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp25 Number of block8x8s with QP=25. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP26**

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp26 Number of block8x8s with QP=26. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP27**

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp27 Number of block8x8s with QP=27. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP28**

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp28 Number of block8x8s with QP=28. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP29**

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	b8num_qp29 Number of block8x8s with QP=29. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP30**

Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp30 Number of block8x8s with QP=30. HEVC CUs of which size are bigger than 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP31**

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp31 Number of block8x8s with QP=31. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP32**

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp32 Number of block8x8s with QP=32. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP33**

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp33 Number of block8x8s with QP=33. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP34**

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp34 Number of block8x8s with QP=34. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP35**

Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp35 Number of block8x8s with QP=35. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP36**

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp36 Number of block8x8s with QP=36. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP37**

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp37 Number of block8x8s with QP=37. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP38**

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp38 Number of block8x8s with QP=38. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP39**

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp39 Number of block8x8s with QP=39. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP40**

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp40 Number of block8x8s with QP=40. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP41**

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp41 Number of block8x8s with QP=41. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP42**

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp42 Number of block8x8s with QP=42. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP43**

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp43 Number of block8x8s with QP=43. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP44**

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp44 Number of block8x8s with QP=44. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP45**

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp45 Number of block8x8s with QP=45. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP46**

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp46 Number of block8x8s with QP=46. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP47**

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp47 Number of block8x8s with QP=47. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP48**

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp48 Number of block8x8s with QP=48. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ clock8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP49**

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp49 Number of block8x8s with QP=49. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP50**

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp50 Number of block8x8s with QP=50. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST B8 QP51**

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp51 Number of block8x8s with QP=51. HEVC CUs of which size are bigger than 8x8 are considered as $(CU\_size/8)*(CU\_size/8)$ block8x8s; while H.264 MB is considered as 4 block8x8s.

**VEPU ST CPLX TMP**

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	madp Mean absolute differences between current encoding and reference frame.

**VEPU ST BNUM CME**

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	num_ctu Number of CTU (HEVC: 64x64; H.264: 64x16) for CME inter-frame prediction.

**VEPU ST CPLX SPT**

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	madi Mean absolute differences for current encoding frame.

**VEPU ST BNUM B16**

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	num_b16 Number of valid 16x16 blocks for one frame.

**VEPU L2CFG ADDR**

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	l2cfg_addr Level2 configuration address.

**VEPU\_L2CFG\_WDATA**

Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	l2cfg_wdata L2 configuration write data. Single access: write address to VEPU_L2CFG_ADDR then write data to VEPU_L2CFG_WDATA. Burst access: write the start address to VEPU_L2CFG_ADDR then write datas (to VEPU_L2CFG_WDATA) consecutively. Address will be auto increased after write VEPU_L2CFG_WDATA, no need to configure VEPU_L2CFG_ADDR.

**VEPU\_L2CFG\_RDATA**

Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	l2cfg_rdata L2 configuration read data. Single access: write address to VEPU_L2CFG_ADDR then read data from VEPU_L2CFG_RDATA. Burst access: write the start address to VEPU_L2CFG_ADDR then read datas (from VEPU_L2CFG_RDATA) consecutively. Address will be auto increased after read VEPU_L2CFG_RDATA, no need to configure VEPU_L2CFG_ADDR.

**VEPU\_OSD\_PLT0**

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	alpha Alpha
23:16	RW	0x00	y Y component
15:8	RW	0x00	u U component
7:0	RW	0x00	v V component

**VEPU\_OSD\_PLT1**

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	alpha Alpha
23:16	RW	0x00	y Y component
15:8	RW	0x00	u U component
7:0	RW	0x00	v V component

**VEPU\_OSD\_PLT255**

Address: Operational Base + offset (0x07FC)



Bit	Attr	Reset Value	Description
31:24	RW	0x00	alpha Alpha
23:16	RW	0x00	y Y component
15:8	RW	0x00	u U component
7:0	RW	0x00	v V component

**VEPU ST WDG**

Address: Operational Base + offset (0x085C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	frm_tout Frame encoding time out.
7	RO	0x0	reserved
6	RO	0x0	reserved
5	RO	0x0	reserved
4	RO	0x0	reserved
3	RO	0x0	reserved
2	RO	0x0	reserved
1	RO	0x0	reserved
0	RO	0x0	reserved

**VEPU ST PPL**

Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	frm_wrk Frame encoding is working.
7	RO	0x0	etpy_wrk Entropy is working.
6	RO	0x0	lpf_wrk Loop filter is working.
5	RO	0x0	rdo_wrk RDO is working.
4	RO	0x0	fme_wrk FME is working.
3	RO	0x0	rme_wrk RME is working.
2	RO	0x0	swm_wrk Search window load is working.
1	RO	0x0	cme_wrk CME is working.
0	RO	0x0	pp_wrk Pre-process is working.

**VEPU ST SLI\_NUM**

Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	sli_num Number of slices.

**VEPU DBG DMA RFPR**

Address: Operational Base + offset (0x08E4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	reserved
29:24	RO	0x00	reserved
23:20	RW	0x0	dfifo5_lvl Level of data FIFO5.
19:16	RW	0x0	dfifo4_lvl Level of data FIFO4.
15:12	RO	0x0	reserved
11:8	RO	0x0	reserved
7:4	RO	0x0	reserved
3:0	RO	0x0	reserved

**VEPU DBG DMA CH ST**

Address: Operational Base + offset (0x08E8)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	dspr_otsd DSPR channel read outstanding.
27:16	RW	0x000	rfpr_otsd RFPR channel read outstanding.
15:11	RO	0x00	reserved
10	RO	0x0	reserved
9	RO	0x0	reserved
8	RO	0x0	reserved
7:6	RO	0x0	reserved
5	RO	0x0	reserved
4	RO	0x0	reserved
3	RO	0x0	reserved
2	RO	0x0	reserved
1	RO	0x0	reserved
0	RO	0x0	reserved

**VEPU MMU0 ADDR**

Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu0_dte_addr Page table address for AXI0 MMU0.

**VEPU MMU0 ST**

Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	mmuflt_id ID for the last MMU0 fault.
5	RO	0x0	mmuflt_typ Type of MMU0 fault. 1'h0: Read fault. 1'h1: Write fault.
4	RO	0x0	mmu_rbly_epty MMU0 replay buffer is empty.
3	RO	0x0	mmu_idl MMU0 idle.

Bit	Attr	Reset Value	Description
2	RO	0x0	mmu_stl MMU0 stall.
1	RO	0x0	mmuflt MMU0 page fault.
0	RO	0x0	mmu_e MMU0 is enabled.

**VEPU MMU0 CMD**

Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd MMU0 command. 3'h0: MMU mapping enable. 3'h1: MMU mapping disable. 3'h2: MMU stall enable. 3'h3: MMU stall disable. 3'h4: Zap(disable) page table cache line. 3'h5: Leave fault mode. 3'h6: MMU reset.

**VEPU MMU0 PFA**

Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu_pfa Address of the last page fault.

**VEPU MMU0 ZAP**

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zpa Invalid address for page table cache mapping.

**VEPU MMU0 ERR**

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rb_err Read bus error.
0	RO	0x0	pf_err Page fault error.

**VEPU MMU0 INT CLR**

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_clr Read bus error interrupt clear.
0	RW	0x0	pfe_clr Page fault error interrupt clear.

**VEPU MMU0 INT MSK**

Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_msk Read bus error interrupt mask.
0	RW	0x0	pfe_msk Page fault error interrupt mask.

**VEPU MMU0 INT STA**

Address: Operational Base + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rbe_sta Read bus error interrupt status.
0	RO	0x0	pfe_sta Page fault error interrupt status.

**VEPU MMU0 ACKG**

Address: Operational Base + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_ackg Auto clock gating enable.

**VEPU MMU1 ADDR**

Address: Operational Base + offset (0x0F40)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu1_dte_addr Page table address for AXI1 MMU1.

**VEPU MMU1 ST**

Address: Operational Base + offset (0x0F44)

Bit	Attr	Reset Value	Description
31:11	RO	0x0000000	reserved
10:6	RO	0x00	mmuflt_id ID for the last MMU fault.
5	RO	0x0	mmuflt_typ Type of MMU1 fault. 1'h0: Read fault. 1'h1: Write fault.
4	RO	0x0	mmu_rply_epty MMU1 replay buffer is empty.
3	RO	0x0	mmu_idl MMU1 idle.
2	RO	0x0	mmu_stl MMU1 stall.
1	RO	0x0	mmuflt MMU1 page fault.
0	RO	0x0	mmu_e MMU1 is enabled.

**VEPU MMU1 CMD**

Address: Operational Base + offset (0x0F48)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	mmu_cmd MMU1 command. 3'h0: MMU mapping enable. 3'h1: MMU mapping disable. 3'h2: MMU stall enable. 3'h3: MMU stall disable. 3'h4: Zap(disable) page table cache line. 3'h5: Leave fault mode. 3'h6: MMU reset.

**VEPU MMU1 PFA**

Address: Operational Base + offset (0x0F4C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu_pfa Address of the last page fault.

**VEPU MMU1 ZAP**

Address: Operational Base + offset (0x0F50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zpa Invalid address for page table cache mapping.

**VEPU MMU1 ERR**

Address: Operational Base + offset (0x0F54)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pf_err Page fault error.

**VEPU MMU1 INT CLR**

Address: Operational Base + offset (0x0F58)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_clr Read bus error interrupt clear.
0	RW	0x0	pfe_clr Page fault error interrupt clear.

**VEPU MMU1 INT MSK**

Address: Operational Base + offset (0x0F5C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_msk Read bus error interrupt mask.
0	RW	0x0	pfe_msk Page fault error interrupt mask.

**VEPU MMU1 INT STA**

Address: Operational Base + offset (0x0F60)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rbe_sta Read bus error interrupt status.

Bit	Attr	Reset Value	Description
0	RO	0x0	pfe_sta Page fault error interrupt status.

**VEPU MMU1 ACKG**

Address: Operational Base + offset (0x0F64)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_ackg Auto clock gating enable.

**13.6.18 VEPUS4X LAYER2 Register Address Mapping**

Table 13-11 VEPUS LAYER2 Address Mapping

Name	Offset	Size	Reset Value	Description
VEPU2 IPRD TTHDY4 0 H264	0x0004	W	0x00000000	Texture thresholds register0 for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU2 IPRD TTHD32 0 HEVC	0x0004	W	0x00000000	Texture threshold register0 for HEVC 32x32 intra prediction, share address with H.264.
VEPU2 IPRD TTHDY4 1 H264	0x0008	W	0x00000000	Texture thresholds register1 for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU2 IPRD TTHD32 1 HEVC	0x0008	W	0x00000000	Texture thresholds register1 for HEVC 32x32 intra prediction, share address with H.264.
VEPU2 IPRD TTHDC8 0 H264	0x000C	W	0x00000000	Texture thresholds register0 for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU2 IPRD TTHD16 0 HEVC	0x000C	W	0x00000000	Texture threshold register0 for HEVC 16x16 intra prediction, share address with H.264.
VEPU2 IPRD TTHDC8 1 H264	0x0010	W	0x00000000	Texture thresholds register1 for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU2 IPRD TTHD16 1 HEVC	0x0010	W	0x00000000	Texture threshold register1 for HEVC 16x16 intra prediction, share address with H.264.
VEPU2 IPRD TTHDY8 0 H264	0x0014	W	0x00000000	Texture thresholds register0 for H.264 LUMA 8x8 intra prediction.
VEPU2 IPRD TTHDY8 1 H264	0x0018	W	0x00000000	texture thresholds register1 for H.264 LUMA 8x8 intra prediction.
VEPU2 IPRD TTHD UL H264	0x001C	W	0x00000000	Texture thresholds of up and left MB for H.264 LUMA intra prediction.
VEPU2 IPRD WGTY8 H264	0x0020	W	0x00000000	Teights of the cost for H.264 LUMA 8x8 intra prediction, share address with HEVC.
VEPU2 IPRD WGTY32 0 HEVC	0x0020	W	0x00000000	Tost weights register0 for HEVC LUMA 32x32 intra prediction, share address with H.264.
VEPU2 IPRD WGTY4 H264	0x0024	W	0x00000000	Weights of the cost for H.264 LUMA 4x4 intra prediction, share address with HEVC.

Name	Offset	Size	Reset Value	Description
<u>VEPU2 IPRD WGTY32 1 HEVC</u>	0x0024	W	0x00000000	Cost weights register1 for HEVC LUMA 32x32 intra prediction, share address with H.264.
<u>VEPU2 IPRD WGTY16 H2 64</u>	0x0028	W	0x00000000	Weights of the cost for H.264 LUMA 16x16 intra prediction, share address with HEVC.
<u>VEPU2 IPRD WGTY16 0 HEVC</u>	0x0028	W	0x00000000	Cost weights register0 for HEVC LUMA 16x16 intra prediction.
<u>VEPU2 IPRD WGTC8 H2 64</u>	0x002C	W	0x00000000	Weights of the cost for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
<u>VEPU2 IPRD WGTY16 1 HEVC</u>	0x002C	W	0x00000000	Cost weights register1 for HEVC LUMA 16x16 intra prediction.
<u>VEPU2 QNT BIAS COMB</u>	0x0030	W	0x00000000	Quantization bias for H.264 and HEVC.
<u>VEPU2 ATR THD0 H264</u>	0x0034	W	0x00000000	H.264 anti ringing noise threshold configuration0.
<u>VEPU2 ATR THD1 H264</u>	0x0038	W	0x00000000	H.264 anti ringing noise threshold configuration1.
<u>VEPU2 ATR WGT16 H26 4</u>	0x003C	W	0x00000000	Weights of 16x16 cost for H.264 anti ringing noise.
<u>VEPU2 ATR WGT8 H264</u>	0x0040	W	0x00000000	Weights of 8x8 cost for H.264 anti ringing noise.
<u>VEPU2 ATR WGT4 H264</u>	0x0044	W	0x00000000	Weights of 4x4 cost for H.264 anti ringing noise.
<u>VEPU2 ATF TTHD0 H264</u>	0x0048	W	0x00000000	Texture threshold configuration0 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF TTHD I32 H EVC</u>	0x0048	W	0x00000000	Intra32x32 texture threshold for HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF TTHD1 H264</u>	0x004C	W	0x00000000	Texture threshold configuration1 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF TTHD I16 H EVC</u>	0x004C	W	0x00000000	Intra16x16 texture thresholdfor HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF STHD0 H264</u>	0x0050	W	0x00000000	(CME) SAD threshold configuration0 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF TTHD P64 H EVC</u>	0x0050	W	0x00000000	Inter64x64 texture thresholdfor HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF STHD1 H264</u>	0x0054	W	0x00000000	(CME) SAD threshold configuration1 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF TTHD P32 H EVC</u>	0x0054	W	0x00000000	Inter32x32 texture thresholdfor HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF WGT0 H264</u>	0x0058	W	0x00000000	Weight configuration0 for H.264 anti-flicker, share address with HEVC.

Name	Offset	Size	Reset Value	Description
<u>VEPU2 ATF TTHD P16 H EVC</u>	0x0058	W	0x00000000	Inter16x16 texture threshold for HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF WGT1 H264</u>	0x005C	W	0x00000000	Weight configuration1 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF WGT0 HEVC</u>	0x005C	W	0x00000000	Weight configuration0 for HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF WGT2 H264</u>	0x0060	W	0x00000000	Weight configuration2 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF WGT1 HEVC</u>	0x0060	W	0x00000000	Weight configuration1 for HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF OFST0 H264</u>	0x0064	W	0x00000000	Offset configuration0 for H.264 anti-flicker, share address with HEVC.
<u>VEPU2 ATF WGT2 HEVC</u>	0x0064	W	0x00000000	Weight configuration2 for HEVC anti-flicker, share address with H.264.
<u>VEPU2 ATF OFST1 H264</u>	0x0068	W	0x00000000	Offset configuration1 for H.264 anti-flicker.
<u>VEPU2 ATF OFST2 H264</u>	0x006C	W	0x00000000	Offset configuration2 for H.264 anti-flicker.
<u>VEPU2 IPRD WGT QP0 HEVC</u>	0x0070	W	0x00000000	Weight of SATD cost when QP is 0 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP1 HEVC</u>	0x0074	W	0x00000000	Weight of SATD cost when QP is 1 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP2 HEVC</u>	0x0078	W	0x00000000	Weight of SATD cost when QP is 2 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP3 HEVC</u>	0x007C	W	0x00000000	Weight of SATD cost when QP is 3 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP4 HEVC</u>	0x0080	W	0x00000000	Weight of SATD cost when QP is 4 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP5 HEVC</u>	0x0084	W	0x00000000	Weight of SATD cost when QP is 5 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP6 HEVC</u>	0x0088	W	0x00000000	Weight of SATD cost when QP is 6 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP7 HEVC</u>	0x008C	W	0x00000000	Weight of SATD cost when QP is 7 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP8 HEVC</u>	0x0090	W	0x00000000	Weight of SATD cost when QP is 8 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP9 HEVC</u>	0x0094	W	0x00000000	Weight of SATD cost when QP is 9 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP10 HEVC</u>	0x0098	W	0x00000000	Weight of SATD cost when QP is 10 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP11 HEVC</u>	0x009C	W	0x00000000	Weight of SATD cost when QP is 11 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP12 HEVC</u>	0x00A0	W	0x00000000	Weight of SATD cost when QP is 12 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP13 HEVC</u>	0x00A4	W	0x00000000	Weight of SATD cost when QP is 13 for HEVC intra prediction.



Name	Offset	Size	Reset Value	Description
VEPU2 IPRD WGT QP14 HEVC	0x00A8	W	0x00000000	Weight of SATD cost when QP is 14 for HEVC intra prediction.
VEPU2 IPRD WGT QP15 HEVC	0x00AC	W	0x00000000	Weight of SATD cost when QP is 15 for HEVC intra prediction.
VEPU2 IPRD WGT QP16 HEVC	0x00B0	W	0x00000000	Weight of SATD cost when QP is 16 for HEVC intra prediction.
VEPU2 IPRD WGT QP17 HEVC	0x00B4	W	0x00000000	Weight of SATD cost when QP is 17 for HEVC intra prediction.
VEPU2 IPRD WGT QP18 HEVC	0x00B8	W	0x00000000	Weight of SATD cost when QP is 18 for HEVC intra prediction.
VEPU2 IPRD WGT QP19 HEVC	0x00BC	W	0x00000000	Weight of SATD cost when QP is 19 for HEVC intra prediction.
VEPU2 IPRD WGT QP20 HEVC	0x00C0	W	0x00000000	Weight of SATD cost when QP is 20 for HEVC intra prediction.
VEPU2 IPRD WGT QP21 HEVC	0x00C4	W	0x00000000	Weight of SATD cost when QP is 21 for HEVC intra prediction.
VEPU2 IPRD WGT QP22 HEVC	0x00C8	W	0x00000000	Weight of SATD cost when QP is 22 for HEVC intra prediction.
VEPU2 IPRD WGT QP23 HEVC	0x00CC	W	0x00000000	Weight of SATD cost when QP is 23 for HEVC intra prediction.
VEPU2 IPRD WGT QP24 HEVC	0x00D0	W	0x00000000	Weight of SATD cost when QP is 24 for HEVC intra prediction.
VEPU2 IPRD WGT QP25 HEVC	0x00D4	W	0x00000000	Weight of SATD cost when QP is 25 for HEVC intra prediction.
VEPU2 IPRD WGT QP26 HEVC	0x00D8	W	0x00000000	Weight of SATD cost when QP is 26 for HEVC intra prediction.
VEPU2 IPRD WGT QP27 HEVC	0x00DC	W	0x00000000	Weight of SATD cost when QP is 27 for HEVC intra prediction.
VEPU2 IPRD WGT QP28 HEVC	0x00E0	W	0x00000000	Weight of SATD cost when QP is 28 for HEVC intra prediction.
VEPU2 IPRD WGT QP29 HEVC	0x00E4	W	0x00000000	Weight of SATD cost when QP is 29 for HEVC intra prediction.
VEPU2 IPRD WGT QP30 HEVC	0x00E8	W	0x00000000	Weight of SATD cost when QP is 30 for HEVC intra prediction.
VEPU2 IPRD WGT QP31 HEVC	0x00EC	W	0x00000000	Weight of SATD cost when QP is 31 for HEVC intra prediction.
VEPU2 IPRD WGT QP32 HEVC	0x00F0	W	0x00000000	Weight of SATD cost when QP is 32 for HEVC intra prediction.
VEPU2 IPRD WGT QP33 HEVC	0x00F4	W	0x00000000	Weight of SATD cost when QP is 33 for HEVC intra prediction.
VEPU2 IPRD WGT QP34 HEVC	0x00F8	W	0x00000000	Weight of SATD cost when QP is 34 for HEVC intra prediction.
VEPU2 IPRD WGT QP35 HEVC	0x00FC	W	0x00000000	Weight of SATD cost when QP is 35 for HEVC intra prediction.
VEPU2 IPRD WGT QP36 HEVC	0x0100	W	0x00000000	Weight of SATD cost when QP is 36 for HEVC intra prediction.
VEPU2 IPRD WGT QP37 HEVC	0x0104	W	0x00000000	Weight of SATD cost when QP is 37 for HEVC intra prediction.
VEPU2 IPRD WGT QP38 HEVC	0x0108	W	0x00000000	Weight of SATD cost when QP is 38 for HEVC intra prediction.
VEPU2 IPRD WGT QP39 HEVC	0x010C	W	0x00000000	Weight of SATD cost when QP is 39 for HEVC intra prediction.

Name	Offset	Size	Reset Value	Description
<u>VEPU2 IPRD WGT QP40 HEVC</u>	0x0110	W	0x00000000	Weight of SATD cost when QP is 40 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP41 HEVC</u>	0x0114	W	0x00000000	Weight of SATD cost when QP is 41 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP42 HEVC</u>	0x0118	W	0x00000000	Weight of SATD cost when QP is 42 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP43 HEVC</u>	0x011C	W	0x00000000	Weight of SATD cost when QP is 43 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP44 HEVC</u>	0x0120	W	0x00000000	Weight of SATD cost when QP is 44 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP45 HEVC</u>	0x0124	W	0x00000000	Weight of SATD cost when QP is 45 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP46 HEVC</u>	0x0128	W	0x00000000	Weight of SATD cost when QP is 46 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP47 HEVC</u>	0x012C	W	0x00000000	Weight of SATD cost when QP is 47 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP48 HEVC</u>	0x0130	W	0x00000000	Weight of SATD cost when QP is 48 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP49 HEVC</u>	0x0134	W	0x00000000	Weight of SATD cost when QP is 49 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP50 HEVC</u>	0x0138	W	0x00000000	Weight of SATD cost when QP is 50 for HEVC intra prediction.
<u>VEPU2 IPRD WGT QP51 HEVC</u>	0x013C	W	0x00000000	Weight of SATD cost when QP is 51 for HEVC intra prediction.
<u>VEPU2 RDO WGTA QP0 COMB</u>	0x0140	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 0.
<u>VEPU2 RDO WGTA QP1 COMB</u>	0x0144	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 1.
<u>VEPU2 RDO WGTA QP2 COMB</u>	0x0148	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 2.
<u>VEPU2 RDO WGTA QP3 COMB</u>	0x014C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 3.
<u>VEPU2 RDO WGTA QP4 COMB</u>	0x0150	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 4.
<u>VEPU2 RDO WGTA QP5 COMB</u>	0x0154	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 5.
<u>VEPU2 RDO WGTA QP6 COMB</u>	0x0158	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 6.
<u>VEPU2 RDO WGTA QP7 COMB</u>	0x015C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 7.
<u>VEPU2 RDO WGTA QP8 COMB</u>	0x0160	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 8.
<u>VEPU2 RDO WGTA QP9 COMB</u>	0x0164	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 9.

Name	Offset	Size	Reset Value	Description
<u>VEPU2_RDO_WGTA_QP10_COMB</u>	0x0168	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 10.
<u>VEPU2_RDO_WGTA_QP11_COMB</u>	0x016C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 11.
<u>VEPU2_RDO_WGTA_QP12_COMB</u>	0x0170	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 12.
<u>VEPU2_RDO_WGTA_QP13_COMB</u>	0x0174	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 13.
<u>VEPU2_RDO_WGTA_QP14_COMB</u>	0x0178	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 14.
<u>VEPU2_RDO_WGTA_QP15_COMB</u>	0x017C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 15.
<u>VEPU2_RDO_WGTA_QP16_COMB</u>	0x0180	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 16.
<u>VEPU2_RDO_WGTA_QP17_COMB</u>	0x0184	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 17.
<u>VEPU2_RDO_WGTA_QP18_COMB</u>	0x0188	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 18.
<u>VEPU2_RDO_WGTA_QP19_COMB</u>	0x018C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 19.
<u>VEPU2_RDO_WGTA_QP20_COMB</u>	0x0190	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 20.
<u>VEPU2_RDO_WGTA_QP21_COMB</u>	0x0194	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 21.
<u>VEPU2_RDO_WGTA_QP22_COMB</u>	0x0198	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 22.
<u>VEPU2_RDO_WGTA_QP23_COMB</u>	0x019C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 23.
<u>VEPU2_RDO_WGTA_QP24_COMB</u>	0x01A0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 24.
<u>VEPU2_RDO_WGTA_QP25_COMB</u>	0x01A4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 25.
<u>VEPU2_RDO_WGTA_QP26_COMB</u>	0x01A8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 26.
<u>VEPU2_RDO_WGTA_QP27_COMB</u>	0x01AC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 27.

Name	Offset	Size	Reset Value	Description
<u>VEPU2_RDO_WGTA_QP28_COMB</u>	0x01B0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 28.
<u>VEPU2_RDO_WGTA_QP29_COMB</u>	0x01B4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 29.
<u>VEPU2_RDO_WGTA_QP30_COMB</u>	0x01B8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 30.
<u>VEPU2_RDO_WGTA_QP31_COMB</u>	0x01BC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 31.
<u>VEPU2_RDO_WGTA_QP32_COMB</u>	0x01C0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 32.
<u>VEPU2_RDO_WGTA_QP33_COMB</u>	0x01C4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 33.
<u>VEPU2_RDO_WGTA_QP34_COMB</u>	0x01C8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 34.
<u>VEPU2_RDO_WGTA_QP35_COMB</u>	0x01CC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 35.
<u>VEPU2_RDO_WGTA_QP36_COMB</u>	0x01D0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 36.
<u>VEPU2_RDO_WGTA_QP37_COMB</u>	0x01D4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 37.
<u>VEPU2_RDO_WGTA_QP38_COMB</u>	0x01D8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 38.
<u>VEPU2_RDO_WGTA_QP39_COMB</u>	0x01DC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 39.
<u>VEPU2_RDO_WGTA_QP40_COMB</u>	0x01E0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 40.
<u>VEPU2_RDO_WGTA_QP41_COMB</u>	0x01E4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 41.
<u>VEPU2_RDO_WGTA_QP42_COMB</u>	0x01E8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 42.
<u>VEPU2_RDO_WGTA_QP43_COMB</u>	0x01EC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 43.
<u>VEPU2_RDO_WGTA_QP44_COMB</u>	0x01F0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 44.
<u>VEPU2_RDO_WGTA_QP45_COMB</u>	0x01F4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 45.

Name	Offset	Size	Reset Value	Description
<u>VEPU2_RDO_WGTA_QP46_COMB</u>	0x01F8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 46.
<u>VEPU2_RDO_WGTA_QP47_COMB</u>	0x01FC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 47.
<u>VEPU2_RDO_WGTA_QP48_COMB</u>	0x0200	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 48.
<u>VEPU2_RDO_WGTA_QP49_COMB</u>	0x0204	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 49.
<u>VEPU2_RDO_WGTA_QP50_COMB</u>	0x0208	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 50.
<u>VEPU2_RDO_WGTA_QP51_COMB</u>	0x020C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 51.
<u>VEPU2_RDO_WGTB_QP0_COMB</u>	0x0210	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 0.
<u>VEPU2_RDO_WGTB_QP1_COMB</u>	0x0214	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 1.
<u>VEPU2_RDO_WGTB_QP2_COMB</u>	0x0218	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 2.
<u>VEPU2_RDO_WGTB_QP3_COMB</u>	0x021C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 3.
<u>VEPU2_RDO_WGTB_QP4_COMB</u>	0x0220	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 4.
<u>VEPU2_RDO_WGTB_QP5_COMB</u>	0x0224	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 5.
<u>VEPU2_RDO_WGTB_QP6_COMB</u>	0x0228	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 6.
<u>VEPU2_RDO_WGTB_QP7_COMB</u>	0x022C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 7.
<u>VEPU2_RDO_WGTB_QP8_COMB</u>	0x0230	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 8.
<u>VEPU2_RDO_WGTB_QP9_COMB</u>	0x0234	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 9.
<u>VEPU2_RDO_WGTB_QP10_COMB</u>	0x0238	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 10.
<u>VEPU2_RDO_WGTB_QP11_COMB</u>	0x023C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 11.

Name	Offset	Size	Reset Value	Description
<u>VEPU2_RDO_WGTB_QP12_COMB</u>	0x0240	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 12.
<u>VEPU2_RDO_WGTB_QP13_COMB</u>	0x0244	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 13.
<u>VEPU2_RDO_WGTB_QP14_COMB</u>	0x0248	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 14.
<u>VEPU2_RDO_WGTB_QP15_COMB</u>	0x024C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 15.
<u>VEPU2_RDO_WGTB_QP16_COMB</u>	0x0250	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 16.
<u>VEPU2_RDO_WGTB_QP17_COMB</u>	0x0254	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 17.
<u>VEPU2_RDO_WGTB_QP18_COMB</u>	0x0258	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 18.
<u>VEPU2_RDO_WGTB_QP19_COMB</u>	0x025C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 19.
<u>VEPU2_RDO_WGTB_QP20_COMB</u>	0x0260	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 20.
<u>VEPU2_RDO_WGTB_QP21_COMB</u>	0x0264	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 21.
<u>VEPU2_RDO_WGTB_QP22_COMB</u>	0x0268	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 22.
<u>VEPU2_RDO_WGTB_QP23_COMB</u>	0x026C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 23.
<u>VEPU2_RDO_WGTB_QP24_COMB</u>	0x0270	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 24.
<u>VEPU2_RDO_WGTB_QP25_COMB</u>	0x0274	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 25.
<u>VEPU2_RDO_WGTB_QP26_COMB</u>	0x0278	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 26.
<u>VEPU2_RDO_WGTB_QP27_COMB</u>	0x027C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 27.
<u>VEPU2_RDO_WGTB_QP28_COMB</u>	0x0280	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 28.
<u>VEPU2_RDO_WGTB_QP29_COMB</u>	0x0284	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 29.

Name	Offset	Size	Reset Value	Description
<u>VEPU2_RDO_WGTB_QP30_COMB</u>	0x0288	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 30.
<u>VEPU2_RDO_WGTB_QP31_COMB</u>	0x028C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 31.
<u>VEPU2_RDO_WGTB_QP32_COMB</u>	0x0290	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 32.
<u>VEPU2_RDO_WGTB_QP33_COMB</u>	0x0294	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 33.
<u>VEPU2_RDO_WGTB_QP34_COMB</u>	0x0298	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 34.
<u>VEPU2_RDO_WGTB_QP35_COMB</u>	0x029C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 35.
<u>VEPU2_RDO_WGTB_QP36_COMB</u>	0x02A0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 36.
<u>VEPU2_RDO_WGTB_QP37_COMB</u>	0x02A4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 37.
<u>VEPU2_RDO_WGTB_QP38_COMB</u>	0x02A8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 38.
<u>VEPU2_RDO_WGTB_QP39_COMB</u>	0x02AC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 39.
<u>VEPU2_RDO_WGTB_QP40_COMB</u>	0x02B0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 40.
<u>VEPU2_RDO_WGTB_QP41_COMB</u>	0x02B4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 41.
<u>VEPU2_RDO_WGTB_QP42_COMB</u>	0x02B8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 42.
<u>VEPU2_RDO_WGTB_QP43_COMB</u>	0x02BC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 43.
<u>VEPU2_RDO_WGTB_QP44_COMB</u>	0x02C0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 44.
<u>VEPU2_RDO_WGTB_QP45_COMB</u>	0x02C4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 45.
<u>VEPU2_RDO_WGTB_QP46_COMB</u>	0x02C8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 46.
<u>VEPU2_RDO_WGTB_QP47_COMB</u>	0x02CC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 47.

Name	Offset	Size	Reset Value	Description
<u>VEPU2_RDO_WGTB_QP48_COMB</u>	0x02D0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 48.
<u>VEPU2_RDO_WGTB_QP49_COMB</u>	0x02D4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 49.
<u>VEPU2_RDO_WGTB_QP50_COMB</u>	0x02D8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 50.
<u>VEPU2_RDO_WGTB_QP51_COMB</u>	0x02DC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 51.
<u>VEPU2_MADI_CFG</u>	0x02E0	W	0x00000000	MADI configuration for CU32 and CU64.
<u>VEPU2_AQ_TTHD0</u>	0x02E4	W	0x00000000	Texture threshold configuration0 for adaptive QP adjustment.
<u>VEPU2_AQ_TTHD1</u>	0x02E8	W	0x00000000	Texture threshold configuration1 for adaptive QP adjustment.
<u>VEPU2_AQ_TTHD2</u>	0x02EC	W	0x00000000	Texture threshold configuration2 for adaptive QP adjustment.
<u>VEPU2_AQ_TTHD3</u>	0x02F0	W	0x00000000	Texture threshold configuration3 for adaptive QP adjustment.
<u>VEPU2_AQ_STP0</u>	0x02F4	W	0x00000000	Adjustment step configuration0 for adaptive QP adjustment.
<u>VEPU2_AQ_STP1</u>	0x02F8	W	0x00000000	Adjustment step configuration1 for adaptive QP adjustment.
<u>VEPU2_AQ_STP2</u>	0x02FC	W	0x00000000	Adjustment step configuration2 for adaptive QP adjustment.
<u>VEPU2_AQ_STP3</u>	0x0300	W	0x00000000	Adjustment step configuration3 for adaptive QP adjustment.
<u>VEPU2_RME_MVD_PNSH_H264</u>	0x0304	W	0x00000000	RME MVD(motion vector difference) cost penalty, H.264 only.
<u>VEPU2_ATR1_THD0_H264</u>	0x0308	W	0x00000000	H.264 anti ringing noise threshold configuration0 of group1.
<u>VEPU2_ATR1_THD1_H264</u>	0x030C	W	0x00000000	H.264 anti ringing noise threshold configuration1 of group1.

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

### 13.6.19 VEP54X LAYER2 Detail Register Description

#### VEPU2\_IPRD\_TTHDY4\_0\_H264

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy4_1 The 2nd texture threshold for H.264 LUMA 4x4 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy4_0 The 1st texture threshold for H.264 LUMA 4x4 intra prediction.

#### VEPU2\_IPRD\_TTHD32\_0\_HEVC

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved



Bit	Attr	Reset Value	Description
27:16	RW	0x000	iprd_tthd32_1 The 2nd texture threshold for HEVC 32x32 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd32_0 The 1st texture threshold for HEVC 32x32 intra prediction.

**VEPU2 IPRD TTHDY4 1 H264**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy4_3 The 4th texture threshold for H.264 LUMA 4x4 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy4_2 The 3rd texture threshold for H.264 LUMA 4x4 intra prediction.

**VEPU2 IPRD TTHD32 1 HEVC**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd32_3 The 4th texture threshold for HEVC 32x32 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd32_2 The 3rd texture threshold for HEVC 32x32 intra prediction.

**VEPU2 IPRD TTHDC8 0 H264**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdc8_1 The 2nd texture threshold for H.264 CHROMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdc8_0 The 1st texture threshold for H.264 CHROMA 8x8 intra prediction.

**VEPU2 IPRD TTHD16 0 HEVC**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd16_1 The 2nd texture threshold for HEVC 16x16 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd16_0 The 1st texture threshold for HEVC 16x16 intra prediction.

**VEPU2 IPRD TTHDC8 1 H264**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdc8_3 The 4th texture threshold for H.264 CHROMA 8x8 intra prediction.

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdc8_2 The 3rd texture threshold for H.264 CHROMA 8x8 intra prediction.

**VEPU2 IPRD TTHD16 1 HEVC**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd16_3 The 4th texture threshold for HEVC 16x16 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd16_2 The 3rd texture threshold for HEVC 16x16 intra prediction.

**VEPU2 IPRD TTHDY8 0 H264**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy8_1 The 2nd texture threshold for H.264 LUMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy8_0 The 1st texture threshold for H.264 LUMA 8x8 intra prediction.

**VEPU2 IPRD TTHDY8 1 H264**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy8_3 The 4th texture threshold for H.264 LUMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy8_2 The 3rd texture threshold for H.264 LUMA 8x8 intra prediction.

**VEPU2 IPRD TTHD UL H264**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	iprd_tthd_ul Texture thresholds of up and left MB for H.264 LUMA intra prediction.

**VEPU2 IPRD WGTY8 H264**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty8_3 The 4th cost weight for H.264 LUMA 8x8 intra prediction
23:16	RW	0x00	iprd_wgty8_2 The 3rd cost weight for H.264 LUMA 8x8 intra prediction.
15:8	RW	0x00	iprd_wgty8_1 The 2nd cost weight for H.264 LUMA 8x8 intra prediction.
7:0	RW	0x00	iprd_wgty8_0 The 1st cost weight for H.264 LUMA 8x8 intra prediction.

**VEPU2 IPRD WGTY32 0 HEVC**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty32_3 The 4th cost weight for HEVC LUMA 32x32 intra prediction
23:16	RW	0x00	iprd_wgty32_2 The 3rd cost weight for HEVC LUMA 32x32 intra prediction.
15:8	RW	0x00	iprd_wgty32_1 The 2nd cost weight for HEVC LUMA 32x32 intra prediction.
7:0	RW	0x00	iprd_wgty32_0 The 1st cost weight for HEVC LUMA 32x32 intra prediction.

**VEPU2 IPRD WGTY4 H264**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty4_3 The 4th cost weight for H.264 LUMA 4x4 intra prediction
23:16	RW	0x00	iprd_wgty4_2 The 3rd cost weight for H.264 LUMA 4x4 intra prediction.
15:8	RW	0x00	iprd_wgty4_1 The 2nd cost weight for H.264 LUMA 4x4 intra prediction.
7:0	RW	0x00	iprd_wgty4_0 The 1st cost weight for H.264 LUMA 4x4 intra prediction.

**VEPU2 IPRD WGTY32 1 HEVC**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	iprd_wgty32_6 The 7th cost weight for HEVC LUMA 32x32 intra prediction.
15:8	RW	0x00	iprd_wgty32_5 The 6th cost weight for HEVC LUMA 32x32 intra prediction.
7:0	RW	0x00	iprd_wgty32_4 The 5th cost weight for HEVC LUMA 32x32 intra prediction.

**VEPU2 IPRD WGTY16 H264**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty16_3 The 4th cost weight for H.264 LUMA 16x16 intra prediction.
23:16	RW	0x00	iprd_wgty16_2 The 3rd cost weight for H.264 LUMA 16x16 intra prediction.
15:8	RW	0x00	iprd_wgty16_1 The 2nd cost weight for H.264 LUMA 16x16 intra prediction.
7:0	RW	0x00	iprd_wgty16_0 The 1st cost weight for H.264 LUMA 16x16 intra prediction.

**VEPU2 IPRD WGTY16 0 HEVC**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty16_3 The 4th cost weight for HEVC LUMA 16x16 intra prediction.
23:16	RW	0x00	iprd_wgty16_2 The 3rd cost weight for HEVC LUMA 16x16 intra prediction.

Bit	Attr	Reset Value	Description
15:8	RW	0x00	iprd_wgty16_1 The 2nd cost weight for HEVC LUMA 16x16 intra prediction.
7:0	RW	0x00	iprd_wgty16_0 The 1st cost weight for HEVC LUMA 16x16 intra prediction.

**VEPU2 IPRD WGTC8 H264**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgtc8_3 The 4th cost weight for H.264 CHROMA 8x8 intra prediction.
23:16	RW	0x00	iprd_wgtc8_2 The 3rd cost weight for H.264 CHROMA 8x8 intra prediction.
15:8	RW	0x00	iprd_wgtc8_1 The 2nd cost weight for H.264 CHROMA 8x8 intra prediction.
7:0	RW	0x00	iprd_wgtc8_0 The 1st cost weight for H.264 CHROMA 8x8 intra prediction.

**VEPU2 IPRD WGTY16 1 HEVC**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	iprd_wgty16_6 The 7th cost weight for HEVC LUMA 16x16 intra prediction, share address with H.264.
15:8	RW	0x00	iprd_wgty16_5 The 6th cost weight for HEVC LUMA 16x16 intra prediction.
7:0	RW	0x00	iprd_wgty16_4 The 5th cost weight for HEVC LUMA 16x16 intra prediction.

**VEPU2 QNT BIAS COMB**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	qnt_bias_p Quantization bias for HEVC and H.264 P frame.
9:0	RW	0x000	qnt_bias_i Quantization bias for HEVC and H.264 I frame.

**VEPU2 ATR THD0 H264**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atr_thd1 The 2nd threshold for H.264 anti-ringing-noise.
15:12	RO	0x0	reserved
11:0	RW	0x000	atr_thd0 The 1st threshold for H.264 anti-ringing-noise.

**VEPU2 ATR THD1 H264**

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atr_qp QP threshold of P frame for H.264 anti-ringing-nois.

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x000	atr_thd2 The 3rd threshold for H.264 anti-ringing-noise.

**VEPU2 ATR WGT16 H264**

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv16_wgt2 The 3rd weight for H.264 16x16 anti-ringing-noise.
15:8	RW	0x00	atr_lv16_wgt1 The 2nd weight for H.264 16x16 anti-ringing-noise.
7:0	RW	0x00	atr_lv16_wgt0 The 1st weight for H.264 16x16 anti-ringing-noise.

**VEPU2 ATR WGT8 H264**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv8_wgt2 The 3rd weight for H.264 8x8 anti-ringing-noise.
15:8	RW	0x00	atr_lv8_wgt1 The 2nd weight for H.264 8x8 anti-ringing-noise.
7:0	RW	0x00	atr_lv8_wgt0 The 1st weight for H.264 8x8 anti-ringing-noise.

**VEPU2 ATR WGT4 H264**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv4_wgt2 The 3rd weight for H.264 4x4 anti-ringing-noise.
15:8	RW	0x00	atr_lv4_wgt1 The 2nd weight for H.264 4x4 anti-ringing-noise.
7:0	RW	0x00	atr_lv4_wgt0 The 1st weight for H.264 4x4 anti-ringing-noise.

**VEPU2 ATF TTHD0 H264**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd1 The 2nd texture threshold for H.264 anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st texture threshold for H.264 anti-flicker.

**VEPU2 ATF TTHD I32 HEVC**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_tthd1 The 2nd intra32x32 texture threshold for HEVC anti-flicker.
15:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	atf_tthd0 The 1st intra32x32 texture threshold for HEVC anti-flicker.

**VEPU2 ATF TTHD1 H264**

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd3 The 4th texture threshold for H.264 anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd2 The 3rd texture threshold for H.264 anti-flicker.

**VEPU2 ATF TTHD I16 HEVC**

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_tthd1 The 2nd intra16x16 texture threshold for HEVC anti-flicker.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_tthd0 The 1st intra16x16 texture threshold for HEVC anti-flicker.

**VEPU2 ATF STHD0 H264**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_sthd_max Max (CME) SAD threshold for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_sthd_10 (CME) SAD threshold0 of texture interval1 for H.264 anti-flicker.

**VEPU2 ATF TTHD P64 HEVC**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_tthd1 The 2nd intra64x64 texture threshold for HEVC anti-flicker.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_tthd0 The 1st inter64x64 texture threshold for HEVC anti-flicker.

**VEPU2 ATF STHD1 H264**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_sthd_20 (CME) SAD threshold0 of texture interval2 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_sthd_11 (CME) SAD threshold1 of texture interval1 for H.264 anti-flicker.

**VEPU2 ATF TTHD P32 HEVC**

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_tthd1 The 2nd intra32x32 texture threshold for HEVC anti-flicker.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_tthd0 The 1st inter32x32 texture threshold for HEVC anti-flicker.

**VEPU2 ATF WGT0 H264**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	atf_wgt11 The 2nd weight in texture interval1 for H.264 anti-flicker.
15:9	RO	0x00	reserved
8:0	RW	0x000	atf_wgt10 The 1st weight in texture interval1 for H.264 anti-flicker.

**VEPU2 ATF TTHD P16 HEVC**

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_tthd1 The 2nd intra16x16 texture threshold for HEVC anti-flicker.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_tthd0 The 1st inter16x16 texture threshold for HEVC anti-flicker.

**VEPU2 ATF WGT1 H264**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	atf_wgt20 The 1st weight in texture interval2 for H.264 anti-flicker.
15:9	RO	0x00	reserved
8:0	RW	0x000	atf_wgt12 The 3rd weight in texture interval1 for H.264 anti-flicker.

**VEPU2 ATF WGT0 HEVC**

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_wgt_i32 HEVC intra32x32 anti-flicker weight.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_wgt_i16 HEVC intra16x16 anti-flicker weight.

**VEPU2 ATF WGT2 H264**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	atf_wgt30 The weight in texture interval3 for H.264 anti-flicker.

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8:0	RW	0x000	atf_wgt21 The 2nd weight in texture interval2 for H.264 anti-flicker.

**VEPU2 ATF WGT1 HEVC**

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_wgt_p64 HEVC inter64x64 anti-flicker weight.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_wgt_p32 HEVC inter32x32 anti-flicker weight.

**VEPU2 ATF OFST0 H264**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_ofst11 The 2nd offset in texture interval1 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_ofst10 The 1st offset in texture interval1 for H.264 anti-flicker.

**VEPU2 ATF WGT2 HEVC**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	atf_wgt_p16 HEVC inter16x16 anti-flicker weight.

**VEPU2 ATF OFST1 H264**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_ofst20 The 1st offset in texture interval2 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_ofst12 The 3rd offset in texture interval1 for H.264 anti-flicker.

**VEPU2 ATF OFST2 H264**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_ofst30 The offset in texture interval3 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_ofst21 The 2nd offset in texture interval2 for H.264 anti-flicker.

**VEPU2 IPRD WGT QP0 HEVC**

Address: Operational Base + offset (0x0070)



Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp0 Weight of SATD cost when QP is 0 for HEVC intra prediction.

**VEPU2 IPRD WGT QP1 HEVC**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp1 Weight of SATD cost when QP is 1 for HEVC intra prediction.

**VEPU2 IPRD WGT QP2 HEVC**

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp2 Weight of SATD cost when QP is 2 for HEVC intra prediction.

**VEPU2 IPRD WGT QP3 HEVC**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp3 Weight of SATD cost when QP is 3 for HEVC intra prediction.

**VEPU2 IPRD WGT QP4 HEVC**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp4 Weight of SATD cost when QP is 4 for HEVC intra prediction.

**VEPU2 IPRD WGT QP5 HEVC**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp5 Weight of SATD cost when QP is 5 for HEVC intra prediction.

**VEPU2 IPRD WGT QP6 HEVC**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp6 Weight of SATD cost when QP is 6 for HEVC intra prediction.

**VEPU2 IPRD WGT QP7 HEVC**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp7 Weight of SATD cost when QP is 7 for HEVC intra prediction.

**VEPU2 IPRD WGT QP8 HEVC**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp8 Weight of SATD cost when QP is 8 for HEVC intra prediction.

**VEPU2 IPRD WGT QP9 HEVC**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp9 Weight of SATD cost when QP is 9 for HEVC intra prediction.

**VEPU2 IPRD WGT QP10 HEVC**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp10 Weight of SATD cost when QP is 10 for HEVC intra prediction.

**VEPU2 IPRD WGT QP11 HEVC**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp11 Weight of SATD cost when QP is 11 for HEVC intra prediction.

**VEPU2 IPRD WGT QP12 HEVC**

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp12 Weight of SATD cost when QP is 12 for HEVC intra prediction.

**VEPU2 IPRD WGT QP13 HEVC**

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp13 Weight of SATD cost when QP is 13 for HEVC intra prediction.

**VEPU2 IPRD WGT QP14 HEVC**

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp14 Weight of SATD cost when QP is 14 for HEVC intra prediction.

**VEPU2 IPRD WGT QP15 HEVC**

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp15 Weight of SATD cost when QP is 15 for HEVC intra prediction.

**VEPU2 IPRD WGT QP16 HEVC**

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp16 Weight of SATD cost when QP is 16 for HEVC intra prediction.

**VEPU2 IPRD WGT QP17 HEVC**

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp17 Weight of SATD cost when QP is 17 for HEVC intra prediction.

**VEPU2 IPRD WGT QP18 HEVC**

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp18 Weight of SATD cost when QP is 18 for HEVC intra prediction.

**VEPU2 IPRD WGT QP19 HEVC**

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp19 Weight of SATD cost when QP is 19 for HEVC intra prediction.

**VEPU2 IPRD WGT QP20 HEVC**

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp20 Weight of SATD cost when QP is 20 for HEVC intra prediction.

**VEPU2 IPRD WGT QP21 HEVC**

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp21 Weight of SATD cost when QP is 21 for HEVC intra prediction.

**VEPU2 IPRD WGT QP22 HEVC**

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp2 Weight of SATD cost when QP is 2 for HEVC intra prediction.

**VEPU2 IPRD WGT QP23 HEVC**

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp23 Weight of SATD cost when QP is 23 for HEVC intra prediction.

**VEPU2 IPRD WGT QP24 HEVC**

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp24 Weight of SATD cost when QP is 24 for HEVC intra prediction.

**VEPU2 IPRD WGT QP25 HEVC**

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp25 Weight of SATD cost when QP is 25 for HEVC intra prediction.

**VEPU2 IPRD WGT QP26 HEVC**

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp26 Weight of SATD cost when QP is 26 for HEVC intra prediction.

**VEPU2 IPRD WGT QP27 HEVC**

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp27 Weight of SATD cost when QP is 27 for HEVC intra prediction.

**VEPU2 IPRD WGT QP28 HEVC**

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp28 Weight of SATD cost when QP is 28 for HEVC intra prediction.

**VEPU2 IPRD WGT QP29 HEVC**

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp29 Weight of SATD cost when QP is 29 for HEVC intra prediction.

**VEPU2 IPRD WGT QP30 HEVC**

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp30 Weight of SATD cost when QP is 30 for HEVC intra prediction.

**VEPU2 IPRD WGT QP31 HEVC**

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	wgt_qp31 Weight of SATD cost when QP is 31 for HEVC intra prediction.

**VEPU2 IPRD WGT QP32 HEVC**

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp32 Weight of SATD cost when QP is 32 for HEVC intra prediction.

**VEPU2 IPRD WGT QP33 HEVC**

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp33 Weight of SATD cost when QP is 33 for HEVC intra prediction.

**VEPU2 IPRD WGT QP34 HEVC**

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp34 Weight of SATD cost when QP is 34 for HEVC intra prediction.

**VEPU2 IPRD WGT QP35 HEVC**

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp35 Weight of SATD cost when QP is 35 for HEVC intra prediction.

**VEPU2 IPRD WGT QP36 HEVC**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp36 Weight of SATD cost when QP is 36 for HEVC intra prediction.

**VEPU2 IPRD WGT QP37 HEVC**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp37 Weight of SATD cost when QP is 37 for HEVC intra prediction.

**VEPU2 IPRD WGT QP38 HEVC**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp38 Weight of SATD cost when QP is 38 for HEVC intra prediction.

**VEPU2 IPRD WGT QP39 HEVC**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp39 Weight of SATD cost when QP is 39 for HEVC intra prediction.

**VEPU2 IPRD WGT QP40 HEVC**

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp40 Weight of SATD cost when QP is 40 for HEVC intra prediction.

**VEPU2 IPRD WGT QP41 HEVC**

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp41 Weight of SATD cost when QP is 41 for HEVC intra prediction.

**VEPU2 IPRD WGT QP42 HEVC**

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp42 Weight of SATD cost when QP is 42 for HEVC intra prediction.

**VEPU2 IPRD WGT QP43 HEVC**

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp43 Weight of SATD cost when QP is 43 for HEVC intra prediction.

**VEPU2 IPRD WGT QP44 HEVC**

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp44 Weight of SATD cost when QP is 44 for HEVC intra prediction.

**VEPU2 IPRD WGT QP45 HEVC**

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp45 Weight of SATD cost when QP is 45 for HEVC intra prediction.

**VEPU2 IPRD WGT QP46 HEVC**

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp46 Weight of SATD cost when QP is 46 for HEVC intra prediction.

**VEPU2 IPRD WGT QP47 HEVC**

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp47 Weight of SATD cost when QP is 47 for HEVC intra prediction.

**VEPU2 IPRD WGT QP48 HEVC**

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp48 Weight of SATD cost when QP is 48 for HEVC intra prediction.

**VEPU2 IPRD WGT QP49 HEVC**

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp49 Weight of SATD cost when QP is 49 for HEVC intra prediction.

**VEPU2 IPRD WGT QP50 HEVC**

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp50 Weight of SATD cost when QP is 50 for HEVC intra prediction.

**VEPU2 IPRD WGT QP51 HEVC**

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp51 Weight of SATD cost when QP is 51 for HEVC intra prediction.

**VEPU2 RDO WGTA QP0 COMB**

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp0_grpa Weight of group A for HEVC and H.264 RDO mode decision when QP is 0.

**VEPU2 RDO WGTA QP1 COMB**

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp1_grpa Weight of group A for HEVC and H.264 RDO mode decision when QP is 1.

**VEPU2 RDO WGTA QP2 COMB**

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp2_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 2.

**VEPU2 RDO WGTA QP3 COMB**

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp3_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 3.

**VEPU2 RDO WGTA QP4 COMB**

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp4_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 4.

**VEPU2 RDO WGTA QP5 COMB**

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp5_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 5.

**VEPU2 RDO WGTA QP6 COMB**

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp6_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 6.

**VEPU2 RDO WGTA QP7 COMB**

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp7_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 7.

**VEPU2 RDO WGTA QP8 COMB**

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp8_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 8.

**VEPU2 RDO WGTA QP9 COMB**

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp9_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 9.

**VEPU2 RDO WGTA QP10 COMB**

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp10_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 10.

**VEPU2 RDO WGTA QP11 COMB**

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp11_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 11.

**VEPU2 RDO WGTA QP12 COMB**

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp12_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 12.

**VEPU2 RDO WGTA QP13 COMB**

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp13_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 13.

**VEPU2 RDO WGTA QP14 COMB**

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp14_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 14.

**VEPU2 RDO WGTA QP15 COMB**

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp15_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 15.

**VEPU2 RDO WGTA QP16 COMB**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp16_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 16.

**VEPU2 RDO WGTA QP17 COMB**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp17_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 17.

**VEPU2 RDO WGTA QP18 COMB**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp18_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 18.

**VEPU2 RDO WGTA QP19 COMB**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp19_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 19.

**VEPU2 RDO WGTA QP20 COMB**

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp20_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 20.

**VEPU2 RDO WGTA QP21 COMB**

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp21_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 21.

**VEPU2 RDO WGTA QP22 COMB**

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp22_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 22.

**VEPU2 RDO WGTA QP23 COMB**

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp23_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 23.

**VEPU2 RDO WGTA QP24 COMB**

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp24_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 24.

**VEPU2 RDO WGTA QP25 COMB**

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp25_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 25.

**VEPU2 RDO WGTA QP26 COMB**

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp26_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 26.

**VEPU2 RDO WGTA QP27 COMB**

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp27_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 27.

**VEPU2 RDO WGTA QP28 COMB**

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp28_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 28.

**VEPU2 RDO WGTA QP29 COMB**

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp29_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 29.

**VEPU2 RDO WGTA QP30 COMB**

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp30_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 30.

**VEPU2 RDO WGTA QP31 COMB**

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp31_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 31.

**VEPU2 RDO WGTA QP32 COMB**

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp32_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 32.

**VEPU2 RDO WGTA QP33 COMB**

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp33_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 33.

**VEPU2 RDO WGTA QP34 COMB**

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp34_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 34.

**VEPU2 RDO WGTA QP35 COMB**

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp35_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 35.

**VEPU2 RDO WGTA QP36 COMB**

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp36_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 36.

**VEPU2 RDO WGTA QP37 COMB**

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp37_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 37.

**VEPU2 RDO WGTA QP38 COMB**

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp38_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 38.

**VEPU2 RDO WGTA QP39 COMB**

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp39_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 39.

**VEPU2 RDO WGTA QP40 COMB**

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp0_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 40.

**VEPU2 RDO WGTA QP41 COMB**

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp41_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 41.

**VEPU2 RDO WGTA QP42 COMB**

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp42_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 42.

**VEPU2 RDO WGTA QP43 COMB**

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp43_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 43.

**VEPU2 RDO WGTA QP44 COMB**

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp44_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 44.

**VEPU2 RDO WGTA QP45 COMB**

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp45_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 5.

**VEPU2 RDO WGTA QP46 COMB**

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp46_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 46.

**VEPU2 RDO WGTA QP47 COMB**

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp47_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 47.

**VEPU2 RDO WGTA QP48 COMB**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp48_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 48.

**VEPU2 RDO WGTA QP49 COMB**

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp9_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 49.

**VEPU2 RDO WGTA QP50 COMB**

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp50_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 50.

**VEPU2 RDO WGTB QP51 COMB**

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp51_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 51.

**VEPU2 RDO WGTB QP0 COMB**

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp0_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 0.

**VEPU2 RDO WGTB QP1 COMB**

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp1_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 1.

**VEPU2 RDO WGTB QP2 COMB**

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp2_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 2.

**VEPU2 RDO WGTB QP3 COMB**

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp3_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 3.

**VEPU2 RDO WGTB QP4 COMB**

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp4_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 4.

**VEPU2 RDO WGTB QP5 COMB**

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp5_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 5.

**VEPU2 RDO WGTB QP6 COMB**

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp6_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 6.

**VEPU2 RDO WGTB QP7 COMB**

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp7_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 7.

**VEPU2 RDO WGTB QP8 COMB**

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp8_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 8.

**VEPU2 RDO WGTB QP9 COMB**

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp9_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 9.

**VEPU2 RDO WGTB QP10 COMB**

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp10_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 10.

**VEPU2 RDO WGTB QP11 COMB**

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp11_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 11.



**VEPU2 RDO WGTB QP12 COMB**

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp12_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 12.

**VEPU2 RDO WGTB QP13 COMB**

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp13_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 13.

**VEPU2 RDO WGTB QP14 COMB**

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp14_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 14.

**VEPU2 RDO WGTB QP15 COMB**

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp15_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 15.

**VEPU2 RDO WGTB QP16 COMB**

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp16_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 16.

**VEPU2 RDO WGTB QP17 COMB**

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp17_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 17.

**VEPU2 RDO WGTB QP18 COMB**

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp18_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 18.

**VEPU2 RDO WGTB QP19 COMB**

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp19_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 19.

**VEPU2 RDO WGTB QP20 COMB**

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp20_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 20.

**VEPU2 RDO WGTB QP21 COMB**

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp21_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 21.

**VEPU2 RDO WGTB QP22 COMB**

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp22_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 22.

**VEPU2 RDO WGTB QP23 COMB**

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp23_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 23.

**VEPU2 RDO WGTB QP24 COMB**

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp24_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 24.

**VEPU2 RDO WGTB QP25 COMB**

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp25_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 25.

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp25_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 25.

**VEPU2 RDO WGTB QP26 COMB**

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp26_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 26.

**VEPU2 RDO WGTB QP27 COMB**

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp27_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 27.

**VEPU2 RDO WGTB QP28 COMB**

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp28_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 28.

**VEPU2 RDO WGTB QP29 COMB**

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp29_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 29.

**VEPU2 RDO WGTB QP30 COMB**

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp30_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 30.

**VEPU2 RDO WGTB QP31 COMB**

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp31_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 31.

**VEPU2 RDO WGTB QP32 COMB**

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp32_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 32.

**VEPU2 RDO WGTB QP33 COMB**

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp33_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 3.

**VEPU2 RDO WGTB QP34 COMB**

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp34_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 34.

**VEPU2 RDO WGTB QP35 COMB**

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp35_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 35.

**VEPU2 RDO WGTB QP36 COMB**

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp36_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 36.

**VEPU2 RDO WGTB QP37 COMB**

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp37_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 37.

**VEPU2 RDO WGTB QP38 COMB**

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp38_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 38.

**VEPU2 RDO WGTB QP39 COMB**

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp39_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 39.

**VEPU2 RDO WGTB QP40 COMB**

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp40_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 40.

**VEPU2 RDO WGTB QP41 COMB**

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp41_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 41.

**VEPU2 RDO WGTB QP42 COMB**

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp42_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 42.

**VEPU2 RDO WGTB QP43 COMB**

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp43_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 43.

**VEPU2 RDO WGTB QP44 COMB**

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp44_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 44.

**VEPU2 RDO WGTB QP45 COMB**

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp45_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 45.

**VEPU2\_RDO\_WGTB\_QP46\_COMB**

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp46_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 46.

**VEPU2\_RDO\_WGTB\_QP47\_COMB**

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp47_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 47.

**VEPU2\_RDO\_WGTB\_QP48\_COMB**

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp48_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 48.

**VEPU2\_RDO\_WGTB\_QP49\_COMB**

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp49_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 49.

**VEPU2\_RDO\_WGTB\_QP50\_COMB**

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp50_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 50.

**VEPU2\_RDO\_WGTB\_QP51\_COMB**

Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp51_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 51.

**VEPU2\_MADI\_CFG**

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	madi_mode MADI generation mode for CU32 and CU64. 1'h0: Follow 32x32 and 64x64 MADI functions. 1'h1: Calculated by the mean of corresponding CU16 MADIs.

**VEPU2 AQ TTHD0**

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd3 Texture threshold3 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd2 Texture threshold2 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd1 Texture threshold1 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd0 Texture threshold0 for adaptive QP adjustment.

**VEPU2 AQ TTHD1**

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd7 Texture threshold7 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd6 Texture threshold6 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd5 Texture threshold5 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd4 Texture threshold4 for adaptive QP adjustment.

**VEPU2 AQ TTHD2**

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd11 Texture threshold7 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd10 Texture threshold10 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd9 Texture threshold9 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd8 Texture threshold8 for adaptive QP adjustment.

**VEPU2 AQ TTHD3**

Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd15 Texture threshold15 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd14 Texture threshold14 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd13 Texture threshold13 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd12 Texture threshold12 for adaptive QP adjustment.

**VEPU2 AQ STP0**

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_2t3 QP adjust step when current texture strength $\geq$ aq_tthd2 and $<$ aq_tthd3.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_1t2 QP adjust step when current texture strength $\geq$ aq_tthd1 and $<$ aq_tthd2.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_0t1 QP adjust step when current texture strength $\geq$ aq_tthd0 and $<$ aq_tthd1.
7:6	RO	0x0	reserved
5:0	RW	0x00	aq_stp_s0 QP adjust step when current texture strength $<$ aq_tthd0.

**VEPU2 AQ\_STP1**

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_6t7 QP adjust step when current texture strength $\geq$ aq_tthd6 and $<$ aq_tthd7.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_5t6 QP adjust step when current texture strength $\geq$ aq_tthd5 and $<$ aq_tthd6.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_4t5 QP adjust step when current texture strength $\geq$ aq_tthd4 and $<$ aq_tthd5.
7:6	RO	0x0	reserved
5:0	RW	0x00	ap_stp_3t4 QP adjust step when current texture strength $\geq$ aq_tthd3 and $<$ aq_tthd4.

**VEPU2 AQ\_STP2**

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_11t12 QP adjust step when current texture strength $>$ aq_tthd11 and $\leq$ aq_tthd12.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_10t11 QP adjust step when current texture strength $>$ aq_tthd10 and $\leq$ aq_tthd11.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_9t10 QP adjust step when current texture strength $>$ aq_tthd9 and $\leq$ aq_tthd10.
7:6	RO	0x0	reserved



Bit	Attr	Reset Value	Description
5:0	RW	0x00	ap_stp_8t9 QP adjust step when current texture strength > aq_tthd8 and <= aq_tthd9.

**VEPU2 AQ STP3**

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_b15 QP adjust step when current texture strength > aq_tthd15.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_14t15 QP adjust step when current texture strength > aq_tthd14 and <= aq_tthd15.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_13t14 QP adjust step when current texture strength > aq_tthd13 and <= aq_tthd14.
7:6	RO	0x0	reserved
5:0	RW	0x00	ap_stp_12t13 QP adjust step when current texture strength > aq_tthd12 and <= aq_tthd13.

**VEPU2 RME MVD PNSH H264**

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	mvd_pnsh_hthd High threshold of the MVs which should be punished.
23:20	RW	0x0	mvd_pnsh_lthd Low threshold of the MVs which should be punished.
19:6	RW	0x0000	mvd_pnsh_cnst MVD cost punishment constant.
5:1	RW	0x00	mvd_pnsh_coef MVD punishment coefficient.
0	RW	0x0	mvd_pnsh_e MVD cost punishment enable.

**VEPU2 ATR1 THD0 H264**

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atr1_thd1 The 2nd threshold for H.264 anti-ringing-noise of group1.
15:12	RO	0x0	reserved
11:0	RW	0x000	atr1_thd0 The 1st threshold for H.264 anti-ringing-noise of group1.

**VEPU2 ATR1 THD1 H264**

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	atr1_thd2 The 3rd threshold for H.264 anti-ringing-noise of group1.

## 13.7 Interface Description

Table 13-12 VEPU54x Interface Description

Module Pin	Direction	Description
clk_core	I	VEPU core clock
resetrn_core	I	Asynchronous reset of core clock domain, low active
clk_axi	I	VEPU AXI clock
resetrn_axi	I	Asynchronous reset of AXI clock domain, low active
clk_ahb	I	VEPU AHB clock
resetrn_ahb	I	Asynchronous reset of AHB clock domain, low active
*_ahb	I/O	32bit width AHB slave port for register configuration
o_enc_int	O	Interrupt, high active
*_axi0	I/O	64-bit write/128-bit read AXI master port
*_axi1	I/O	128-bit read AXI master port

Notes: I=input, O=output, I/O=input/output, bidirectional

VEPU accesses DDR through \*\_axi0 and \*\_axi1

## 13.8 Application Notes

### 13.8.1 MMU Config Flow

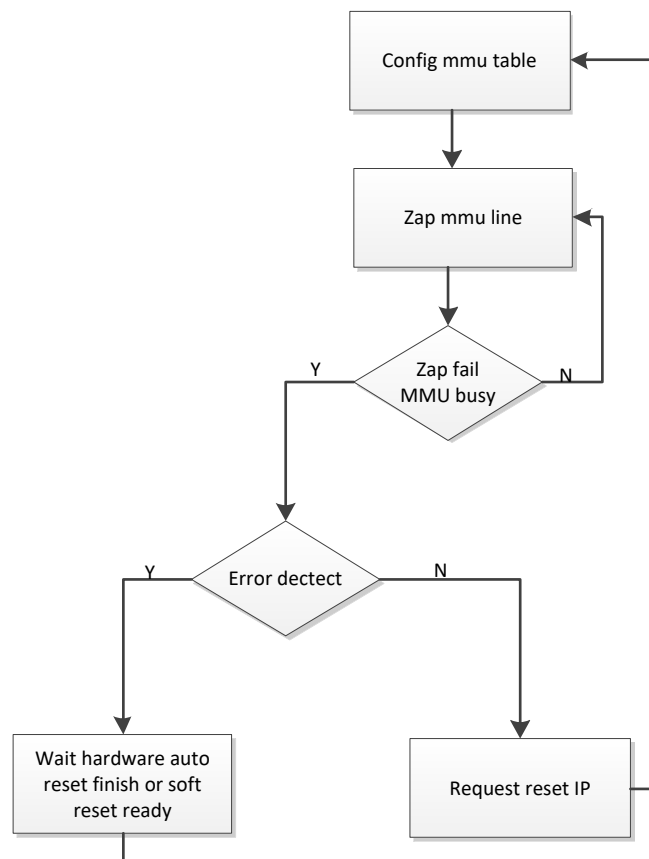


Fig. 13-11 MMU config flow

1. Prepare mmu table to ddr and config DTE address before begin to decoder.
2. If the mmu table have been changed, you will zap one mmu line.
3. If you zap succeeded, you can continus to zap next line.
4. If you zap fail, maybe some error happened, then you should check if there any error happen when decoding.
5. If some error happen, you should wait reset finish, and then re-start mmu config.
6. If don't have any error find, it will still need to reset, and then re-start mmu config.

### 13.8.2 VDPU345 H265 Configuration Flow

1. Prepare the data in the DDR.
2. Set the H265 general system configuration in RKVDEC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with RKVDEC.swreg3.
4. Set the input and output data base address and H265 reference configuration with RKVDEC.swreg4~RKVDEC.swreg43.
5. If CABAC error detection is desired, set the RKVDEC.swreg44 to enable the corresponding error detection.
6. Set the interrupt configuration and start the H265 with H265.swreg1.
7. Wait for the frame interrupt, and then get the processed results in the target DDR.
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

### 13.8.3 VDPU345 H264 Configuration Flow

1. Prepare the data in the DDR, for normal mode, we should prepare bitstream, tbl, pps and rps.
2. Set the H264 general system configuration in RKVDEC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with RKVDEC.swreg3.
4. Set the input and output data base address and H264 reference configuration with RKVDEC.swreg4~RKVDEC.swreg43.
5. If stream error detection is desired, set the swreg77\_H264\_error\_e and swreg44\_strmd\_error\_en to enable the corresponding error detection.
6. If prefetch function is desired, set the prefetch common registers and clear its TLB. Pay attention, there contains two caches, which are for Y channel and UV channel.
7. If MMU function is desired, set the MMU common registers and clear its TLB. Pay attention, there contains two MMUs, which are for read channel and write channel.
8. Set the interrupt configuration and start the decoder with RKVDEC.swreg1.
9. Wait for the frame interrupt, and then get the processed results in the target DDR. There may be decoded frame, error\_info, cur frame colmv output.  
When the stream mode is not frame by frame mode, we also wait buf empty, and then send the next pack, repeat it until sw\_dec\_rdy\_sta.
10. Clear all the interrupts, and repeat Process2~Process9 to start a new frame decoding if the decoding is not finished yet.

### 13.8.4 VDPU345 Link table Pointer mode configuration flow

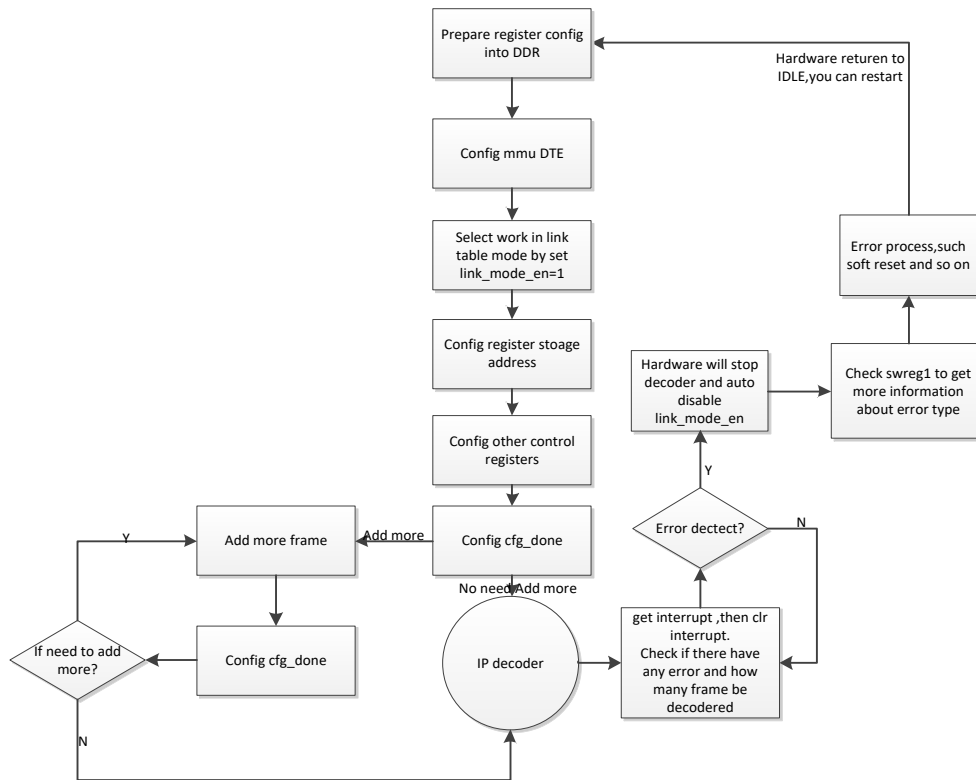


Fig. 13-12 Link table Pointer mode work flow

- 14 Prepare all the register config value into DDR.
  - 15 Config mmu DTE and enable mmu before config link table mode.
  - 16 Config link\_mode\_irq and other link table mode register. The register is from link\_tale\_swreg0~link\_table\_swreg2.
  - 17 Config config\_done(set link\_table\_swreg3[0]=1'b1) to make the link table register configuration effect, after that, hardware will begin to decoder frame by frame.
  - 18 If you need to add more frame, you can use superaddition mode, you can add more frame when decoder at any status.
  - 19 If all config be rdy, you should enable the working flag by config link\_mode\_en (link\_table\_swreg6[0]) to 1.
  - 20 If all the frame be decoded, the hardware will hold the working status wait user to process, you can add more frame or set link\_mode\_en=0(need to set config\_done=1'b1) to finish link table mode.
  - 21 When you get interrupt, at first, you should clear the irq, and then, goto check if there have any error by check link\_table\_swreg4[31]=1'b1 or not. If any error found by hardware, the hardware will disable link table mode and stop decoder until user restart next link table mode. And then you can get more information about error type from normal register swreg1.
9. When you get interrupt, if there doesn't have any error, you may be to check the frame number which have been decoded.
10. Please note that: Any link table register be config, you need to config swreg3[0]=1'b1 to make it effective.

### 13.8.5 VPU121 JPEG decoder and encoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used. And please notice that which be list as follows:
  - For encoder: We can configure the registers to control the input picture data format (such as endian and swap), but some input data format are fixed, such as cabac\_table data. And the register VEPUSWREG0~31 are JPEG quantization registers. They are write only registers. When you want to write these registers, you should first set

VEPU\_SWREG103[0] to 1'b0 and VEPUSWREG103[5:4] to 2'b10( select JPEG mode).

- For decoder: The decoder can support ref buffer mode or cacheable mode, but they can't be both enabled. We can config the swreg57[28],swreg57[29] to enable cache and config the swreg65 to control the ref buffer.
4. You should config VDPUSWREG57[0] as 1'b1 to enable video decoder. And config VDPUSWREG41[0] as 1'b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPUSWREG41[4] as 1'b1 and then config VDPUSWREG57[0] as 1'b1 to enable decoder and pp. VEPUSWREG103[0] set to 1'b1 to enable encoder.
  5. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
  6. Clear all the interrupts, repeat step 2~5 to start a new frame decoder or encoder.
  7. Please note that before you config h.264 encoder to work, you should need config GRF\_SOC\_CON3[11] to 1'b0.

### 13.8.6 VEPUS4X Layer2 Register Access

User can access VEPUS Layer2 registers through VEPUS\_L2CFG\_ADDR(0x03f0), VEPUS\_L2CFG\_WDATA(0x03f4) and VEPUS\_L2CFG\_RDATA(0x03f8) in Layer1.

Example1: write "DATAx" into layer2 address "ADDRx"

- Write(VEPUS\_L2CFG\_ADDR, "ADDRx")
- Write(VEPUS\_L2CFG\_WDATA, "DATAx")

Example2: read back "DATAx" from layer2 register "ADDRx"

- Write(VEPUS\_L2CFG\_ADDR, "ADDRx")
- Read(VEPUS\_L2CFG\_RDATA, "DATAx")

To increase configuration speed, VEPUS also support "burst mode" which auto increase VEPUS\_L2CFG\_ADDR after write to VEPUS\_L2CFG\_WDATA or read L2CFG\_RDATA if VEPUS\_L2CFG\_WDATA.burst\_mode is 1.

Example3: write DATA[0~3] into layer2 address "ADDRx", "ADDRx+4", "ADDRx+8", "ADDRx+12" continuously.

- Write(VEPUS\_L2CFG\_ADDR, "ADDRx"|32'h1)
- Write(VEPUS\_L2CFG\_WDATA, "DATA[0]")
- Write(VEPUS\_L2CFG\_WDATA, "DATA[1]")
- Write(VEPUS\_L2CFG\_WDATA, "DATA[2]")
- Write(VEPUS\_L2CFG\_WDATA, "DATA[3]")

Example4: read 4 "DATA[0~4]" from layer2 registers with the address of "ADDRx", "ADDRx+4", "ADDRx+8" and "ADDRx+12" continuously.

- Write(VEPUS\_L2CFG\_ADDR, "ADDRx"|32'h1)
- Read(VEPUS\_L2CFG\_RDATA, "DATA[0]")
- Read(VEPUS\_L2CFG\_RDATA, "DATA[1]")
- Read(VEPUS\_L2CFG\_RDATA, "DATA[2]")
- Read(VEPUS\_L2CFG\_RDATA, "DATA[3]")

### 13.8.7 VEPUS4X Buffer Allocation

User should allocates the following buffers and informs VEPUS before the corresponding frame encoding starts.

- Video source buffer
- (ROI) block level configuration buffer
- Reference frame buffer
- Current frame buffer
- Collocated MV buffer
- Current MV buffer
- Down-sampled reference frame buffer
- Down-sampled current frame buffer
- Motion information buffer
- Bitstream buffer

#### 13.8.7.1 Video Source Buffer

Depending on different video source format, there're up to 3 buffers should be configured. When video source format is BGRA8888, RGB888, RGB565, YUYV422 or UYVY422, only one buffer should be allocated and LAYER1.VEPUS\_ADR\_SRC0(0x0118) should be set to the buffer start address.

When video source format is arm AFBC (YUV420 or YUV422), LAYER1.VEPU\_ADR\_SRC0 should be set to the start address of "AFBC header portion". LAYER1.VEPU\_ADR\_SRC1 should be set to the address of which the "AFBC body portion" offset base on (layer1.ADR\_SRC0 and layer1.ADR\_SRC1 are the same in most cases).

When video source format is YUV420 or YUV 422 semi-planar, LAYER1.VEPU\_ADR\_SRC0 should be set to the LUMA component start address, LAYER1.VEPU\_ADR\_SRC1 should be set to the CHROMA component start address.

Otherwise (YUV420 or YUV422 planar), LAYER1.VEPU\_ADR\_SRC0 should be set to the Y component start address, LAYER1.ADR\_SRC1 should be set to the U component start address, and LAYER1.VEPU\_ADR\_SRC2 should be set to the V component start address.

#### **13.8.7.2 Block Level Configure Buffer**

This buffer should be allocated and configured when LAYER1.VEPU\_ENC\_PIC.roi\_en is 1. The size of block level configure buffer is:

$((\text{LAYER1.VEPU\_ENC\_RSL.pic\_wd8\_m1}+8)/8) \times$   
 $((\text{LAYER1.VEPU\_ENC\_RSL.pic\_hd8\_m1}+8)/8) \times 32\text{Bytes}.$

#### **13.8.7.3 Current And Reference Frame Buffer**

Reference frame buffer and current frame buffer store the reconstructed frame data for motion estimation. Because of that frame buffer compression is implemented, each buffer has head portion and body portion. LAYER1.VEPU\_ADR\_RFPW\_H and LAYER1.VEPU\_ADR\_RFPW\_B should be set to the head portion and body portion start address of current frame buffer separately. LAYER1.VEPU\_ADR\_RFPR\_H and LAYER1.VEPU\_ADR\_RFPR\_B should be set to the header portion and body portion start address of reference frame buffer.

The size of head portion of current and reference frame buffer is:

$((\text{LAYER1.VEPU\_ENC\_RSL.pic\_wd8\_m1}+2)/2) \times$   
 $((\text{LAYER1.VEPU\_ENC\_RSL.pic\_hd8\_m1}+1) \times 2) + 15) / 16 \times 16\text{Bytes}.$

The size of body portion of current and reference frame buffer is:

$((\text{LAYER1.VEPU\_ENC\_RSL.pic\_wd8\_m1}+2)/2) \times$   
 $((\text{LAYER1.VEPU\_ENC\_RSL.pic\_hd8\_m1}+1) \times 2) \times 96\text{Bytes}.$

Note that the head and body start address should be 4K byte aligned.

#### **13.8.7.4 Col-Mv Buffer And Cur-Mv buffer**

Col-Mv buffer and Cur-Mv buffer stores the col-mv information for HEVC encoding.

When LAYER1.VEPU\_ME\_CFG.colmv\_stor is 1, the LAYER1.VEPU\_ADR\_CMVW should be set to the start address of Cur-Mv buffer. VEPU will store the col-mv information of current encoding frame into Cur-Mv buffer.

When LAYER1.VEPU\_ME\_CFG.colmv\_load is 1, the LAYER1.VEPU\_ADR\_CMVR should be set to the start address of Col-Mv buffer. VEPU will load the col-mv information for MVP generation.

The size of Col-Mv buffer and Cur-Mv buffer is calculated by the following function:

$((\text{LAYER1.VEPU\_ENC\_RSL.pic\_wd8\_m1}+8)/8) \times$   
 $((\text{LAYER1.VEPU\_ENC\_RSL.pic\_hd8\_m1}+8)/8) \times 32\text{Bytes}.$

Note that the start address of col-mv and cur-mv buffer should be 1K byte aligned.

#### **13.8.7.5 Down-sampled Current and Reference Frame Buffer**

Down-sampled frame buffer is for VEPU coarse motion estimation. If current frame will be referred in subsequent encoding, the down-sampled current frame buffer should be allocated and set the start address to LAYER1.VEPU\_ADR\_DSPW. If current frame is P frame, a reference frame buffer should be selected and set the start address to LAYER1.VEPU\_ADR\_DSPR.

The size of down-sampled frame buffer is:

$((\text{LAYER1.VEPU\_ENC\_RSL.pic\_wd8\_m1}+8)/8) \times$   
 $((\text{LAYER1.VEPU\_ENC\_RSL.pic\_hd8\_m1}+2)/2) \times 64\text{Bytes}.$

Note that the start address of down-sampled frame buffer should be 1KB aligned.

#### **13.8.7.6 Motion Information Buffer**

When LAYER1.VEPU\_ENC\_PIC.mei\_stor is 1, the motion information buffer should be allocated and set the start address to LAYER1.VEPU\_ADR\_MEIW. VEPU stores best motion vector and corresponding SAD into this buffer just for user extended extraction.

The size of motion information buffer is:

$((\text{LAYER1.VEPU\_ENC\_RSL.pic\_wd8\_m1}+32)/32) \times (\text{LAYER1.VEPU\_ENC\_RSL.pic\_hd8\_m1}+1) \times 2 \times 64\text{Bytes}$ .

### 13.8.7.7 Bit Stream Buffer

VEPU stores the encoding result (bit stream) into bit stream buffer.

There are 4 address pointers for one bit stream buffer management:

- LAYER1.VEPU\_ADR\_BSBT: buffer top address, not included.
- LAYER1.VEPU\_ADR\_BSBB: buffer bottom address, included.
- LAYER1.VEPU\_ADR\_BSBR: buffer read address to avoid overlap.
- LAYER1.VEPU\_ADR\_BSBW: buffer write start address.

Two types of buffer management strategy can be implemented by configuring the four address pointers: single buffer and cyclic buffer management.

Single buffer management allocates a new buffer for each frame while cyclic buffer management allocates a shared cyclic buffer for all encoding frames.

Interrupt LAYER1.VEPU\_INT\_STUS.bs\_ovflr will assert when write address meets read address (which indicates buffer is full) and encoding process is paused. Driver should allocated a new buffer to continue current frame encoding by setting new values to the four address pointers or change buffer read address (read out the bitstream before that), and then the encoding process will continue.

Note that LAYER1.VEPU\_ADR\_BSBW must be configured after the other 3 address pointers.

### 13.8.8 VEPU54X Link Table Mode

VEPU54X supports a batch process mode named "link table mode". It will increase the interaction efficiency between hardware and software. CPU can stores the configuration for several frames in DDR before encoding or add new frames to be encoded when VEPU is processing the previous one. This will save the time of interrupt response and register configuration and let VEPU and software process in parallel.

The struct contains one frame configuration in DDR is called node. It contains the LAYER1 register configuration and status from address 0x0030 to 0x002C. VEPU will load the node and replace corresponding LAYER1 registers automatically.

Note that only the registers between LAYER1 0x0030 to 0x002C can be re-configured in link table mode, other configurations can not be changed.

When LAYER1.VEPU\_INT\_EN.lkt\_done\_en is 1, the interrupt of

LAYER1.VEPU\_INT\_STA.lkt\_done\_sta will assert after each frame encoding whose

LAYER1.VEPU\_ENC\_PIC.node\_int is 1. User can set dedicated frame interrupt such as the last node of link table. LAYER1.VEPU\_ST\_LKT.fnum\_int contains the number of frames have been encoded when interrupt is assert.

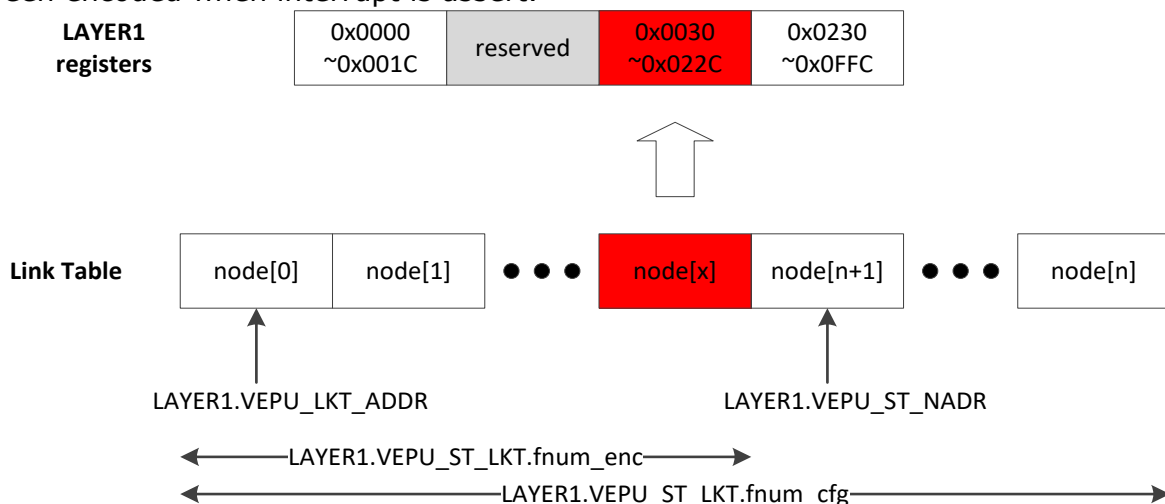


Fig. 13-13 VEPU Link Table Introduction

### 13.8.9 VEPU54X ROI Application

User can adjust QP and inter/intra selection base on 16x16 block and stores the configurations in block level configuration buffer. Each 16x16 block has 16 bits ROI configuration struct as the table listed below.

Table 13-13 ROI Configuration Structure

Bit	Field	Description
15	qp_mode	QP adjustment mode 0: absolute QP 1: relative QP
14:8	qp_value	QP adjustment value This field is the absolute QP when qp_mode is 0, otherwise it's the relative QP base on corresponding 16x16 block's QP
7	amap_en	Area map enable
6:4	amap_idx	Area map index. QP clip is implemented base on area map index, each map index has its dedicated threshold. ROI configuration mapping will use amap_idx to arbitrate the final configure when CU size is bigger than 16x16. Bigger amap_idx has higher priority.
3:1	reserved	Reserved
0	force_intra	Force intra encoding

The configuration structures of different blocks are stored in the order of raster scanning within a frame.

### 13.8.10 VEPU54X OSD Application

VEPU has 8 rectangular OSD areas, which insert user defined picture into encoding frames. The top left and bottom right ordinate for each OSD area is assigned by LAYER1.VEPU\_OSD0~7\_POS, and the materials buffer assigned by LAYER1.VEPU\_ADR\_OSD0~7.

VEPU's OSD material bases on palette. LAYER1.VEPU\_OSD\_CFG.osd\_plt\_typ selects the type of palette: default OSD palette has only 8 colors while user defined OSD palette (configured by LAYER1.VEPU\_OSD\_PLT0~255) supports up to 256 colors.

Note that LAYER1.VEPU\_OSD\_CFG.osd\_plt\_cks should be 0 when configure and be 1 when encoding.

### 13.8.11 VEPU54X Safe Clear

Safe Clear confirms the integrity of BUS transaction. It will discard the (AXI) transactions have not sent out and complete all outstanding ones. To implement safe clear, software should set LAYER1.VEPU\_ENC\_CLR to 1, and wait for LAYER1.VEPU\_ST\_STUS.clr\_fnsh interrupt. After that pull down VEPU asynchronous reset port to perform force reset.



## Chapter 14 Crypto

### 14.1 Overview

Crypto is a hardware accelerator for encrypting or decrypting. The Crypto supports following features:

- Support Link List Item (LLI) DMA transfer
- Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
- Support HMAC of SHA-1, SHA-256, SHA-512, MD5 with hardware padding
- Support AES-128, AES-256 encrypt & decrypt cipher
- Support DES & TDES cipher
- Support SM2/SM3/SM4 cipher
- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC
- Support up to 8-channels configuration
- Support up to 256 bit TRNG output

### 14.2 Block Diagram

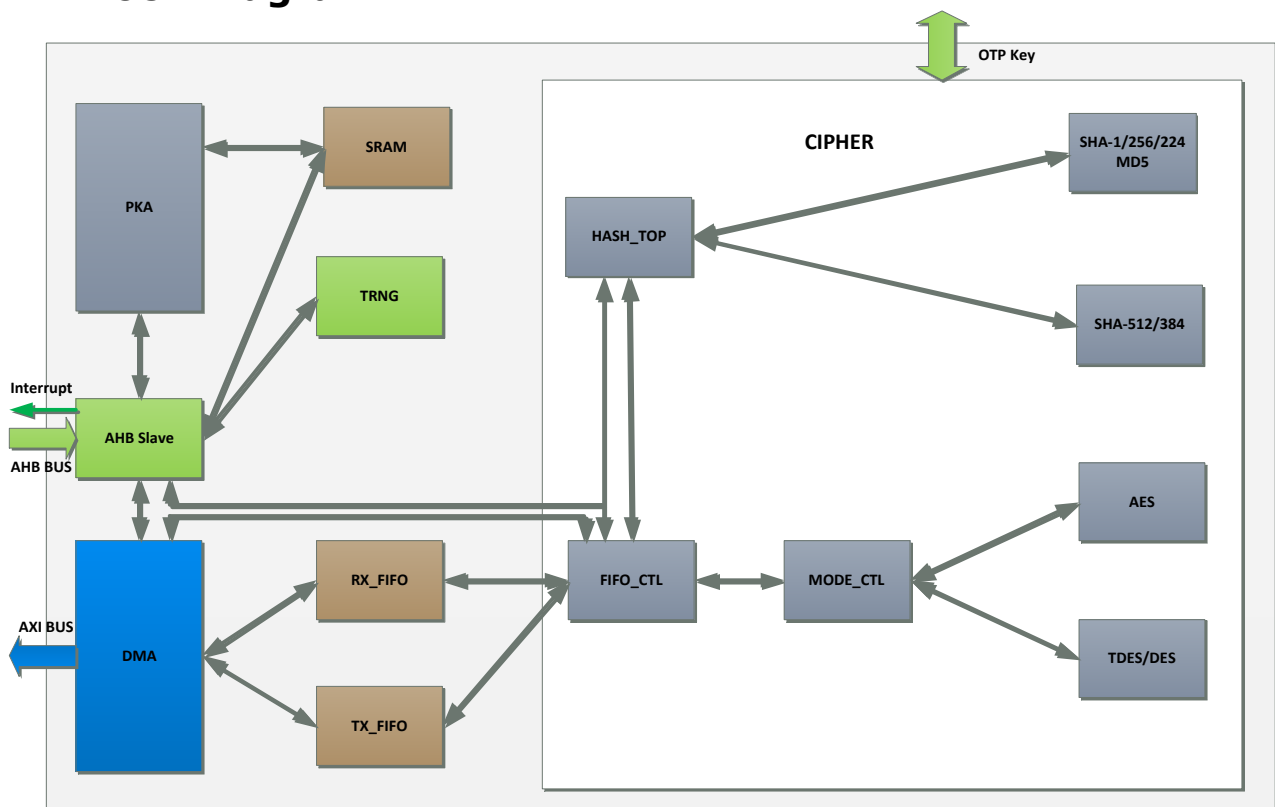


Fig. 14-1 Crypto Architecture

Crypto contains several modules: AHB\_Slave, DMA, CIPHER, PKA, TRNG.

#### AHB\_Slave

AHB\_Slave is used to configure registers. This module is in HCLK domain.

#### DMA

DMA is used to transfer data from external memory to RX\_FIFO, or from TX\_FIFO to external memory. DMA uses 64-bits AXI3 protocol with max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in ACLK domain.

#### CIPHER

CIPHER contains AES, DES/TDES and HASH engines. And it also supports various mode operations. The source data is either from RX\_FIFO, or from other engine output. The result data is sending either to TX\_FIFO, or Registers in module AHB\_Slave. This module is in CLK\_CORE domain.

#### PKA

PKA is used to accelerate mathematical operations for big numbers. It supports - Modular arithmetic (addition, subtraction, multiplication and division), Regular arithmetic (addition, subtraction, multiplication and division), Modular inversion, Modular exponentiation, Logical operations (AND, OR, XOR, SHIFT). PKA has a SRAM which is used to store source, result and intermediate data for PKA operations. The software driver could use PKA operations to implement complicate calculation, such as RSA, ECC etc. It could support up to 4096 bits RSA modular exponentiation calculation. This module is in CLK\_PKA domain.

#### TRNG

TRNG is used to collect random bits from the ring oscillator, up to 256 random bits per time. This module is in HCLK domain.

### 14.3 Register Description

#### 14.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

#### 14.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
<u>CRYPTO_CLK_CTL</u>	0x0000	W	0x00000001	Clock Control Register
<u>CRYPTO_RST_CTL</u>	0x0004	W	0x00000000	Reset Control Register
<u>CRYPTO_DMA_INT_EN</u>	0x0008	W	0x00000000	DMA Interrupt Enable Register
<u>CRYPTO_DMA_INT_ST</u>	0x000C	W	0x00000000	DMA Interrupt Status Register
<u>CRYPTO_DMA_CTL</u>	0x0010	W	0x00000000	DMA Control Register
<u>CRYPTO_DMA_LLI_ADDR</u>	0x0014	W	0x00000000	DMA LIST Start Address Register
<u>CRYPTO_DMA_ST</u>	0x0018	W	0x00000000	DMA Status Register
<u>CRYPTO_DMA_STATE</u>	0x001C	W	0x00000000	DMA State Register
<u>CRYPTO_DMA_LLI_RADDR</u>	0x0020	W	0x00000000	DMA LLI Read Address Register
<u>CRYPTO_DMA_SRC_RADDR</u>	0x0024	W	0x00000000	DMA Source Data Read Address Register
<u>CRYPTO_DMA_DST_WADDR</u>	0x0028	W	0x00000000	DMA Destination Data Read Address Register
<u>CRYPTO_DMA_ITEM_ID</u>	0x002C	W	0x00000000	DMA Descriptor ID Register
<u>CRYPTO_FIFO_CTL</u>	0x0040	W	0x00000003	FIFO Control Register
<u>CRYPTO_BC_CTL</u>	0x0044	W	0x00000000	Block Cipher Control Register
<u>CRYPTO_HASH_CTL</u>	0x0048	W	0x00000004	Hash Control Register
<u>CRYPTO_CIPHER_ST</u>	0x004C	W	0x00000000	Cipher Status Register
<u>CRYPTO_CIPHER_STATE</u>	0x0050	W	0x00000400	Cipher Current State Register
<u>CRYPTO_CHn_IV_0</u>	0x0100	W	0x00000000	Channel n range from 0 to 7. CHn_IV_0 address = 0x0100 + 0x10 * n. For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.
<u>CRYPTO_CHn_IV_1</u>	0x0104	W	0x00000000	Channel n range from 0 to 7. CHn_IV_1 address = 0x0104 + 0x10 * n. For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.
<u>CRYPTO_CHn_IV_2</u>	0x0108	W	0x00000000	Channel n range from 0 to 7. CHn_IV_2 address = 0x0108 + 0x10 * n. For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

Name	Offset	Size	Reset Value	Description
<u>CRYPTO CHn IV 3</u>	0x010C	W	0x00000000	Channel n range from 0 to 7. CHn_IV_3 address = $0x010c + 0x10 * n$ . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.
<u>CRYPTO CHn KEY 0</u>	0x0180	W	0x00000000	Channel n range from 0 to 7. CHn_KEY_0 address = $0x0180 + 0x10 * n$ .
<u>CRYPTO CHn KEY 1</u>	0x0184	W	0x00000000	Channel n range from 0 to 7. CHn_KEY_1 address = $0x0184 + 0x10 * n$ .
<u>CRYPTO CHn KEY 2</u>	0x0188	W	0x00000000	Channel n range from 0 to 7. CHn_KEY_2 address = $0x0188 + 0x10 * n$ .
<u>CRYPTO CHn KEY 3</u>	0x018C	W	0x00000000	Channel n range from 0 to 7. CHn_KEY_3 address = $0x018c + 0x10 * n$ .
<u>CRYPTO CHn PKEY 0</u>	0x0200	W	0x00000000	Channel n range from 0 to 7. CHn_PKEY_0 address = $0x0200 + 0x10 * n$ .
<u>CRYPTO CHn PKEY 1</u>	0x0204	W	0x00000000	Channel n range from 0 to 7. CHn_PKEY_1 address = $0x0204 + 0x10 * n$ .
<u>CRYPTO CHn PKEY 2</u>	0x0208	W	0x00000000	Channel n range from 0 to 7. CHn_PKEY_2 address = $0x208 + 0x10 * n$ .
<u>CRYPTO CHn PKEY 3</u>	0x020C	W	0x00000000	Channel n range from 0 to 7. CHn_PKEY_3 address = $0x020c + 0x10 * n$ .
<u>CRYPTO CHn PC LEN 0</u>	0x0280	W	0x00000000	Channel n range from 0 to 7. CHn_PC_LEN_0 address = $0x0280 + 0x8 * n$ . Length in byte unit.
<u>CRYPTO CHn PC LEN 1</u>	0x0284	W	0x00000000	Channel n range from 0 to 7. CHn_PC_LEN_1 address = $0x0284 + 0x8 * n$ . Length in byte unit.
<u>CRYPTO CHn AAD LEN 0</u>	0x02C0	W	0x00000000	Channel n range from 0 to 7. CHn_AAD_LEN_0 address = $0x02c0 + 0x8 * n$ . Length in byte unit.
<u>CRYPTO CHn AAD LEN 1</u>	0x02C4	W	0x00000000	Channel n range from 0 to 7. CHn_AAD_LEN_1 address = $0x02c4 + 0x8 * n$ . Length in byte unit.
<u>CRYPTO CHn IV LEN 0</u>	0x0300	W	0x00000000	Channel n range from 0 to 7. CHn_IV_LEN_0 address = $0x0300 + 0x4 * n$ . Length in byte unit.
<u>CRYPTO CHn TAG 0</u>	0x0320	W	0x00000000	Channel n range from 0 to 7. CHn_TAG_0 address = $0x0320 + 0x10 * n$ . When the corresponding TAG_VALID is high, TAG value is valid.

Name	Offset	Size	Reset Value	Description
<u>CRYPTO CHn TAG 1</u>	0x0324	W	0x00000000	Channel n range from 0 to 7. CHn_TAG_1 address = $0x0324 + 0x10 * n$ . When the corresponding TAG_VALID is high, TAG value is valid.
<u>CRYPTO CHn TAG 2</u>	0x0328	W	0x00000000	Channel n range from 0 to 7. CHn_TAG_2 address = $0x0328 + 0x10 * n$ . When the corresponding TAG_VALID is high, TAG value is valid.
<u>CRYPTO CHn TAG 3</u>	0x032C	W	0x00000000	Channel n range from 0 to 7. CHn_TAG_3 address = $0x032c + 0x10 * n$ . When the corresponding TAG_VALID is high, TAG value is valid.
<u>CRYPTO HASH DOUT 0</u>	0x03A0	W	0x00000000	HASH Data Output Register 0
<u>CRYPTO HASH DOUT 1</u>	0x03A4	W	0x00000000	HASH Data Output Register 1
<u>CRYPTO HASH DOUT 2</u>	0x03A8	W	0x00000000	HASH Data Output Register 2
<u>CRYPTO HASH DOUT 3</u>	0x03AC	W	0x00000000	HASH Data Output Register 3
<u>CRYPTO HASH DOUT 4</u>	0x03B0	W	0x00000000	HASH Data Output Register 4
<u>CRYPTO HASH DOUT 5</u>	0x03B4	W	0x00000000	HASH Data Output Register 5
<u>CRYPTO HASH DOUT 6</u>	0x03B8	W	0x00000000	HASH Data Output Register 6
<u>CRYPTO HASH DOUT 7</u>	0x03BC	W	0x00000000	HASH Data Output Register 7
<u>CRYPTO HASH DOUT 8</u>	0x03C0	W	0x00000000	HASH Data Output Register 8
<u>CRYPTO HASH DOUT 9</u>	0x03C4	W	0x00000000	HASH Data Output Register 9
<u>CRYPTO HASH DOUT 10</u>	0x03C8	W	0x00000000	HASH Data Output Register 10
<u>CRYPTO HASH DOUT 11</u>	0x03CC	W	0x00000000	HASH Data Output Register 11
<u>CRYPTO HASH DOUT 12</u>	0x03D0	W	0x00000000	HASH Data Output Register 12
<u>CRYPTO HASH DOUT 13</u>	0x03D4	W	0x00000000	HASH Data Output Register 13
<u>CRYPTO HASH DOUT 14</u>	0x03D8	W	0x00000000	HASH Data Output Register 14
<u>CRYPTO HASH DOUT 15</u>	0x03DC	W	0x00000000	HASH Data Output Register 15
<u>CRYPTO TAG VALID</u>	0x03E0	W	0x00000000	TAG Valid Register
<u>CRYPTO HASH VALID</u>	0x03E4	W	0x00000000	HASH Output Valid Register
<u>CRYPTO VERSION</u>	0x03F0	W	0x01000001	CRYPTO Version Number Register
<u>CRYPTO RNG CTL</u>	0x0400	W	0x0000000C	RNG Control Register
<u>CRYPTO RNG SAMPLE CNT</u>	0x0404	W	0x00000000	RNG Sample Counter Register
<u>CRYPTO RNG DOUT 0</u>	0x0410	W	0x00000000	RNG Data Output Register 0
<u>CRYPTO RNG DOUT 1</u>	0x0414	W	0x00000000	RNG Data Output Register 1
<u>CRYPTO RNG DOUT 2</u>	0x0418	W	0x00000000	RNG Data Output Register 2
<u>CRYPTO RNG DOUT 3</u>	0x041C	W	0x00000000	RNG Data Output Register 3
<u>CRYPTO RNG DOUT 4</u>	0x0420	W	0x00000000	RNG Data Output Register 4
<u>CRYPTO RNG DOUT 5</u>	0x0424	W	0x00000000	RNG Data Output Register 5
<u>CRYPTO RNG DOUT 6</u>	0x0428	W	0x00000000	RNG Data Output Register 6
<u>CRYPTO RNG DOUT 7</u>	0x042C	W	0x00000000	RNG Data Output Register 7
<u>CRYPTO RAM CTL</u>	0x0480	W	0x00000000	RAM Control Register
<u>CRYPTO RAM ST</u>	0x0484	W	0x00000001	RAM Status Register

Name	Offset	Size	Reset Value	Description
CRYPTO_DEBUG_CTL	0x04A0	W	0x00000000	PKA Debug Control Register
CRYPTO_DEBUG_ST	0x04A4	W	0x00000001	PKA Debug Status Register
CRYPTO_DEBUG_MONITOR	0x04A8	W	0x0000FEEF	PKA Debug Monitor Bus Register
CRYPTO_PKA_MEM_MAP0	0x0800	W	0x00000000	PKA Memory Map 0 Register
CRYPTO_PKA_MEM_MAP1	0x0804	W	0x00000000	PKA Memory Map 1 Register
CRYPTO_PKA_MEM_MAP2	0x0808	W	0x00000000	PKA Memory Map 2 Register
CRYPTO_PKA_MEM_MAP3	0x080C	W	0x00000000	PKA Memory Map 3 Register
CRYPTO_PKA_MEM_MAP4	0x0810	W	0x00000000	PKA Memory Map 4 Register
CRYPTO_PKA_MEM_MAP5	0x0814	W	0x00000000	PKA Memory Map 5 Register
CRYPTO_PKA_MEM_MAP6	0x0818	W	0x00000000	PKA Memory Map 6 Register
CRYPTO_PKA_MEM_MAP7	0x081C	W	0x00000000	PKA Memory Map 7 Register
CRYPTO_PKA_MEM_MAP8	0x0820	W	0x00000000	PKA Memory Map 8 Register
CRYPTO_PKA_MEM_MAP9	0x0824	W	0x00000000	PKA Memory Map 9 Register
CRYPTO_PKA_MEM_MAP10	0x0828	W	0x00000000	PKA Memory Map 10 Register
CRYPTO_PKA_MEM_MAP11	0x082C	W	0x00000000	PKA Memory Map 11 Register
CRYPTO_PKA_MEM_MAP12	0x0830	W	0x00000000	PKA Memory Map 12 Register
CRYPTO_PKA_MEM_MAP13	0x0834	W	0x00000000	PKA Memory Map 13 Register
CRYPTO_PKA_MEM_MAP14	0x0838	W	0x00000000	PKA Memory Map 14 Register
CRYPTO_PKA_MEM_MAP15	0x083C	W	0x00000000	PKA Memory Map 15 Register
CRYPTO_PKA_MEM_MAP16	0x0840	W	0x00000000	PKA Memory Map 16 Register
CRYPTO_PKA_MEM_MAP17	0x0844	W	0x00000000	PKA Memory Map 17 Register
CRYPTO_PKA_MEM_MAP18	0x0848	W	0x00000000	PKA Memory Map 18 Register
CRYPTO_PKA_MEM_MAP19	0x084C	W	0x00000000	PKA Memory Map 19 Register
CRYPTO_PKA_MEM_MAP20	0x0850	W	0x00000000	PKA Memory Map 20 Register
CRYPTO_PKA_MEM_MAP21	0x0854	W	0x00000000	PKA Memory Map 21 Register
CRYPTO_PKA_MEM_MAP22	0x0858	W	0x00000000	PKA Memory Map 22 Register
CRYPTO_PKA_MEM_MAP23	0x085C	W	0x00000000	PKA Memory Map 23 Register
CRYPTO_PKA_MEM_MAP24	0x0860	W	0x00000000	PKA Memory Map 24 Register
CRYPTO_PKA_MEM_MAP25	0x0864	W	0x00000000	PKA Memory Map 25 Register
CRYPTO_PKA_MEM_MAP26	0x0868	W	0x00000000	PKA Memory Map 26 Register
CRYPTO_PKA_MEM_MAP27	0x086C	W	0x00000000	PKA Memory Map 27 Register
CRYPTO_PKA_MEM_MAP28	0x0870	W	0x00000000	PKA Memory Map 28 Register
CRYPTO_PKA_MEM_MAP29	0x0874	W	0x00000000	PKA Memory Map 29 Register
CRYPTO_PKA_MEM_MAP30	0x0878	W	0x00000000	PKA Memory Map 30 Register
CRYPTO_PKA_MEM_MAP31	0x087C	W	0x00000000	PKA Memory Map 31 Register
CRYPTO_PKA_OPCODE	0x0880	W	0x00000000	PKA Operation Code Register
CRYPTO_N_NP_TO_T1_ADDR	0x0884	W	0x000FF820	N_NP_TO_T1_ADDR Register
CRYPTO_PKA_STATUS	0x0888	W	0x00000001	PKA Status Register
CRYPTO_PKA_SW_RESET	0x088C	W	0x00000000	software reset of PKA
CRYPTO_PKA_L0	0x0890	W	0x00000000	PKA Length 0 Register
CRYPTO_PKA_L1	0x0894	W	0x00000000	PKA Length 1 Register
CRYPTO_PKA_L2	0x0898	W	0x00000000	PKA Length 2 Register
CRYPTO_PKA_L3	0x089C	W	0x00000000	PKA Length 3 Register
CRYPTO_PKA_L4	0x08A0	W	0x00000000	PKA Length 4 Register
CRYPTO_PKA_L5	0x08A4	W	0x00000000	PKA Length 5 Register
CRYPTO_PKA_L6	0x08A8	W	0x00000000	PKA Length 6 Register
CRYPTO_PKA_L7	0x08AC	W	0x00000000	PKA Length 7 Register
CRYPTO_PKA_PIPE_RDY	0x08B0	W	0x00000001	PKA ready for new Operation Code.
CRYPTO_PKA_DONE	0x08B4	W	0x00000001	PKA Done Register
CRYPTO_PKA_MON_SELECT	0x08B8	W	0x00000000	PKA Monitor Select Register

Name	Offset	Size	Reset Value	Description
CRYPTO PKA DEBUG REG EN	0x08BC	W	0x00000000	PKA Debug Enable Register
CRYPTO DEBUG CNT ADDR	0x08C0	W	0x00000000	Debug Counter Address Register
CRYPTO DEBUG EXT ADDR	0x08C4	W	0x00000000	Debug Extra Address Register
CRYPTO PKA DEBUG HALT	0x08C8	W	0x00000000	PKA Debug Halt State Register
CRYPTO PKA MON READ	0x08D0	W	0x0000FEEF	PKA Monitor Read Register
CRYPTO PKA INT ENA	0x08D4	W	0x00000000	PKA Interrupt Enable Register
CRYPTO PKA INT ST	0x08D8	W	0x00000000	PKA Interrupt Status Register
CRYPTO SRAM ADDR	0x1000	W	0x00000000	SRAM Base Address

Notes: **Size: B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access **DW**- Double WORD (64 bits) access

### 14.3.3 Detail Registers Description

#### CRYPTO CLK CTL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0000	reserved
0	RW	0x1	auto_clkgate_en CRYPTO will gate unused Block Cipher and HASH module automatically. 1'b0: Disable 1'b1: Enable

#### CRYPTO RST CTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:3	RO	0x0000	reserved
2	R/WSC	0x0	sw_pka_reset Software set this bit to start a reset to PKA module. After the reset is done, CRYPTO will clear this bit.
1	R/WSC	0x0	sw_rng_reset Software set this bit to start a reset to TRNG module. After the reset is done, CRYPTO will clear this bit.
0	R/WSC	0x0	sw_cc_reset Software set this bit to start a reset to Symmetric Cipher and HASH module. After the reset is done, CRYPTO will clear this bit.

#### CRYPTO DMA INT EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	zero_len_int_en 1'b1: Enable 1'b0: Disable
5	RW	0x0	list_err_int_en 1'b1: Enable 1'b0: Disable
4	RW	0x0	src_err_int_en 1'b1: Enable 1'b0: Disable
3	RW	0x0	dst_err_int_en 1'b1: Enable 1'b0: Disable
2	RW	0x0	src_item_done_int_en 1'b1: Enable 1'b0: Disable
1	RW	0x0	dst_item_done_int_en 1'b1: Enable 1'b0: Disable
0	RW	0x0	list_done_int_en 1'b1: Enable 1'b0: Disable

**CRYPTO\_DMA\_INT\_ST**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	W1C	0x0	zero_len 1'b1: Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use. 1'b0: Nothing
5	RO	0x0	reserved
4	W1C	0x0	src_err 1'b1: Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use. 1'b0: Nothing
3	W1C	0x0	dst_err 1'b1: Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use. 1'b0: Nothing
2	W1C	0x0	src_item_done 1'b1: Indicate that DMA has completed a read transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use. 1'b0: Nothing
1	W1C	0x0	dst_item_done 1'b1: Indicate that DMA has completed a write transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use. 1'b0: Nothing

Bit	Attr	Reset Value	Description
0	W1C	0x0	list_done 1'b1: Indicate that DMA has completed all the transfers which the list descriptors pointed to. After the bit is read, the application should write 1 to clear this bit for next time use. 1'b0: Nothing

**CRYPTO DMA CTL**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:2	RO	0x0000	reserved
1	R/WSC	0x0	dma_restart If DMA data for next stage is not ready, application could pause DMA by descriptor commands. DMA will stop prefetching next descriptor. The application could restart DMA by asserting this bit when DMA data for next state is ready. Crypto will continue with previous transfer, and clear the bit automatically.
0	R/WSC	0x0	dma_start DMA asserts the bit to start DMA transfer, then Crypto will clear the bit automatically.

**CRYPTO DMA LLI ADDR**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_lll_addr When DMA_CTL start asserted, Crypto will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lll_addr 64-byte align for best performance consideration.

**CRYPTO DMA ST**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dma_busy 1'b1: Dma busy 1'b0: Dma idle

**CRYPTO DMA STATE**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:6	RO	0x00000000	reserved
5:4	RO	0x0	dma_lll_state For debug use only. 2'b00: IDLE STATE 2'b01: FETCH STATE 2'b10: WORK STATE Others: Reserved.



Bit	Attr	Reset Value	Description
3:2	RO	0x0	dma_src_state For debug use only. 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved
1:0	RO	0x0	dma_dst_state For debug use only. 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved

**CRYPTO\_DMA\_LLI\_RADDR**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_llr_raddr For debug use only. It indicates the current dma lli read address.

**CRYPTO\_DMA\_SRC\_RADDR**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_src_raddr For debug use only. It indicates the current dma source read address.

**CRYPTO\_DMA\_DST\_WADDR**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_dst_waddr For debug use only. It indicates the current dma destination write address.

**CRYPTO\_DMA\_ITEM\_ID**

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	dma_item_id For debug use only. It indicates the current descriptor ID.

**CRYPTO\_FIFO\_CTL**

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:2	RO	0x0000	reserved
1	RW	0x1	dout_byteswap 1'b1: Little endian 1'b0: Big endian

Bit	Attr	Reset Value	Description
0	RW	0x1	din_byteswap 1'b1: Little endian 1'b0: Big endian

**CRYPTO BC CTL**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	WO	0x000	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:10	RO	0x00	reserved
9:8	RW	0x0	bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES Others: Reserved
7:4	RW	0x0	mode For AES. 4'h0: ECB 4'h1: CBC 4'h2: CTS 4'h3: CTR 4'h4: CFB 4'h5: OFB 4'h6: XTS 4'h7: CCM 4'h8: GCM 4'h9: CMAC 4'hA: CBC-MAC Others: Reserved For TDES/DES. 4'h0: ECB 4'h1: CBC 4'h4: CFB 4'h5: OFB Others: Reserved
3:2	RW	0x0	key_size For AES. 2'b00: 128 bit 2'b01: 192 bit 2'b10: 256 bit 2'b11: Reserved For TDES/DES, it is reserved.
1	RW	0x0	decrypt 1'b1: Decrypt 1'b0: Encrypt
0	RW	0x0	bc_enable 1'b1: Enable 1'b0: Disable

**CRYPTO HASH CTL**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	WO	0x00	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:8	RO	0x00	reserved
7:4	RW	0x0	hash_cipher_sel 4'h0: SHA-1 4'h1: MD-5 4'h2: SHA-256 4'h3: SHA-224 4'h8: SHA-512 4'h9: SHA-384 4'hA: SHA-512/224 4'hB: SHA-512/256 Others: Reserved
3	RW	0x0	hmac_enable Crypto supports HMAC-SHA1, HMAC-SHA256, HMAC_SHA512. 1'b1: Enable 1'b0: Disable
2	RW	0x1	hw_pad_enable 1'b1: Enable 1'b0: Disable
1	RW	0x0	hash_src_sel 1'b1: From TX-FIFO 1'b0: From RX-FIFO
0	RW	0x0	hash_enable 1'b1: Enable 1'b0: Disable

**CRYPTO\_CIPHER\_ST**

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	otp_key_valid Indicate if otp_key is valid. 1'b1: Valid 1'b0: Invalid
1	RO	0x0	hash_busy 1'b1: Busy 1'b0: Idle
0	RO	0x0	block_cipher_busy 1'b1: Busy 1'b0: Idle

**CRYPTO\_CIPHER\_STATE**

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:10	RO	0x01	hash_state For debug use only. 5'h01: IDLE State 5'h02: IPAD State 5'h04: TEXT State 5'h08: OPAD State 5'h10: OPAD EXT State
9:8	RO	0x0	gcm_state For debug use only. 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
7:6	RO	0x0	ccm_state For debug use only. 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
5:4	RO	0x0	parallel_state For debug use only. 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
3:2	RO	0x0	mac_state For debug use only. 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
1:0	RO	0x0	serial_state For debug use only. 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State 2'b11: Reserved

**CRYPTO CHn IV 0**

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_0 Channel N IV[127:96].

**CRYPTO CHn IV 1**

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_1 Channel N IV[95:64].

**CRYPTO CHn IV 2**

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_2 Channel N IV[63:32].

**CRYPTO CHn IV 3**

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_3 Channel N IV[31:0].

**CRYPTO CHn KEY 0**

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_0 Channel N Key[127:96].

**CRYPTO CHn KEY 1**

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_1 Channel N Key[95:64].

**CRYPTO CHn KEY 2**

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_2 Channel N Key[63:32].

**CRYPTO CHn KEY 3**

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_3 Channel N Key[31:0].

**CRYPTO CHn PKEY 0**

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_pkey_0 Channel N PKey[127:96].

**CRYPTO CHn PKEY 1**

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pkey_1 Channel N PKey[95:64].

**CRYPTO CHn PKEY 2**

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pkey_2 Channel N PKey[63:32].

**CRYPTO CHn PKEY 3**

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_3 Channel N PKey[31:0].

**CRYPTO CHn PC LEN 0**

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pc_len_0 Channel N Plain/Cipher Text Length[31:0].

**CRYPTO CHn PC LEN 1**

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	chn_pc_len_1 Channel N Plain/Cipher Text Length[60:32].

**CRYPTO CHn AAD LEN 0**

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_aad_len_0 Channel N additional data Length[31:0].

**CRYPTO CHn AAD LEN 1**

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	chn_aad_len_1 Channel N additional data Length[60:32].

**CRYPTO CHn IV LEN 0**

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x00000000	reserved
4:0	RW	0x00	chn_iv_len Channel N initial vector length. Up to 16 byte IV for GCM.

**CRYPTO CHn TAG 0**

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_0 Channel N tag[127:96].

**CRYPTO CHn TAG 1**

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_1 Channel N tag[95:64].

**CRYPTO CHn TAG 2**

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_2 Channel N tag[63:32].

**CRYPTO CHn TAG 3**

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_3 Channel N tag[31:0].

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_3 Channel N tag[31:0].

**CRYPTO HASH DOUT 0**

Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_0 0'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 1**

Address: Operational Base + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_1 1'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 2**

Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_2 2'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 3**

Address: Operational Base + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_3 3'th output word for all hash function, in big endian. This is MD5 last output word. HASH_DOUT_4 ~ HASH_DOUT_15 is invalid data for MD5.

**CRYPTO HASH DOUT 4**

Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_4 4'th output word for all hash function, in big endian. This is SHA-1 last output word. HASH_DOUT_5 ~ HASH_DOUT_15 is invalid data for SHA-1.

**CRYPTO HASH DOUT 5**

Address: Operational Base + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_5 5'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 6**

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_6 6'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 7**

Address: Operational Base + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_7 7'th output word for all hash function, in big endian. This is SHA-256/224 last output word. HASH_DOUT_8 ~ HASH_DOUT_15 is invalid data for SHA-256/224.

**CRYPTO HASH DOUT 8**

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_8 8'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 9**

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_9 9'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 10**

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_10 10'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 11**

Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_11 11'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 12**

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_12 12'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 13**

Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_13 13'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 14**

Address: Operational Base + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_14 14'th output word for all hash function, in big endian.

**CRYPTO HASH DOUT 15**

Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_15 15'th output word for all hash function, in big endian. This is SHA-512, SHA-384, SHA-512/224, SHA-512/256 last output word.



**CRYPTO\_TAG\_VALID**

Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	ch7_tag_valid When channel 7 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 7 tag is valid. 1'b0: Channel 7 tag is invalid.
6	W1C	0x0	ch6_tag_valid When channel 6 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 6 tag is valid. 1'b0: Channel 6 tag is invalid.
5	W1C	0x0	ch5_tag_valid When channel 5 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 5 tag is valid. 1'b0: Channel 5 tag is invalid.
4	W1C	0x0	ch4_tag_valid When channel 4 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 4 tag is valid. 1'b0: Channel 4 tag is invalid.
3	W1C	0x0	ch3_tag_valid When channel 3 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 3 tag is valid. 1'b0: Channel 3 tag is invalid.
2	W1C	0x0	ch2_tag_valid When channel 2 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 2 tag is valid. 1'b0: Channel 2 tag is invalid.
1	W1C	0x0	ch1_tag_valid When channel 1 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 1 tag is valid. 1'b0: Channel 1 tag is invalid.
0	W1C	0x0	ch0_tag_valid When channel 0 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: Channel 0 tag is valid. 1'b0: Channel 0 tag is invalid.

**CRYPTO\_HASH\_VALID**

Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	hash_valid When HASH calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b1: HASH_DOUT is valid. 1'b0: HASH_DOUT is invalid.

**CRYPTO\_VERSION**

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x01010000	version_num

**CRYPTO\_RNG\_CTL**

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	WO	0x00	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:6	RO	0x000	reserved
5:4	RW	0x0	rng_len 2'b00: 64 bit 2'b01: 128 bit 2'b10: 192 bit 2'b11: 256 bit
3:2	RW	0x0	ring_sel There are 4 osc rings choice to decide the rng output data. 2'b00: Fastest osc ring 2'b01: Slower than osc ring 0 2'b10: Slower than osc ring 1 2'b11: Slowest osc ring
1	RW	0x0	rng_enable 1'b1: Enable 1'b0: Disable
0	R/WSC	0x0	rng_start The application triggers this bit to start collect rng output data. After rng is started, CRYPTO will clear the bit automatically. 1'b1: Start 1'b0: Do nothing

**CRYPTO\_RNG\_SAMPLE\_CNT**

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rng_sample_cnt RNG collects osc ring output bit every rng_sample_cnt time. The value of rng_sample_cnt affects RNG output data rate, the value more bigger, the rate more slower.

**CRYPTO\_RNG\_DOUT\_0**

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_0 The 32'th osc ring bit is captured in RNG_DOUT_0.bit31.

**CRYPTO RNG DOUT 1**

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_1 The 64'th osc ring bit is captured in RNG_DOUT_1.bit31. If RNG_CTL.rng_len = 0x00, the last valid bit of RNG is stored in RNG_DOUT_1.bit31, and RNG_DOUT_2 ~ RNG_DOUT_7 are invalid.

**CRYPTO RNG DOUT 2**

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_2 The 96'th osc ring bit is captured in RNG_DOUT_2.bit31.

**CRYPTO RNG DOUT 3**

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_3 The 128'th osc ring bit is captured in RNG_DOUT_3.bit31. If RNG_CTL.rng_len = 0x01, the last valid bit of RNG is stored in RNG_DOUT_3.bit31, and RNG_DOUT_4 ~ RNG_DOUT_7 are invalid.

**CRYPTO RNG DOUT 4**

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_4 The 160'th osc ring bit is captured in RNG_DOUT_4.bit31.

**CRYPTO RNG DOUT 5**

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_5 The 192'th osc ring bit is captured in RNG_DOUT_5.bit31. If RNG_CTL.rng_len = 0x02, the last valid bit of RNG is stored in RNG_DOUT_5.bit31, and RNG_DOUT_6~ RNG_DOUT_7 are invalid.

**CRYPTO RNG DOUT 6**

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rng_dout_6 The 224'th osc ring bit is captured in RNG_DOUT_6.bit31.

**CRYPTO RNG DOUT 7**

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rng_dout_7 The 256'th osc ring bit is captured in RNG_DOUT_7.bit31. If RNG_CTL.rng_len = 0x03, the last valid bit of RNG is stored in RNG_DOUT_7.bit31.

**CRYPTO\_RAM\_CTL**

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0000	reserved
0	RW	0x0	ram_pka_rdy Indicate whether ram is controlled by PKA engine. 1'b0: Ram is controlled by CPU 1'b1: Ram is controlled by CRYPTO PKA engine

**CRYPTO\_RAM\_ST**

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	clk_ram_rdy Indicate whether clk_ram is stable, and ready for use. 1'b0: Not stable 1'b1: Stable

**CRYPTO\_DEBUG\_CTL**

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0000	reserved
0	RW	0x0	pka_debug_mode 1'b1: PKA is in debug mode. 1'b0: PKA is in normal mode.

**CRYPTO\_DEBUG\_ST**

Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_debug_clk_en For debug use only. 1'b1: Enable 1'b0: Disable

**CRYPTO\_DEBUG\_MONITOR**

Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000feef	pka_monitor_bus For debug use only.

**CRYPTO\_PKA\_MEM\_MAP0**

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map0 Memory map 0 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP1**

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map1 Memory map 1 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP2**

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map2 Memory map 2 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP3**

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map3 Memory map 3 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP4**

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map4 Memory map 4 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP5**

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map5 Memory map 5 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP6**

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map6 Memory map 6 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP7**

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map7 Memory map 7 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP8**

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map8 Memory map 8 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP9**

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map9 Memory map 9 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP10**

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map10 Memory map 10 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP11**

Address: Operational Base + offset (0x082C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map11 Memory map 11 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP12**

Address: Operational Base + offset (0x0830)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map12 Memory map 12 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP13**

Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map13 Memory map 13 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP14**

Address: Operational Base + offset (0x0838)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map14 Memory map 14 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP15**

Address: Operational Base + offset (0x083C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map15 Memory map 15 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP16**

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map16 Memory map 16 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP17**

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map17 Memory map 17 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP18**

Address: Operational Base + offset (0x0848)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map18 Memory map 18 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP19**

Address: Operational Base + offset (0x084C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map19 Memory map 19 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP20**

Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map20 Memory map 20 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP21**

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map21 Memory map 21 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP22**

Address: Operational Base + offset (0x0858)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map22 Memory map 22 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP23**

Address: Operational Base + offset (0x085C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map23 Memory map 23 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP24**

Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map24 Memory map 24 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP25**

Address: Operational Base + offset (0x0864)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map25 Memory map 25 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP26**

Address: Operational Base + offset (0x0868)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map26 Memory map 26 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP27**

Address: Operational Base + offset (0x086C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map27 Memory map 27 [11:2], bit[1:0] is stuck to 0.



Bit	Attr	Reset Value	Description
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP28**

Address: Operational Base + offset (0x0870)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map28 Memory map 28 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP29**

Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map29 Memory map 29 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP30**

Address: Operational Base + offset (0x0878)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map30 Memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA MEM MAP31**

Address: Operational Base + offset (0x087C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map31 Memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

**CRYPTO PKA OPCODE**

Address: Operational Base + offset (0x0880)

Bit	Attr	Reset Value	Description
31:27	WO	0x00	opcode Defines the PKA operation. 5'h04: Add, Inc 5'h05: Sub, Dec, Neg 5'h06: ModAdd, ModInc 5'h07: ModSub, ModDec, ModNeg 5'h08: AND, TST0, CLR0 5'h09: OR, COPY, SET0 5'h0A: XOR, FLIP0, INVERT, COMPARE 5'h0B: SHR0 5'h0D: SHR1 5'h0E: SHL0 5'h0F: SHL1 5'h10: MulLow 5'h11: ModMul 5'h12: ModMulN 5'h13: ModExp 5'h14: Division 5'h15: Div 5'h16: ModDiv 5'h00: Terminate
26:24	WO	0x0	len The virtual length address 0-7. Virtual address 0 point to PKA_L0. Virtual address 1 point to PKA_L1. ... Virtual address 7 point to PKA_L7.
23:18	WO	0x00	reg_a Operand A virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
17:12	WO	0x00	reg_b Operand B virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
11:6	WO	0x00	reg_r Result register virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
5:0	WO	0x00	tag Tag

**CRYPTO N NP TO T1 ADDR**

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x1f	reg_t1 Virtual address of temporary register number 1. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
14:10	RW	0x1e	reg_t0 Virtual address of temporary register number 0. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
9:5	RW	0x01	reg_np Virtual address of register np. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
4:0	RW	0x00	reg_n Virtual address of register n. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.

**CRYPTO PKA STATUS**

Address: Operational Base + offset (0x0888)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:14	RO	0x00	tag Tag of the Last Operation.
13:9	RO	0x00	opcode The last OPCODE.
8	RO	0x0	pka_cpu_busy PKA is busy memory control is by PKA.
7	RO	0x0	modinv_of_zero Modular inverse of zero flag.
6	RO	0x0	alu_sign_out Sign of the last operation(MSB).
5	RO	0x0	alu_carry Carry of the last ALU operation.
4	RO	0x0	div_by_zero Division by 0.
3	RO	0x0	alu_mod_ovflw Modular overflow flag.
2	RO	0x0	alu_out_zero ALU out is 0.
1	RO	0x0	pka_busy PKA is busy.
0	RO	0x1	pipe_is_busy PKA ready signal. 1'b0: Pipe full 1'b1: PKA ready for new command

**CRYPTO PKA SW RESET**

Address: Operational Base + offset (0x088C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	pka_sw_reset PKA software reset the reset mechanism will take about four PKA clocks until the reset line is de-asserted.

**CRYPTO PKA L0**

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l0 PKA length 0, in bit unit.

**CRYPTO PKA L1**

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l1 PKA length 1, in bit unit.

**CRYPTO PKA L2**

Address: Operational Base + offset (0x0898)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l2 PKA length 2, in bit unit.

**CRYPTO PKA L3**

Address: Operational Base + offset (0x089C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l3 PKA length 3, in bit unit.

**CRYPTO PKA L4**

Address: Operational Base + offset (0x08A0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l4 PKA length 4, in bit unit.

**CRYPTO PKA L5**

Address: Operational Base + offset (0x08A4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l5 PKA length 5, in bit unit.

**CRYPTO PKA L6**

Address: Operational Base + offset (0x08A8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l6 PKA length 6, in bit unit.

**CRYPTO PKA L7**

Address: Operational Base + offset (0x08AC)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l7 PKA length 7, in bit unit.

**CRYPTO PKA PIPE RDY**

Address: Operational Base + offset (0x08B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_pipe_rdy PKA pipe is ready for new opcode.

**CRYPTO PKA DONE**

Address: Operational Base + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_done PKA operation is completed and pipe is empty.

**CRYPTO PKA MON SELECT**

Address: Operational Base + offset (0x08B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x00000000	reserved
3:0	RW	0x0	pka_mon_select PKA monitor select which PKA fsm monitor is being output.

**CRYPTO PKA DEBUG REG EN**

Address: Operational Base + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pka_debug_reg_en Enable all the debug mechanism when set.

**CRYPTO DEBUG CNT ADDR**

Address: Operational Base + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	R/WSC	0x00000	debug_cnt_addr The clock counter initial values. clock is disabled when counter expires. Triggered when pka_debug_en is set.

**CRYPTO DEBUG EXT ADDR**

Address: Operational Base + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	debug_ext_addr Disable the debug Mechanism.

**CRYPTO PKA DEBUG HALT**

Address: Operational Base + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pka_debug_halt In debug mode: PKA is in halt state.

**CRYPTO PKA MON READ**

Address: Operational Base + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000feef	pka_mon_read This is the PKA monitor bus register output.

**CRYPTO PKA INT\_ENA**

Address: Operational Base + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pka_int_ena 1'b1: Enable pka interrupt 1'b0: Disable pka interrupt

**CRYPTO PKA INT\_ST**

Address: Operational Base + offset (0x08D8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	pka_int_st Indicate that PKA operation completes. After the bit is read, the application should write 1 to clear this bit for next time use.

**CRYPTO SRAM\_ADDR**

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x7fff2fff	sram_addr Sram address starts from 0x1000 to 0x1fff. When RAM_CTL.ram_pka_rdy == 0, application could access sram. Otherwise, application can't.

**14.4 Application Notes****14.4.1 Clock & Reset**

There are 4 clock domains in Crypto. The clock and reset signals are described in the following table.

Table 14-1 Crypto Clock &amp; Reset Description

Signal	Attr	Description
hclk	clock	AHB clock
aclk	clock	AXI master clock
clk_core	clock	Cipher work clock
clk_pka	clock	PKA work clock
hresetn	reset	Asynchronously assert, synchronously de-assert to hclk, low active
aresetn	reset	Asynchronously assert, synchronously de-assert to aclk, low active
resetn_core	reset	Asynchronously assert, synchronously de-assert to clk_core, low active
resetn_pka	reset	Asynchronously assert, synchronously de-assert to clk_pka, low active

Each function needs different clocks. The applications could gate the un-used clock to save power. Please see the following table for detail information.

Table 14-2 Crypto Clock &amp; Reset Description

Operation	HCLK	ACLK	CLK_CORE	CLK_PKA
AES	ON	ON	ON	OFF

Operation	HCLK	ACLK	CLK_CORE	CLK_PKA
DES/TDES	ON	ON	ON	OFF
HASH/HMAC	ON	ON	ON	OFF
PKA	ON	OFF	OFF	ON
TRNG	ON	OFF	OFF	OFF

Even when CLK\_CORE is on, Crypto is doing some cipher job. And Crypto could still be able to automatically gate most parts of un-used blocks to save more power, if CRYPTO\_CLK\_CTL.auto\_clkgate\_en is set to '1'. The default value for this bit is also '1'. Application could do a soft reset to a certain clock domain. Please refer to "Chapter CRU" for more details.

#### 14.4.2 Performance

Cipher performance is shown in the following table.

Table 14-3 Crypto Performance Description

Algorithm	block size (Byte)	clk_core frequency (Mhz)	cycle	serial max throughput (MBps)	parallel max throughput (MBps)
DES	8	200	18	88	352
TDES	8	200	55	29	116
AES-128	16	200	12	266	1066
AES-192	16	200	14	228	914
AES-256	16	200	16	200	800
SHA-1	64	200	81	158	NA
MD5	64	200	65	196	NA
SHA-256/224	64	200	65	196	NA
SHA-512/384/ 512_224/ 512_256	128	200	81	316	NA

There are 2 column throughput rates in the table, 1 is serial mode, the other is parallel mode. In parallel mode, there are 4 engines working at the same time. So the speed is 4 times than serial mode. Parallel mode includes ECB/CTR/XTS both encryption and decryption mode, CFB/CBC/CTS only decryption mode. Other modes are serial. HASH doesn't have parallel mode.

For PKA, the cycles for each calculation are not certain. It depends on the parameters. Take RSA-2048 for example, it takes about 28M cycles to finish a calculation. PKA can run 300 Mhz. It means it can run over 10 times per second.

#### 14.4.3 DMA

DMA supports Link List Item (LLI) DMA transaction.

- Each item contains 8 bytes, and start address should be 8 bytes align.
- We suggest that DATA start address is 8 bytes align.
- Total DATA length is byte align.
- Support segmenting HASH/HMAC DATA into multi sections. We suggest that each section DATA length is a multiple of 64 bytes, except this section is the last section.

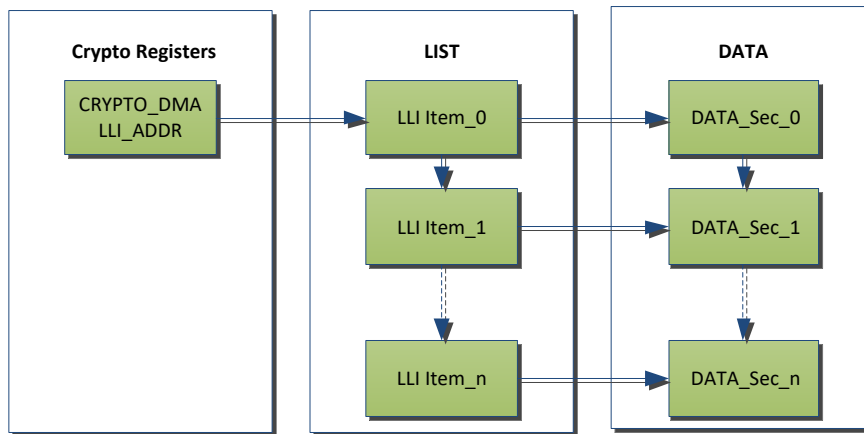


Fig.14-2 LLI DMA Usage

As shown in the Figure above, Register CRYPTO\_DMA\_LLI\_ADDR points to 1'st LLI item in external memory. Each LLI item contains DATA address, length, control information and next LLI item pointer, except the last LLI item. The last item doesn't have the next LLI item pointer. After the last LLI item is finished, DMA will go to idle state. LLI item definition is shown in the following table.

Table 14-4 LLI Item Description

offset	Def	Description
0x00	SRC_ADDRESS[31:0]	source data start address
0x04	SRC_LENGTH[31:0]	source data length, in byte unit
0x08	DST_ADDRESS[31:0]	destination data start address
0x0c	DST_LENGTH[31:0]	destination data length, in byte unit
0x10	USER_DEFINE[31:0]	used in cipher block
0x14	reserve	reserve
0x18	DMA_CTRL[31:0]	used in DMA block
0x1c	next address[31:0]	next LLI item address. When DMA_CTRL.LAST = "1", NEXT_ADDRESS is invalid.

DMA\_CTRL: the definition is shown in the following table.

Table 14-5 LLI Item dma\_ctl Description

Bit	Def	Definition
[31:24]	ITEM_ID[7:0]	used to identify LLI items.
[23:16]	reserve	reserve
[15:11]	reserve	reserve
10	source_item_done enable	When source data fetch is completed, CRYPTO_DMA_INT_ST.source_item_done will assert if this bit is set.
9	reserved	reserved
8	list_done enable	When all LLI items transfer is completed, CRYPTO_DMA_INT_ST.list_done will assert if this bit is set.
[7:2]	reserved	reserved
1	PAUSE	indicate DMA will hold on after executes current item. DMA won't go on unless CRYPTO_DMA_CTL.restart is configured



Bit	Def	Definition
0	LAST	indicate current item is the last one. After executes current item, DMA will return to IDLE state.

Table 14-6 LLI Item user\_define Description

Bit	Signal	Description
31:9	Reserved	Reserved
8	otpkey_sel	otpkey select. 1: select otpkey; 0: select register key
7	Privacy_sel	pkey select. 1: select pkey ; 0: select key ;
6:4	Chnl_num	channel number, from 0 to 7 .
3	String_attr	indicate current item's attribution. 1: ADA ; 0: PC(plaintext or ciphertext)
2	String_last	indicate current item is the string last item
1	String_start	indicate current item is the string first item
0	Cipher_start	indicate current item is the cipher first item

#### 14.4.4 Multi-Channel Map

There are 8-channel configurations for AES or DES/TDES operation. For different key-size, the map is different. Please find the register map in the following table.

Table 14-7 LLI Item user\_define Description

Cipher sel	otpkey sel	privacy sel	chnl num	key	iv(tag/...)
AES-128/ DES	0	0	0	CH0_KEY0-3/ CH0_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	0	0	n	CHn_KEY0-3/ CHn_KEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	0	0	7	CH7_KEY0-3/ CH7_KEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-128/ DES	0	1	0	CH0_PKEY0-3/ CH0_PKEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	0	1	n	CHn_PKEY0-3/ CHn_PKEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	0	1	7	CH7_PKEY0-3/ CH7_PKEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-128/ DES	1	NA	0	OTP_KEY[255:128]	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	1	NA	n	OTP_KEY[127:0]	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	1	NA	7	OTP_KEY[127:0]	CH7_IV0-3/ CH7_IV0-1
AES-192/ TDES	0	0	0	CH0_KEY0-3, CH1_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	0	0	1	CH2_KEY0-3, CH3_KEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/ TDES	0	0	2	CH4_KEY0-3, CH5_KEY0-1	CH2_IV0-3/ CH2_IV0-1

Cipher sel	otpkey sel	privacy sel	chnl num	key	iv(tag/...)
AES-192/TDES	0	0	3	CH6_KEY0-3, CH7_KEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/TDES	0	1	0	CH0_PKEY0-3, CH1_PKEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/TDES	0	1	1	CH2_PKEY0-3, CH3_PKEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/TDES	0	1	2	CH4_PKEY0-3, CH5_PKEY0-1	CH2_IV0-3/ CH2_IV0-1
AES-192/TDES	0	1	3	CH6_PKEY0-3, CH7_PKEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/TDES	0	NA	4-7	not supported	not supported
AES-192/TDES	1	NA	0	OTP[255:64]	CH0_IV0-3/ CH0_IV0-1
AES-192/TDES	1	NA	1-7	not supported	not supported
AES-256	0	0	0	CH0_KEY0-3, CH1_KEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	0	0	1	CH2_KEY0-3, CH3_KEY0-3	CH1_IV0-3/ CH1_IV0-1
AES-256	0	0	2	CH4_KEY0-3, CH5_KEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	0	0	3	CH6_KEY0-3, CH7_KEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	0	1	0	CH0_PKEY0-3, CH1_PKEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	0	1	1	CH2_PKEY0-3, CH3_PKEY0-3	CH1_IV0-3/ CH1_IV0-1
AES-256	0	1	2	CH4_PKEY0-3, CH5_PKEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	0	1	3	CH6_PKEY0-3, CH7_PKEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	0	NA	4-7	not supported	not supported
AES-256	1	NA	0	OTP[255:0]	CH0_IV0-3/ CH0_IV0-1
AES-256	1	NA	1-7	not supported	not supported

In AES-XTS mode, there are 2 keys, and only AES-128 and AES-256 mode are. Please refer to the following table for detail information.

Table 14-8 LLI Item user\_define Description

Cipher sel	otpkey sel	privacy sel	chnl num	key1	key2	tweak
AES-128	0	0	0	CH0_KEY0-3	CH4_KEY0-3	CH0_IV0-3

Cipher sel	otpkey sel	privacy sel	chnl num	key1	key2	tweak
AES-128	0	0	1	CH1_KEY0-3	CH5_KEY0-3	CH1_IV0-3
AES-128	0	0	2	CH2_KEY0-3	CH6_KEY0-3	CH2_IV0-3
AES-128	0	0	3	CH3_KEY0-3	CH7_KEY0-3	CH3_IV0-3
AES-128	0	1	0	CH0_PKEY0-3	CH4_PKEY0-3	CH0_IV0-3
AES-128	0	1	1	CH1_PKEY0-3	CH5_PKEY0-3	CH1_IV0-3
AES-128	0	1	2	CH2_PKEY0-3	CH6_PKEY0-3	CH2_IV0-3
AES-128	0	1	3	CH3_PKEY0-3	CH7_PKEY0-3	CH3_IV0-3
AES-128	0	NA	4-7	not supported	not supported	not supported
AES-128	1	NA	NA	not supported	not supported	not supported
AES-256	0	0	0	CH0_KEY0-3, CH1_KEY0-3	CH4_KEY0-CH5_KEY3	CH0_IV0-3
AES-256	0	0	1	CH2_KEY0-3, CH3_KEY0-3	CH6_KEY0-CH7_KEY3	CH1_IV0-3
AES-256	0	1	0	CH0_PKEY0-3, CH1_PKEY0-3	CH4_PKEY0-CH5_PKEY3	CH0_IV0-3
AES-256	0	1	1	CH2_PKEY0-3, CH3_PKEY0-3	CH6_PKEY0-CH7_PKEY3	CH1_IV0-3
AES-256	0	NA	2-7	not supported	not supported	not supported
AES-256	1	NA	NA	not supported	not supported	not supported

Note: The difference between CHn\_KEY and CHn\_PKEY is that: CHn\_KEY could be read/write, CHn\_PKEY could be write, but can't be read. The read value for CHn\_PKEY is all '0'.

#### 14.4.5 HASH Data Path

HASH and AES could run in parallel way. There are 2 paths lead to AES-HASH function. One is AES-HASH-RX mode, the other is AES-HASH-TX mode.

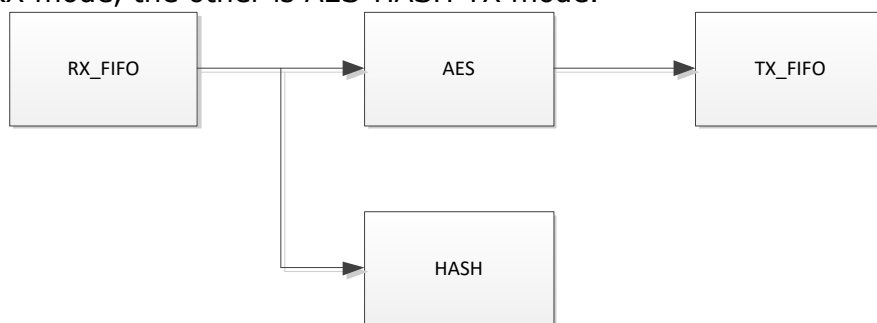


Fig.14-3 AES-HASH-RX mode

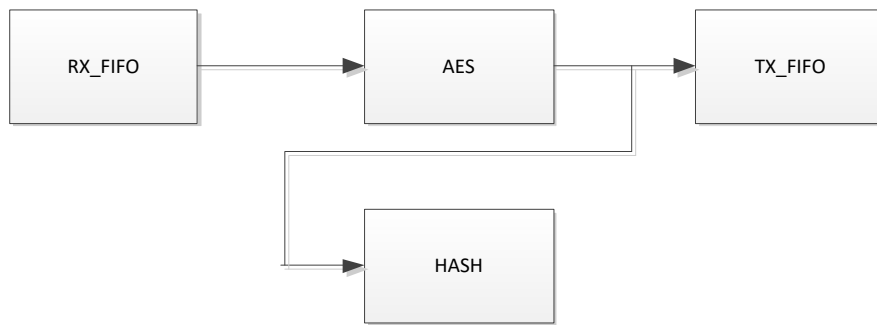


Fig.14-4 AES-HASH-TX mode

As shown in the figures above, we could facilitate operations in some cases. For example, secure boot, we need both AES and HASH operations for the same blocks of data. The data HASH gets from RX\_FIFO or TX\_FIFO is byte-swapped if the byte-swap function is configured.

#### 14.4.6 Program Steps

The application could succeed various crypto operations if they program properly.

- Program the LLI address to DMA\_LLI\_ADDR;
- Program KEY , IV, or other parameter if needed ;
- Program BC\_CTL or HASH\_CTL for control information;
- Prepare LLI Item;
- Enable interrupt, or do nothing.

All these operations could be in any order.

- Program DMA\_CTL.start to start the operation;

This step should be the last configuration step. After this register is configured, other registers should not be changed.

- Wait interrupt asserted, or just poll the DMA\_INT\_ST bits .
- Program DMA\_INT\_ST to clear interrupt status, and get the result.

The application could also use LLI.pause when the next LLI item is not ready. After the new item is prepared, the application could program DMA\_CTL.restart to continue previous operation.

## Chapter 15 Process-Voltage-Temperature Monitor (PVTM)

### 15.1 Overview

The Process-Voltage-Temperature Monitor (PVTM) is used to monitor the chip performance variance caused by chip process, voltage and temperature.

PVTM supports the following features:

- A clock oscillation ring is integrated and used to generate a clock like signal, the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit.
- A calculation logic is used to measure the frequency of the clock oscillation ring.
- Follow PVTM blocks are supported:
  - CPU\_PVTM, used near CPU
  - NPU\_PVTM, used near NPU
  - PMU\_PVTM, used near PMU

### 15.2 Block Diagram

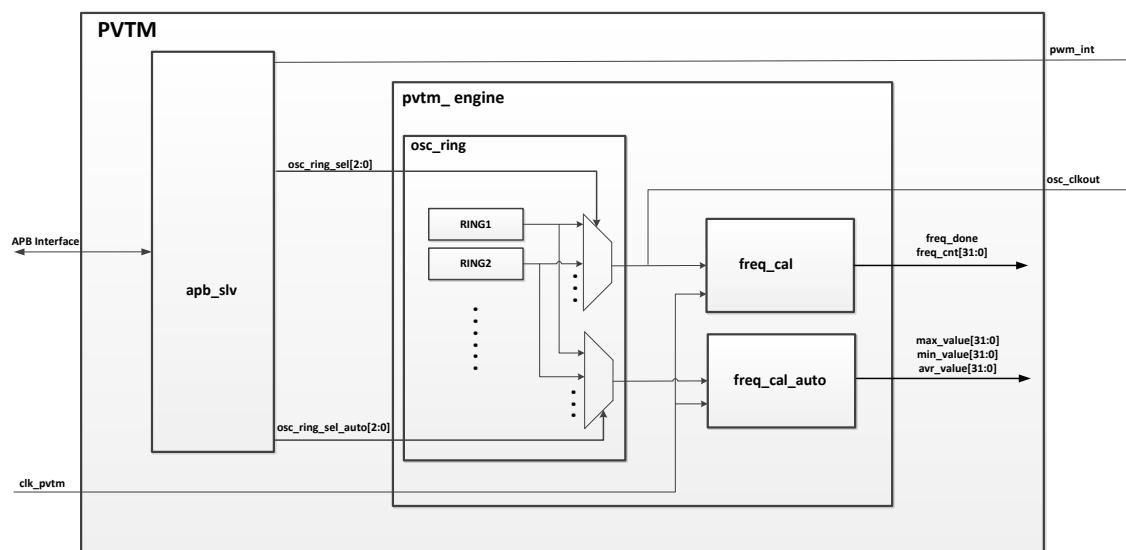


Fig. 15-1 PVTM Block Diagram

The PVTM include two main blocks:

- apb\_slv  
APB slave interface with 32-bit bus width.
- pvtm\_engine

It is composed with inverters with odd number, which is used to generate a clock.

CPU/NPU\_PVTM supports several clock oscillation rings, and finally selects one. PMU\_PVTM only supports one clock oscillation ring.

The frequency calculation logic of CPU/NPU\_PVTM support manual mode and auto mode, and these two modes can be used at simultaneously. The PMU\_PVTM only support manual mode.

### 15.3 Function Description

#### 15.3.1 Frequency Calculation

A clock is generated by the oscillation ring and a frequency fixed clock `clk_pvtm` is used to calculate the cycles of the clock. Supposing the time period is 1s, then the clock period of oscillation ring clock is  $T = 1/\text{clock\_counter(s)}$ , the cell delay value is  $T/2$ .

For manual mode, user can only get one frequency result for a calculation.

For auto mode, user can set the calculation times, and get the maximum, minimum and average frequency during calculation. It also support to generate an interrupt when the minimum or average frequency below a threshold. The threshold can be configured.

#### 15.3.2 Low power mode usage

A clock divided from PMU\_PVTM oscillation ring is used in low power mode, which can

replace the function of 32KHz clock source

## 15.4 Register Description

### 15.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PVTM_VERSION	0x0000	W	0x00000203	PVTM version register
PVTM_CON0	0x0004	W	0x00000000	PVTM control register0
PVTM_CON1	0x0008	W	0x00000000	PVTM control register 1
PVTM_CON2	0x000C	W	0x00000000	PVTM control register 2
PVTM_CON3	0x0010	W	0x00000000	PVTM control register 3
PVTM_CON4	0x0014	W	0x00000000	PVTM control register 4
PVTM_CON5	0x0018	W	0x00000000	PVTM control register 5
PVTM_CON6	0x001C	W	0x00000000	PVTM control register 6
PVTM_INT_EN	0x0070	W	0x00000000	PVTM Interrupt Enable Register
PVTM_INTSTS	0x0074	W	0x00000000	PVTM Interrupt Status Register
PVTM_STATUS0	0x0080	W	0x00000000	PVTM status register0
PVTM_STATUS1	0x0084	W	0x00000000	PVTM status register1
PVTM_STATUS2	0x0088	W	0x00000000	PVTM status register2
PVTM_STATUS3	0x008C	W	0x00000000	PVTM status register3
PVTM_STATUS4	0x0090	W	0x00000000	PVTM status register4
PVTM_STATUS5	0x0094	W	0x00000000	PVTM status register5
PVTM_STATUS6	0x0098	W	0x00000000	PVTM status register6
PVTM_STATUS7	0x009C	W	0x00000000	PVTM status register7

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

### 15.4.2 Detail Register Description

#### PVTM\_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RU	0x0203	version PVTM version

#### PVTM\_CON0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pvtm_rnd_seed_en Set high to enable the round seed in PVTM.

Bit	Attr	Reset Value	Description
4:2	RW	0x0	<p>pvtm_osc_sel</p> <p>Oscillation ring selection</p> <p>3'b000: oscillation ring 0</p> <p>3'b001: oscillation ring 1</p> <p>3'b010: oscillation ring 2</p> <p>3'b011: oscillation ring 3</p> <p>3'b100: oscillation ring 4</p> <p>3'b101: oscillation ring 5</p> <p>3'b110: oscillation ring 6</p> <p>others: Reserved</p>
1	RW	0x0	<p>pvtm_osc_en</p> <p>Set high to enable the oscillation ring in the PVTM.</p>
0	RW	0x0	<p>pvtm_start</p> <p>Set high to start PVTM.</p>

**PVTM\_CON1**

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>pvtm_cal_cnt</p> <p>PVTM calculation counter</p>

**PVTM\_CON2**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	<p>write_enable</p> <p>write_enable</p> <p>Write enable for lower 16 bits, each bit is individual.</p> <p>1'b0: Write access disable</p> <p>1'b1: Write access enable</p>
15:8	RW	0x00	<p>pvtm_osc_ring_autosel_en</p> <p>PVTM oscillation ring auto select enable control. It will take turns the oscillation ring (enabled by pvtm_osc_ring_autosel_en[7:0]) in order and then loop back. When none of them is enabled, use the oscillation ring selected by pvtm_osc_sel_auto.</p> <p>pvtm_osc_ring_autosel_en[0]: auto select enable 0</p> <p>pvtm_osc_ring_autosel_en[1]: auto select enable 1</p> <p>pvtm_osc_ring_autosel_en[2]: auto select enable 2</p> <p>pvtm_osc_ring_autosel_en[3]: auto select enable 3</p> <p>pvtm_osc_ring_autosel_en[4]: auto select enable 4</p> <p>pvtm_osc_ring_autosel_en[5]: auto select enable 5</p> <p>pvtm_osc_ring_autosel_en[6]: auto select enable 6</p> <p>pvtm_osc_ring_autosel_en[7]: reserved, must be 0</p>

Bit	Attr	Reset Value	Description
7	RW	0x0	pvtm_avr_cal_mode PVTM average value calculate mode 1'b0: The average value = (summary_value-max_value-min_value) /(measurement_number-2) 1'b1: The average value = summary_value /measurement_number
6	RW	0x0	pvtm_avr_update_mode PVTM average value update mode 1'b0: Only when the number of measurement arrive pvtm_avr_period, the average value is updated. 1'b1: When the number of measurement is equal to or greater than 3, the average value is updated gradually.
5	RW	0x0	pvtm_start_auto_mode PVTM start mode 1'b0: When the number of measurement arrive pvtm_cal_period, calculate stop and pvtm_start_auto is cleared. 1'b1: When the number of measurement arrive pvtm_cal_period, calculate don't stop and pvtm_start_auto is not cleared.
4:2	RW	0x0	pvtm_osc_sel_auto Oscillation ring selection for auto mode 3'b000: oscillation ring 0 3'b001: oscillation ring 1 3'b010: oscillation ring 2 3'b011: oscillation ring 3 3'b100: oscillation ring 4 3'b101: oscillation ring 5 3'b110: oscillation ring 6 others: Reserved
1	RW	0x0	pvtm_osc_en_auto Set high to enable the oscillation ring in the PVTM for auto mode.
0	RW	0x0	pvtm_start_auto Set high to start PVTM for auto mode.

**PVTM\_CON3**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_cal_cnt_auto PVTM calculation counter for auto mode

**PVTM\_CON4**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pvtm_avr_period PVTM average calculation period



Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pvtm_cal_period PVTM calculation period

**PVTM\_CON5**

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_min_threshold PVTM minimum value threshold

**PVTM\_CON6**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_avr_threshold PVTM average value threshold

**PVTM\_INT\_EN**

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	cal_done_Int_en 1'b0: Calculation done Interrupt disabled 1'b1: Calculation done Interrupt enabled
1	RW	0x0	avr_value_Int_en 1'b0: Average value Interrupt disabled 1'b1: Average value Interrupt enabled
0	RW	0x0	min_value_Int_en 1'b0: Minimum value Interrupt disabled 1'b1: Minimum value Interrupt enabled

**PVTM\_INTSTS**

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	cal_done_IntSts 1'b0: Calculation done Interrupt not generated 1'b1: Calculation done Interrupt generated
1	W1C	0x0	avr_value_IntSts 1'b0: Average value Interrupt not generated 1'b1: Average value Interrupt generated
0	W1C	0x0	min_value_IntSts 1'b0: Minimum value Interrupt not generated 1'b1: Minimum value Interrupt generated

**PVTM\_STATUS0**

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pvtm_freq_done Indicates PVTM frequency count done.

**PVTM STATUS1**

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_freq_cnt Indicates the cycle counts of the OSC_RING clock.

**PVTM STATUS2**

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_rnd_seed_low_bits Indicates low 32bits of the cycle count of round seed.

**PVTM STATUS3**

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_rnd_seed_high_bits Indicates high 32bits of the cycle count of round seed.

**PVTM STATUS4**

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_min_value PVTM minimum value

**PVTM STATUS5**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_avr_value PVTM average value

**PVTM STATUS6**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_max_value PVTM maximum value

**PVTM STATUS7**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pvtm_avr_cnt PVTM average calculation current count
15:0	RO	0x0000	pvtm_cal_cnt PVTM calculation current counter

## 15.5 Application Notes

### 15.5.1 PVTM Manual mode Usage Flow

1. Enable the frequency fixed clock clk\_pvtm.
2. Reset the PVTM.
3. Set pvtm\_osc\_en to enable the generated clock.
4. Set pvtm\_osc\_sel to select the clock oscillation ring.
5. Set the pvtm\_cal\_cnt to an appropriate value.
6. Set pvtm\_start to calculate the cycles of the generated clock.
7. Wait the pvtm\_freq\_done is asserted, then get the value of pvtm\_freq\_cnt. The period OSC\_RING clock is  $T = \text{cal\_cnt} * (\text{Period of clk\_pvtm clock}) / \text{freq\_cnt}$ , the cell delay value is  $T/2$ .

### 15.5.2 PVTM Auto mode Usage Flow

1. Enable the frequency fixed clock clk\_pvtm.
2. Reset the PVTM.
3. Set pvtm\_osc\_en\_auto to enable the generated clock.
4. Set pvtm\_osc\_sel\_auto to select the clock oscillation ring.
5. Set pvtm\_cal\_cnt\_auto to an appropriate value.
6. Set pvtm\_cal\_period to configure the all calculation times
7. Set pvtm\_avr\_period to configure the average times
8. Set cal\_done\_Int\_en to enable the interrupt
9. Set pvtm\_start\_auto to calculate the cycles of the generated clock.
10. Wait the interrupt is asserted, then get the value of pvtm\_min\_value/pvtm\_max\_value/pvtm\_avr\_value. The minimum period OSC\_RING clock is  $T = \text{cal\_cnt\_auto} * (\text{Period of clk\_pvtm clock}) / \text{pvtm\_min\_value}$ , the minimum cell delay value is  $T/2$ . The frequency calculation of average and maximum value are same with minimum value.